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Proposed Adder and Modified LUT Bit Parallel Unrolled CORDIC Circuit for an Application in Mobile Robots

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ABSTRACT

The advent of reconfigurable computers allows the higher performance of dedicated hardware solutions that are competitive with the conventional software approach. The Coordinate Rotation Digital Computer (CORDIC) circuit gives a smart applications of robotic performance. This research is to design a CORDIC circuit for robotic applications, the modified Lookup-Table (LUT) and Mux-Shannon adder circuits are proposed and implemented in bit parallel unrolled CORDIC circuit. The proposed LUT and Mux-Shannon adder based unrolled CORDIC circuit is designed using by DSCH2 VLSI CAD tool and their layout is generated with Microwind 3 VLSI CAD tool. A simulation using BSIM4 analyzer is used to evaluate the performance of CORDIC cell for anticipation of mobile robot. The parameter analysis is done using BSIM4 analyzer. The output parameters such as area, power dissipation and propagation delay are calculated from CORDIC cell layout which obtained by simulation results. Lookup-Table (LUT) and Mux-Shannon adder based CORDIC circuit design enhances the low energy and improved speed. The simulated results of modified LUT and proposed Mux-Shannon adder based CORDIC circuit are compared with other published adder's that are connected with CORDIC circuit. From the simulated result analysis, the modified LUT and proposed Mux-Shannon adder based unrolled CORDIC circuit gives better performance in terms of speed performance, power characteristics and propagation delay than former published outcomes.

Key words: Mobile robot, modified LUT, unrolled CORDIC, BSIM4 analyzer, Monte-Carlo

INTRODUCTION

The Robotic technology has found its applications in many fields such as security system, office automation, dangerous environment detection, military, space exploration, entertainment and factory automation. Nowadays, many researchers show their involvements in intelligent service robot. The performance such as auto-recharging within the stipulated time for mobile robot is designed by Luo and Su (2008). Mobile robots which are autonomic in nature have built in machine intelligence and an onboard control system which helps to perform the task without the human intervention. Autonomous robots' onboard control system have characters like light weight, low power consumption and small size which are mostly used in embedded controllers during real operation (Baturone *et al*., 2008). This article mainly focus on to improve the performance of mobile robot in terms of power consumption, fast response, speed and delay.

A CORDIC unit using simple hardware components such as shifters and adders has received much attention because of the efficient implementations in various types of rotations. CORDIC units are flexible relatively simple and can work parallely with no idle time and hence are used as basic elements for processor arrays in scientific computing and signal processing (Volder, 1959; Walther, 1971; Hu, 1992). An area efficient solution to CORDIC with application to robotic exploration is proposed and some CORDIC designs have been evaluated on FPGA's by Leena *et al.* (2009), Angarita *et al.* (2005) and Valls *et al.* (2002).

This research considers the CORDIC algorithm to improve the performance of mobile robot. The design of bit parallel unrolled CORDIC circuit can implement in the architecture of Robotic anticipation circuits to improve the speed, reduced propagation delay and power consumption. The core component of CORDIC circuit designed in terms of transistor models for logic operation. The basic CORDIC has components such as multiplexer, full adder and LUT that are designed using by Pass Transistor Logic (PTL). According to circuits analyses, the proposed Mux-Shannon adder based unrolled CORDIC circuit improves performance for area, power dissipation and propagation delay. The analysis can be extending to parameter analysis in terms of speed by BSIM4 analyzer. The existing adder circuits are implementing into CORDIC circuit and then compared to proposed adder based CORDIC circuit. Adder based CORDIC circuit in this research gives better performance than existing adder based CORDIC circuits.

MATERIALS AND METHODS

This research mainly focused on bit parallel unrolled CORDIC circuit which may useful for performance of mobile robot. The direct implementation of CORDIC equations, the vector coordinates to be converted (or) initial values are loaded via multiplexers with an adjacent adder/subtractor. The low arctan LUT is often called an angle accumulator. The registered values are passed through adders/subtractors on each of the clock cycles. They are loaded back to the same component. Each iteration takes one clock cycle, that is in n clock cycles, n iterations are executed and changed coordinates are stored in components. The bit parallel unrolled CORDIC circuit designed components are proposed Mux-Shannon adder, multiplexer and modified LUT that are implemented in PTL. The designed cells such as adder and multiplexer are developed by less number of transistors compared than existing circuits.

Proposed Mux-Shannon adder design: The proposed Mux-Shannon adder in unrolled CORDIC does the computing functions which has the combinational circuit which forms the arithmetic sum of three input bits (Mano, 1979). A, B and C are the three inputs in proposed design and the third input C is carried input to the first stage. The proposed Mux-Shannon adder sum circuit is designed using by pass transistor technique and boolean identities. According to Eq. 1, A⊕B is designed by multiplexing control input techniques. The output of A⊕B is given swing restoration in output node. This node directly connected into C and its compliment for sum circuit. According to pass logic, the swing restoration node is connected to another node, the output node became differential node of obtained input of A⊕B. After connecting C and its compliment, sum output behaving as swing restoration node which gives better results of summing input.

The carry circuit design using by Eq. 2, the sum circuit A⊕B input is directly fed into pass transistor gate input. C is connected as a source input of transistor. The carry circuit is designed according to Shannon based equation (Senthilpari *et al.*, 2008, 2009). The AND logic A and B is derived from pass logic which is implemented into circuit. The circuit according to

boolean identities, the V_{IH} and V_{IL} is minimum which is opposing the output. So the additional circuit supporting AND gate and minimizing the voltage noise margin of the transistors. According to this adder circuit we sacrificed extra two transistors but the output swing, noise margin and switching events are minimized. The complete design of proposed Mux-Shannon adder circuit is shown in Fig. 1.

$$SUM = A \oplus B \oplus C \quad (1)$$

$$CARRY = AB + C(A \oplus B) \quad (2)$$

Modified Lookup Table (LUT) design: The LUT is used to transform the input data into a more desirable output format. LUT's are known as method of implementing an arbitrary binary logic function (Brown *et al*., 1992). Truth table for modified LUT is shown in Table 1. According to Sheikholeslami *et al*. (1998) pass transistors are directly connect to input and output which means the output's are purely performs of dependent input's. This concern is affecting individual input which can feed directly to unrolled CORDIC circuit. LUT circuit in Sheikholeslami *et al*. (1998) is modified for convenient and it can be operate for individual independent output which is shown in Fig. 2. Even though, two transistors are sacrificed in each output, the modified LUT consume lower power and high speed which may useful to mobile robots. LUT used as a logic building block in FPGA uses less area and operates fastly and used in the direct implementation of truth table (Sheikholeslami *et al*., 1998).

LUT based design enhances the processing speed of fuzzy obstacle avoidance controller by reducing the operation time. This work sought to implement a real time mobile robot system that

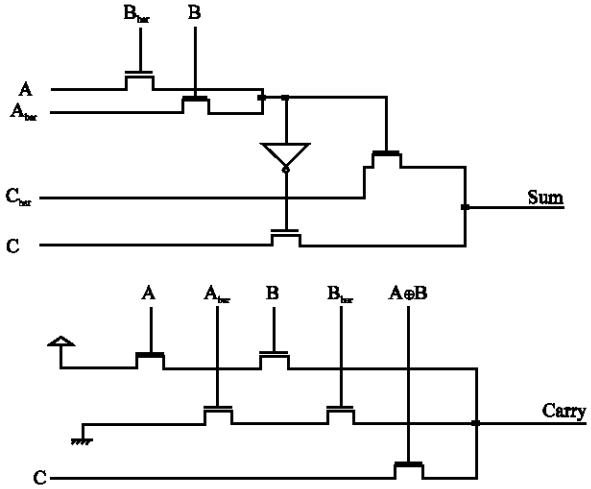

Fig. 1: Proposed Mux-Shannon adder

Table 1: Truth table for Lookup Table

A	B	Selection input	Output
0	0	f_0	f_0'
0	1	f_1	f_1'
1	0	f_2	f_2'
1	1	f_3	f_3'

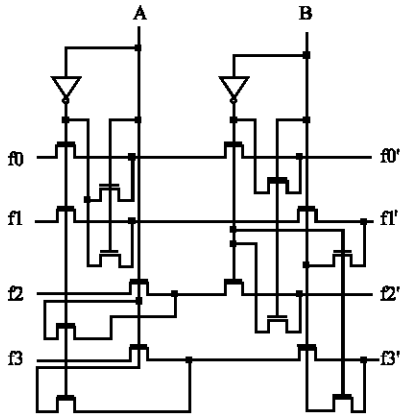

Fig. 2: Modified Lookup Table

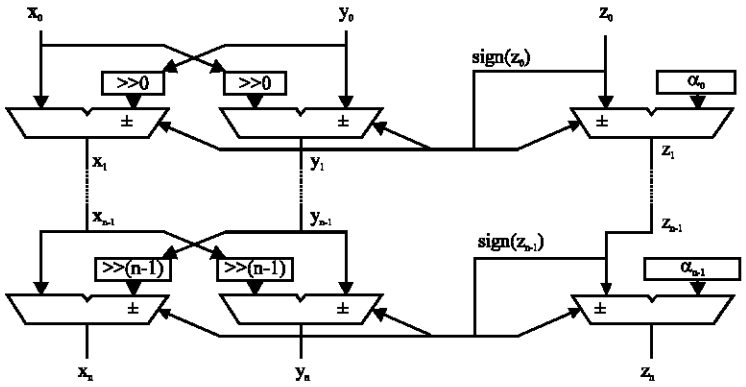

Fig. 3: Architecture of bit parallel unrolled CORDIC

uses relatively less power (Kim *et al.*, 2011). The modified LUT occupies extra two transistors in row output due to the transition of charges. This extra transistors are balancing current flow of input cells. This method gives lower dissipation and high speed due to charge sharing between two transistors, even though number of transistors increased.

Bit parallel unrolled CORDIC: Cascaded iterative CORDIC structure could be used by rebuilding for each iteration instead of buffering the output and using the resources again. Consequently, the input of each stage is output of previous one, as shown in Fig. 3. Wiring the connections between the stages appropriately performs the shift operations. Constant values need not be changed and can also be wired. Multiplexer, full adder, LUT are components used in unrolled CORDIC design which computes one sine value per clock cycle. Input values find their path through the architecture on their own and do not need to be controlled (Kumar and Sappal, 2011).

RESULTS AND DISCUSSION

The bit parallel unrolled CORDIC circuit is designed by proposed Mux-Shannon adder and modified LUT. The modified LUT is main component of unrolled CORDIC circuit which could useful for arctan rotation and compute the number of iterations used in system. The modified LUT circuit

Table 2: Power dissipation, delay, area and number of transistors for LUT

LUT	65 nm	90 nm	130 nm	180 nm
Sheikholeslami *et al.* (1998)				
Power dissipation (μW)	0.326	0.38	0.275	1.77
Propagation delay (psec)	6.4	22.2	7.9	7.9
V_{out} (V)	0.68	0.98	1.18	1.98
Area (μm^2)	96	130	180	713
No. of transistors	12	12	12	12
Modified LUT				
Power dissipation (μW)	0.274	0.107	0.18	1.15
Propagation delay (psec)	4.8	11	3.1	1.6
V_{out} (V)	0.69	0.97	1.19	1.96
Area (μm^2)	210	242	378	1430
No. of transistors	20	20	20	20

compared with LUT in Sheikholeslami *et al.* (1998) in terms of power dissipation, propagation delay, output voltage, area and number transistors is shown in Table 2.

In proposed Mux-Shannon adder based bit parallel unrolled CORDIC circuit to get a rough estimation of propagation delay, Microwind 3 simulation was executed for adder and smaller but often occurring logic gates. The propagation delay for each of these components was used in estimating propagation delay for entire circuit. The worst-case scenario for the delay was found to be one in which all inputs was set to logic low to high (000-111). Maximum delay along the critical path determines the speed of proposed adder based CORDIC circuit. The energy dissipation of CMOS design system is reduced by the developed delay chain techniques. Reduced supply voltage, number of transitions, capacitance and optimized timing signals does the minimization of power. The energy dissipation caused by reduced V_{DD} decreases quadratically, while increasing the delay and degrading the performance. A possible solution can be obtained by using different supply voltages with different inputs in the circuit. Lower voltages are provided to the inputs that are not in the critical path, while higher voltages are provided to the critical ones. The proposed Mux-Shannon adder CORDIC circuit gives lower power dissipation and improved speed than former CORDIC circuits due to normalized channel effect and critical path decreased, that are clearly indicated in Table 3.

Parametric analysis of bit parallel unrolled CORDIC: The bit parallel unrolled CORDIC circuit is analysed by capacitance versus speed. The interconnect parasitic capacitance associated with source or drain of a transistor includes the gate-to-diffusion overlap capacitance, C_{gol}, the diffusion area, perimeter capacitance C_{jb} and C_{jbsw}. The interconnect assign a different capacitance C_{jbswg} to the perimeter along the gate side. The diffusion capacitance is voltage-dependent but as with gate capacitance. The parameter could extract an effective capacitance averaged over the switching transition to use for delay estimation. The capacitance is found, assuming the transistors are wide enough that perimeter perpendicular to the polysilicon gate is negligible fraction of overall capacitance. The total capacitance of shared and merged regions should be split between the two transistors sharing the diffusion node. The maximum frequency is depends upon the rise and fall delay of output transistor parameters. In most of CORDIC circuits, the delay of a single gate is dominated by the output rise and fall time. According to Weste and Eshraghian (1994), the propagational delay is approximately given by:

Table 3: Power dissipation, delay, area and number of transistors for bit parallel unrolled CORDIC

CORDIC cell	65 nm	90 nm	130 nm	180 nm
MCIT 7T Adder CORDIC				
Power dissipation (μW)	1.04	1.882	3.149	13.26
Propagation delay (psec)	23.7	39.6	7.9	23.7
V_{out} (V)	0.68	0.98	1.18	1.98
Area (μm^2)	5543	3819	3667	24598
No. of transistors	249	249	249	249
Mixed Shannon adder CORDIC				
Power dissipation (μW)	1.644	1.914	4.16	19.24
Propagation delay (psec)	31.6	15.9	23.8	19.8
V_{out} (V)	0.67	0.97	1.17	1.96
Area (μm^2)	5796	3910	3757	25300
No. of transistors	268	268	268	268
Shannon Adder CORDIC				
Power dissipation (μW)	0.521	0.789	5.08	10.32
Propagation delay (psec)	8.02	23.8	10.9	31.7
V_{out} (V)	0.67	0.96	1.17	1.97
Area (μm^2)	8487	5833	5605	37583
No. of transistors	316	316	316	316
Proposed adder CORDIC				
Power dissipation (μW)	0.419	0.6889	1.15	9.42
Propagation delay (psec)	7.42	14.2	6.4	18.12
V_{out} (V)	0.69	0.99	1.19	1.99
Area (μm^2)	5439	3888	3519	24255
No. of transistors	256	256	256	256

$$t_{dr} = \frac{t_r}{2} \tag{3}$$

$$t_{df} = \frac{t_f}{2} \tag{4}$$

An alternative formulation is given by:

$$t_{df} = A_N \frac{C_L}{\beta_n} \tag{5}$$

where, A_N is a process constant for a specific supply voltage. A_N has been derived as:

$$A_N = \frac{1}{V_{DD}(1-n)}\left[\frac{2n}{1-n} + \ln\left(\frac{2(1-n)-V_o}{V_o}\right)\right] \tag{6}$$

The process constant is depends upon the CORDIC circuit output voltage (V_o), number of stage and specific voltage of feature size.
Where:

$$n = \frac{V_{tn}}{V_{DD}} \tag{7}$$

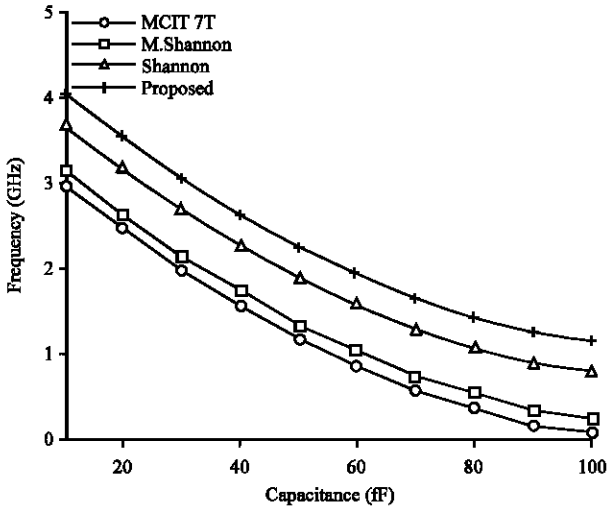

Fig. 4: Capacitance vs. frequency for unrolled CORDIC circuit

$$V_0 = \frac{V_{out}}{V_{DD}} \tag{8}$$

According to Fig. 4, the analysis are done for speed of circuit. This unrolled CORDIC circuit used for finding angle of mobile robot. The proposed adder based unrolled CORDIC circuit gives faster response with varying of interconnect capacitance values. So, this circuit can useful for mobile robot. This circuit giving approximately 4.02 GHz speed which is high speed than the existing mobile robot circuits.

The unrolled CORDIC circuit capacitive coupling can occur on both input and output. According to proposed adder based unrolled CORDIC circuit, the input of dynamic gates have the lowest noise margin. Even though noise margin is low, proposed circuit actively driven by a static gate which fights coupling noise. Coupling is minimized by keeping wires short and increasing the spacing to neighbors or shielding the lines. Coupling can be extremely bad in processes below 250 nm because the wires have such high aspect ratios.

The dynamic leakage current outputs are especially susceptible to noise when they float high, held only by a weak keeper. Dynamic inputs have low noise margins due to less critical path in proposed circuit. The charge leakage in the proposed adder based unrolled CORDIC interconnect circuit having less subthreshold leakage on the dynamic node. In proposed adder based unrolled CORDIC circuit, has low leakage current due to high integrity of node, than other adder based CORDIC circuits. The shrinkage of gate capacitance and gate area of MOSFET is changing charge channel values which increased leakage current because of improper arrangement of transistor tree structure and longer critical path being in circuit. The proposed adder CORDIC circuit has lower leakage current than other CORDIC circuit due to reduce the critical path. The pass logic design basically reduced two transistors per logic that means the channel effect is reduced. The proposed adder based unrolled CORDIC circuit has lower operating current than other CORDIC to trade-off in critical path. The maximum leakage current can be found from PMOS to NMOS aspect ratio (W/L) of CMOS inverter which also affects the performance of CORDIC circuit. The proposed adder based unrolled CORDIC circuit gives less leakage current which is shown in Fig. 5. So, this circuit may used in mobile robot for long duration.

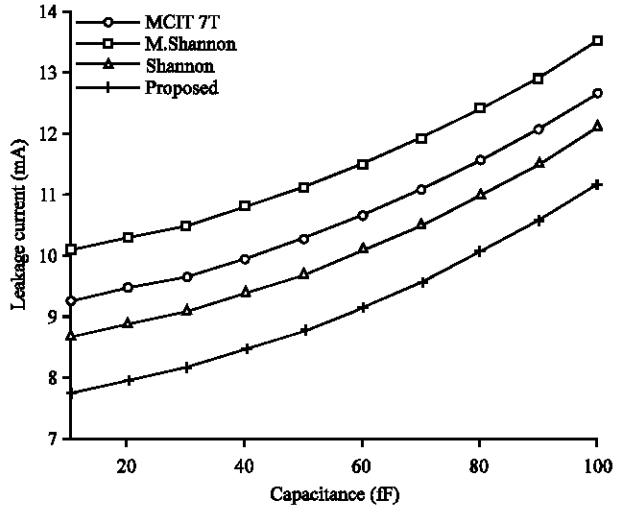

Fig. 5: Capacitance vs. leakage current for unrolled CORDIC circuit

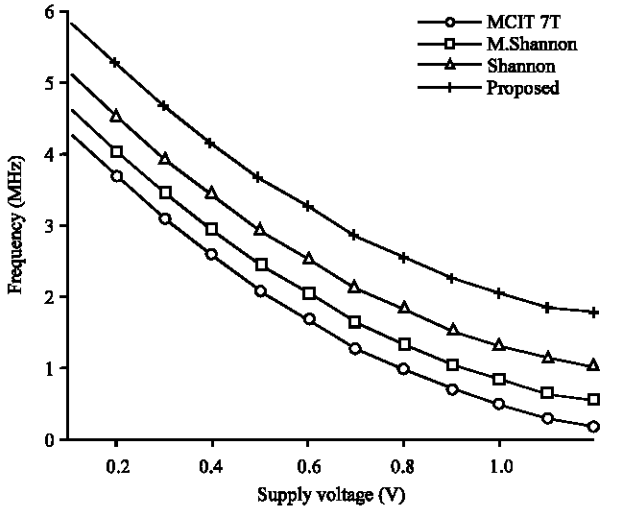

Fig. 6: Supply voltage vs. frequency for unrolled CORDIC circuit

The supply voltage versus frequency is shown in Fig. 6. The dynamic power dissipation of CORDIC circuits is dissipated when the output capacitance is charged/discharged. The dynamic dissipation may calculate using by Eq. 9:

$$P_{dynamic} = \alpha C_L V_{DD}^2 f \quad (9)$$

Where:
α = Switching activity
C_L = Load capacitance which derived from layout analysis
V_{DD} = Supply voltage
f = Operating frequency

According to CORDIC circuits, supply voltage depends upon feature size which is denoting in Table 3. The operating frequency of designed circuits is varied from 0.16 to 5.8 GHz. The

normalized operating frequency is approximately 2.98 GHz. The average number of high to low transition occur in proposed circuit is 0.95 nsec. The dynamic power dissipation is measured according to above mentioned conditions. Since this research mainly focusing on dynamic power, the total power dissipation can be estimated as Eq. 9 and the energy consumption during the time interval [0, T] is given by:

$$E = \int_0^T P(t)dt \propto V_{DD}^2 fT = V_{DD}^2 N_{cycle} \tag{10}$$

where, P(t) is total dynamic power dissipation at t and N_{cycle} is number of clock cycles. These equations designate that a important energy saving which can be attained by reducing the supply voltage V_{DD}; a decrease in the supply voltage by a factor of 2 concedes a decrease in the energy consumption by a factor of 4 (Chen, 2006).

The energy consumption may calculate using Eq. 10. The total dynamic power dissipation measured from CORDIC cell layout output parameters which are derived from output x_n of CORDIC circuit. The total power dissipation depends upon layout channel effect. The proposed adder based unrolled CORDIC circuit gives less power dissipation due to lower channel effect, less critical path and minimized transition time. According to proposed design concept, we have chosen only logic '1' as a source input of all transistors. So the power dissipation would be happened only dynamic. The operating frequency, f is always equal to dynamic power dissipation and reciprocal of square of supply voltage and load capacitance which is shown in Eq. 11:

$$f = \frac{P_D}{C_L V_{DD}^{\ 2}} \tag{11}$$

According to Eq. 11 the supply voltage varied from 0.1 to 1.2 V and speed of CORDIC circuits varied to approximately 5.8 to 0.16 GHz, respectively. The dynamic power dissipation determines according to switching events of transistor which is tabulated in Table 3. The energy gap of load capacitance is depends upon supply voltage which leads to performance degradation. When the scaling technique is Ultra Deep Sub Micron (UDSM) device, the current passing through the terminal is channelized. So the voltage energy saving is satisfied by UDSM. The proposed adder based CORDIC circuit gives higher speed (5.8 to 1.72 GHz) corresponding to 0.1 to 1.2 V, than other reference circuits that are illustrated in Fig. 6. According to Fig. 6, the unrolled CORDIC circuit can used very low supply voltage. So the mobile robot may work long time period due to circuit consuming lower voltage and with high speed.

The supply voltage against dynamic leakage current (mA) of CORDIC circuits is shown in Fig. 7. As the supply voltage increases the maximum operating current of CORDIC circuit also increases irrespective of design technique as shown in Fig. 7. Other important notice is that the proposed Mux-Shannon adder CORDIC circuit show less increase in leakage current compared to other CORDIC circuits. If a voltage is applied to the drain or source, a small leakage current flows into or out of, the device. There are many contributions to the leakage current. One is due to the required bulk connections: pFET bulk is the nWell region which is connected to the power supply V_{DD}. Since the pFET source is a p+ region, this creates a pn junction that admits a small leakage

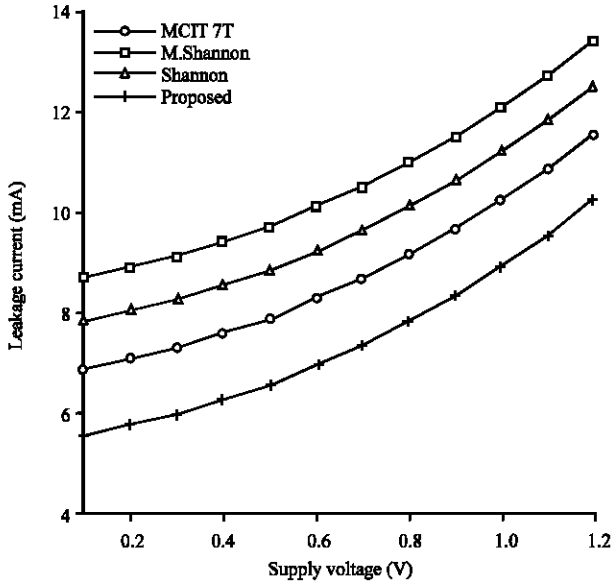

Fig. 7: Supply voltage vs. leakage current for unrolled CORDIC circuit

current i_p flowing on to the node. The nFET has same problem, with in flowing from output to p-substrate. Denoting the current off of parasitic component by i_{out}, we may sum the contributions to obtain:

$$i_{out} = i_n - i_p = -C_{out}\frac{dV}{dt} \tag{12}$$

The effects of the leakage currents, suppose that circuit have an initial voltage $V(t = 0) = V_1$ stored on parasitic component. If $i_n > i_p$, then $i_{out} = I_L$ is a positive number (Uyemura, 2002). According to previous discussion, Eq. 12 may rewrite as:

$$I_L = -C_{out}\frac{dV}{dt} \tag{13}$$

Monte-Carlo simulation can be used to find the effects of random variations on a circuit. It consists of running a simulation repeatedly with different randomly chosen parameter offsets. To use Monte Carlo simulation, the transistor models must include the offset parameters (Weste and Harris, 2005). According to Monte-Carlo simulation method the proposed adder based unrolled CORDIC circuit gives shorter critical path in circuit. Especially, sharing the charge in between input and output (transconductance) of designed full adder cell is regulated. Due to equal charge sharing in the input node and output node is reducing propagation delay which yield the speed of charge carrier. The proposed Mux-Shannon adder based unrolled CORDIC circuit gives faster response than former adder based unrolled CORDIC circuits that are illustrated in Fig. 8.

According to Eq. 12, the current output is always depends upon output voltage derivate of output parasitic component. The output current is always flow through the output parasitic

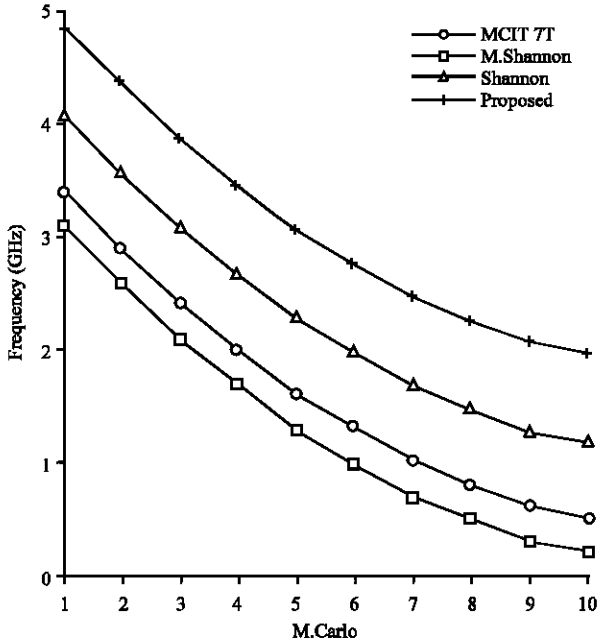

Fig. 8: Monte-Carlo value vs. frequency for unrolled CORDIC circuit

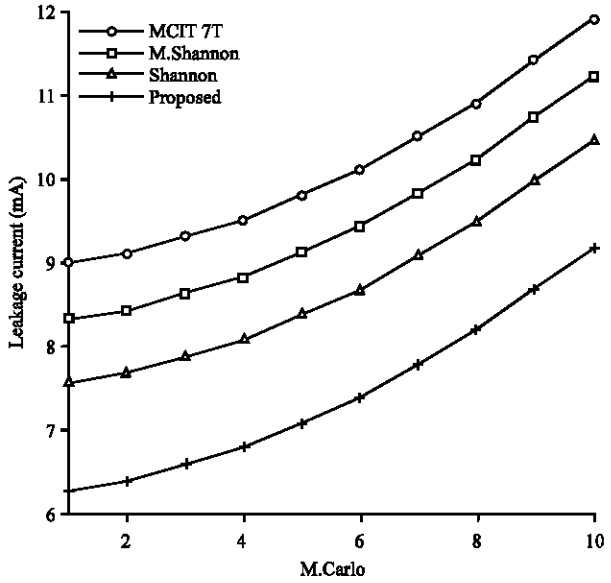

Fig. 9: Monte-Carlo value vs. leakage current for unrolled CORDIC circuit

component value that are depends upon charge and discharge. In proposed adder circuit the connection tree of sum and carry sub threshold nodes are minimized due to equal paths are connected to sum and carry. So proposed Mux-Shannon adder based circuit gives lower leakage than former adder based unrolled CORDIC circuit which is shown in Fig. 9.

CONCLUSIONS

The bit parallel unrolled CORDIC circuits were designed using PTL logic based proposed Mux-Shannon adder, modified LUT and Multiplexer. The proposed Mux-Shannon adder based CORDIC

outperforms than other CORDIC circuits. Shorter critical path and low switching events gives the proposed Mux-Shannon adder based CORDIC cell better performance in terms of area, power characteristics and Propagation delay compared to other CORDIC circuits. The proposed circuit can be applied in mobile robot applications due to its improved speed, low power dissipation and lower delay.

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