Low Voltage Flip-flop Standard Cells with Optimum Energy Delay Product

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Abstract: This study presents transmission gate flip-flop standard cells with channel length and dual-threshold techniques and their low-voltage operating. The proposed transmission gate flip-flops have the same structure with the basic master-slave transmission gate one using multiplexers, but the different place is the feedback path (non-critical path). In the non-critical path, the dual-channel length flip-flop uses high threshold devices while the dual-threshold flip-flop uses gate-length modulation device. Three flip-flop standard cells are investigated from 0.5 to 1.2 V in term of Energy Delay Product (EDP) with HSPICE at a SMIC 130 nm technology. The dual-threshold flip-flop standard cell achieves considerable leakage reductions and gate-length biasing flip-flop standard cell achieves the lowest total energy consumption in all the cells. The results demonstrate that scaling supply voltage using dual-threshold CMOS (low threshold and ultra high threshold) and gate-length biasing are advantageous, especially in low voltage regions (800-900 mv) which yield the best EDP.

Key words: Microelectronics, energy-efficient digital circuit, energy delay product, standard cell

INTRODUCTION

Technology scaling increases the density and performance of integrated circuits resulting in large power dissipations. Low power designs become more and more attractive (Hu et al., 2013).

Supply voltage of near-threshold circuits is between the supply voltage and the transistor threshold voltage (Yu and Hu, 2010). Because the dynamic power is proportional to the square of the supply voltage, near-threshold circuits can effectively reduce the power consumption of the circuits (Hu and Yu, 2012). Therefore, they are suitable for medium performance.

The total energy consumption per cycle \( E_{\text{total}} \) includes two components: Switching energy \( E_{\text{sw}} \) due to charging and discharging for loads and static energy dissipation \( E_{\text{static}} \) that is caused by leakage currents of MOS devices. \( E_{\text{mul}} \) can be expressed as:

\[
E_{\text{mul}} = E_{\text{sw}} + E_{\text{static}} = \alpha C_i V_{DD}^2 + V_{DD}I_{\text{leakage}}T
\]  

where, \( \alpha \) is switching activity, \( C_i \) is the load capacitance, \( V_{DD} \) is source voltage, \( I_{\text{leakage}} \) is average leakage current of MOS transistors through the \( V_{DD} \) and \( T \) is operation cycle, respectively (Yu et al., 2011).

For large source voltages (\( V_{DD} > V_{th} \)), the energy dissipation operating at a maximum frequency is reduced quadratically as the supply voltage scales down. For a low source voltage (\( V_{DD} < V_{th} \)), the energy dissipation operating at a maximum frequency is increased exponentially as supply voltage scales down, because of the exponential relationship between leakage energy dissipation and delay (Markovic et al., 2010).

Performance and energy consumption are equally significant in high-performance and low-power applications. EDP (Energy Delay Product) metric provides a good compromise between delay (\( t_{d} \)) and energy consumption which is written as (Gonzalez et al., 1997; Stan, 1999):

\[
EDP = E_{\text{total}} \cdot t_{d}
\]  

where, \( E_{\text{total}} \) is the total energy consumption per cycle, \( t_{d} \) is the delay of circuits, respectively.

As supply voltage scales down, the energy consumption reduces and the delay increases. Therefore, the minimum EDP can be reached in a low source voltage. In digital chip designs, widely used methods are cell-based design flow with commercial EDA tools (Jayakumar and Khatri, 2007). This study presents low-voltage operating of flip-flop standard cells using dual-threshold CMOS (low threshold and ultra high threshold) and gate-length biasing to reduce leakage power. Three flip-flop standard cells based on transmission gates are investigated from 0.5V to 1.2V in term of EDP. Results show that lowering supply voltage is advantageous, especially in low voltage regions (800-900 mv) at SMIC 130 nm technology which yields the best EDP.

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FLIP-FLOPS

The basic transmission gate flip-flop (DFFQX1_R) is shown in Fig. 1 which is extensively used in sequential circuits, because of its simple structure with reliable performance (Yu et al., 2011). There are a critical path (from D to Q) which determines the maximum speed of the circuit and non-critical path (from n3 and n7 to n2 and from Q and n6 to n4) which holds the value by using feedback.

The channel length biasing technique increases the channel length of transistor to alter the threshold voltage and reduces leakage exponentially. It is reported that small biases in channel length of transistor can afford significant leakage savings with small performance impact (Gupta et al., 2006; Zhang et al., 2011). The transmission gate flip-flop using the dual-channel length (DFFQX1_Lbiasing) is shown in Fig. 2a, where the channel length of the transistors in the feedback path (non-critical path) is increased to reduce leakage dissipation.

Sub-threshold leakage current increases exponentially with the threshold voltage scales down. Dual-threshold CMOS (DTCMOS) is effective technique to achieve low leakage power design (Zhang et al., 2011). The dual-threshold transmission gate flip-flop (DFFQX1_Lh) is shown in Fig. 2b. DFFQX1_Lh utilizes low-threshold voltage (V_TL) devices in the critical path to meet timing constraint and high-threshold voltage (V_TO) transistors in the non-critical path to reduce leakage dissipation.

POST-LAYOUT SIMULATIONS

In order that the layouts of flip flop standard cells can be used for automatic placement and routing tools such as SoC Encounter, their pitch (the min center distance between routing metal) should follow the SMIC 130 nm technology. The METAL2 (vertical route metal) pitch is 0.46μm and the METAL1 (horizontal route metal) pitch is 0.41μm. All the width of the standard cell layout is a multiple of the pitch of METAL2 and all the height of the layout is 3.69μm, also is a multiple of the pitch of METAL1.

The layouts of two flip-flop cells are shown in Fig. 3 and 4. The metal lines are placed horizontally at the top and the bottom of the power supply (VDD) and ground (VSS). Both of the layout areas of the DFFQX1_R and DFFQX1_Lbiasing are 6.9μm×3.69μm while the DFFQX1_Lh standard cell is 8.74×3.69μm.

The energy dissipation and delay of the three flip-flops are compared in Fig. 5 and 6 by using post-layout simulations at a SMIC 130nm technology. The energy delay product of the three flip-flops is shown in Fig. 7 by using post-layout simulations for different
source voltages from 0.5 to 1.2 V. When supply voltage is 1.2 V, the energy delay products of DFFQX1_lbiasing and DFFQX1_lh cells are 57 and 49.12% lower than DFFQX1_R, respectively.

Fig. 6: Propagation delay of three flip-flops cells

Lowering supply voltage is an effective way to achieve low EDP (energy delay product) for the three flip-flops, especially in medium-voltage region (0.8-0.9 V) which yields the best EDP. The optimum supply voltage of the basic flip-flops varies slightly with gate style from Fig. 7.

Fig. 7: Energy delay product of three flip-flops cells

STANDARD CELL DESIGNS

The standard cell design flow is shown in Fig. 8. We use the stream cut function of IC5141 to generate the GDS database that is used to create the auto place and route library. The synthesis library is generated by using the liberty NCX and HSPICE. After the layout design, the abstract based on physical layout and process technology information in library Exchange Format (LEF) is created for standard cells, as shown in Fig. 9 and 10.

The final LEF (Library Exchange Format) tech file for the flip-flop standard-cell is shown in Fig. 11. From the LEF file, we can see that all the PIns are abstracted and the size is 10.58-3.69 µm defined in the LEF file.

For a characterization task, the template file that specifies the SPICE model file name, the SPICE net list directory and the SPICE simulator executable is shown in Fig. 12.
In order to estimate power information, the shift register is synthesized by using Design Compile, as shown in Fig. 13. The area of the shift register is shown in Fig. 14.

![Diagram](image)

**Fig. 8:** Standard cell design flow

![Image](image)

**Fig. 9:** Abstract view of the DFFQX1_Lbiasing flip-flop standard cell

![Image](image)

**Fig. 10:** Abstract view of the DFFQX1_Lh flip-flop standard cell

MACRO DFFQX1_Lbiasing
CLASS CORE
FOREIGN TGMS0 0
ORIGIN 0.0000 0.0000
SIZE 9.0000 BY 3.6900
SYMMETRY X Y
SITE SM13SITE
PIN CK
DIRECTION INPUT
PORT
LAYER METAB
... ...
END
END CK
DIRECTION INPUT
... ...
END
END VSS
END DFFQX1_Lbiasing

**Fig. 11:** LEF tech file of DFFQX1_Lbiasing flip-flop standard cell

```
set input_library ./input_lib/smic13_typical.lib
set output_library ./out_lib/smic13_typical_out.lib
set model_file ./model/model.typ
set netlist_dir ./netlists
set simulator_exec /home/tools/synopsys/hspice_yC-2009.09/hspice/linux/hspice
set templates true
set input_template_dir config
set timing true
set power true
set uldm true
set ulpm true
set precision 6
set farm_type noFarm
set cos_power false
set compact_power false
set cos_timing false
```

**Fig. 12:** Template files of the liberty NCX

| Tab1: Power of two shift register cells by varying supply voltages (μW) |
|---------------------|---|---|---|
| **Vcc**           | 0.9 V | 0.7 V | 0.6 V |
| **DFFQX1_R**      | 13.3853 | 7.979 | 5.071 |
| **DFFQX1_Lbiasing** | 6.9589  | 4.1268 | 2.9139 |
| **DFFQX1_Lh**     | 6.9734  | 4.1472 | 2.9489 |

The shift register cells are analysed by using the DFFQX1_R, DFFQX1_Lbiasing and DFFQX1_Lh flip-flops, respectively. Figure 15 and 16 show the analysis results. The power of the shift register cells is shown in Table 1. The power dissipations of the near-threshold shift registers using flip-flop cells based on DTCMOS and channel length biasing techniques are lower than basic transmission gate one.
Table 1: Information of flip-flop cells used in the shift register design

<table>
<thead>
<tr>
<th>Cell</th>
<th>Reference</th>
<th>Library</th>
<th>Area</th>
<th>Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>DFFQX1_R</td>
<td>typical _1v2c25</td>
<td>25.461000n</td>
<td></td>
</tr>
<tr>
<td>U2</td>
<td>DFFQX1_R</td>
<td>typical _1v2c25</td>
<td>25.461000n</td>
<td></td>
</tr>
<tr>
<td>U3</td>
<td>DFFQX1_R</td>
<td>typical _1v2c25</td>
<td>25.461000n</td>
<td></td>
</tr>
<tr>
<td>U4</td>
<td>DFFQX1_R</td>
<td>typical _1v2c25</td>
<td>25.461000n</td>
<td></td>
</tr>
</tbody>
</table>

Total 4 cells (a) 101.844002

<table>
<thead>
<tr>
<th>Cell</th>
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<th>Area</th>
<th>Attributes</th>
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<tbody>
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<td>DFFQX1_lbiasing</td>
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<td>25.461000n</td>
<td></td>
</tr>
<tr>
<td>U2</td>
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<td>typical _1v2c25</td>
<td>25.461000n</td>
<td></td>
</tr>
<tr>
<td>U3</td>
<td>DFFQX1_lbiasing</td>
<td>typical _1v2c25</td>
<td>25.461000n</td>
<td></td>
</tr>
<tr>
<td>U4</td>
<td>DFFQX1_lbiasing</td>
<td>typical _1v2c25</td>
<td>25.461000n</td>
<td></td>
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</table>

Total 4 cells (b) 101844002

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<th>Area</th>
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</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>DFFQX1_lh</td>
<td>typical _1v2c25</td>
<td>32250599n</td>
<td></td>
</tr>
<tr>
<td>U2</td>
<td>DFFQX1_lh</td>
<td>typical _1v2c25</td>
<td>32250599n</td>
<td></td>
</tr>
<tr>
<td>U3</td>
<td>DFFQX1_lh</td>
<td>typical _1v2c25</td>
<td>32250599n</td>
<td></td>
</tr>
<tr>
<td>U4</td>
<td>DFFQX1_lh</td>
<td>typical _1v2c25</td>
<td>32250599n</td>
<td></td>
</tr>
</tbody>
</table>

Total 4 cells (c) 129.002396

Fig. 14(a-c): Design compile synthesis results of the shift register using the three flip flop cells
Global Operating Voltage = 0.9
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000pF
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, CT unit)
Leakage Power Units = 1pW
Cell Internal Power = 1.31540nW (98%)
Net Switching Power = 229.8103nW (2%)

Total Dynamic Power = 13.3838nW (100%)
Cell Leakage Power = 1.5342nW

Global Operating Voltage = 0.7
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000pF
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, CT unit)
Leakage Power Units = 1pW
Cell Internal Power = 7.8413 nW (98%)
Net Switching Power = 136.4367 nW (2%)

Total Dynamic Power = 7.9780 nW (100%)
Cell Leakage Power = 1.0196 nW

Global Operating Voltage = 0.6
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000pF
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, CT unit)
Leakage Power Units = 1pW
Cell Internal Power = 4.7142 nW (98%)
Net Switching Power = 99.3881 nW (2%)

Total Dynamic Power = 4.8136 nW (100%)
Cell Leakage Power = 257.4428 nW

Fig. 15: Power analysis of the synthesis results of the shift register using the DFFQX1 R cell

Global Operating Voltage = 0.9
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000pF
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, CT unit)
Leakage Power Units = 1pW
Cell Internal Power = 6.9539 nW (98%)
Net Switching Power = 162.4877 nW (2%)

Total Dynamic Power = 6.9539 nW (100%)
Cell Leakage Power = 1.5205 nW

Global Operating Voltage = 0.7
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000pF
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, CT unit)
Leakage Power Units = 1pW
Cell Internal Power = 4.1268 nW (99%)
Net Switching Power = 96.4256 nW (2%)

Total Dynamic Power = 4.1268 nW (100%)
Cell Leakage Power = 1.0143 nW

Global Operating Voltage = 0.6
Power-specific unit information:
Voltage Units = 1V
Capacitance Units = 1.000000pF
Time Units = 1ns
Dynamic Power Units = 1mW (derived from V, CT unit)
Leakage Power Units = 1pW
Cell Internal Power = 2.8437 nW (98%)
Net Switching Power = 76.1871 nW (2%)

Total Dynamic Power = 2.9139 nW (100%)
Cell Leakage Power = 195.2974 nW

Fig. 16(a-c): Power analysis of the synthesis results of the shift register using the DFFQX1_l biasing cell

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As shown in Table 1, when supply voltage is 0.9 V, compared with the basic transmission gate cell, the power dissipations of the near-threshold shift registers using flip-flop cells based on DTCMOS and channel length biasing techniques provides a reduction of 48% and 47.89%, respectively.

CONCLUSION

Near-threshold circuits can effectively reduce the power consumption of the circuits. The low-voltage operating of the flip-flop standard cells using dual-threshold CMOS (low threshold and ultra high threshold) and gate-length biasing have been investigated from 0.5 to 1.2V in term of EDP with a SMIC 130 nm process in this study. The flip-flops based on DTCMOS and gate-length biasing techniques show low leakage energy consumptions and gate-length biasing flip-flop standard cell is one of the lowest total energy consumption in the three flip-flop standard cells. The simulation results demonstrate that lowering supply voltage is an effective way to achieve low EDP, especially in low-voltage regions (0.8V-0.9V) which yield the best EDP. These circuits could be suitable for medium performance module.

ACKNOWLEDGMENTS

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