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A High-performance Implementation of OFDM-MIMO Base-band in Wireless Video System

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Abstract: Orthogonal Frequency Division Multiplexing (OFDM) and Multiple Input Multiple Output (MIMO) become the key technology of next-generation wireless communication system. In order to support wireless transmission of real-time high-definition video, an OFDM-MIMO system is designed. In this study, a high-performance implementation of OFDM-MIMO base-band system is proposed. It is designed and optimized by pipeline architecture of binary tree, state machine decomposition, bit-level algorithm and simplified Advanced Extensible Interface (AXI). Testing results show that the base-band system supports up to 221.776 Mbps data rate and 283.046 MHz clock frequency and it only costs a small part of the FPGA resources. This means that there is still plenty of space to support the implementation of more sophisticated anti-jamming algorithm. The proposed OFDM-MIMO base-band system can be applied to a variety of scenarios of high-speed data transmission.

Key words: OFDM, MIMO, base-band, FPGA, implementation

INTRODUCTION

Era of big data is on the way, people are eager to enjoy high-speed wireless access services at all times and places. In this context, OFDM-MIMO system has been widely used. OFDM system can effectively resist the multi-path fading in wireless high-speed movement and enhance the reliability of data transmission (Yaacoub and Dawy, 2012). MIMO system improves data transmission efficiency greatly through the multi-antenna array. The OFDM-MIMO base-band system is responsible for the achievement of wireless anti-jamming algorithm which requires a lot of real-time digital signal processing. Moreover, it not only requires high data processing efficiency and minimizes consumption of resources, but must have good scalability to support further developments for more specific functions. Virtex®-6 FPGA (Jin *et al*., 2012; Hieu *et al*., 2013) has a large number of programmable logic resources. Besides, with the rapid development of System-on-a-Programmable-Chip (SOPC) technology, Virtex®-6 FPGA integrates multiple processors, it can support real-time digital signal processing and high-layer protocol development.

3 GPP Long Term Evolution (LTE) (E-UTRA, 2010a, b, c; Ketonen *et al*., 2010; Sarker and Lee, 2012) and its enhancement has become the main candidate of 4G standards. It can support 150 Mbps downlink data rate and 50 Mbps uplink data rate in wireless environment. Some researcher has focus on the implementation of link protocol of OFDM-MIMO system, for example, in Qian *et al*. (2013), an OFDM-MIMO user terminal link-layer protocol stack is software implemented. However, the hardware implementation of OFDM-MIMO base-band does not obtained much attention. In this study, a high-performance design of OFDM-MIMO base-band system is proposed by referring to the LTE physical layer protocol.

For enhancing the performance of base-band system, this study proposes several ideas of efficient modeling and optimized algorithms. Firstly, pipeline architecture of binary tree maximizes the efficiency of parallel processing; secondly, state machine decomposition enhances the performance of system clock; thirdly, bit-level algorithm reduce the resource consumption without losing performance; finally, simplified AXI-stream interface makes OFDM-MIMO base-band system to keep very good compatibility with more functional modules.

AN OVERVIEW OF OFDM-MIMO BASE-BAND AND TECHNICAL CHALLENGES

As shown in Fig. 1, in order to adapt MIMO antenna configuration, the two-layer architecture is selected for the base-band system. Each layer contains a common transceiver link; specific parameters are configured through the register, such as the distribution of the pilot signal. In the future, the base-band system can be easily extended to the 4×4 antenna configuration.

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The base-band system also includes scrambler, QAM, synchronization and channel estimator. The scrambler randomizes the bit data to enhance the anti-jamming capability; QAM modulator maps bit to IQ data; Synchronization detects and recovers frame structures from RF antenna; Channel estimator use channel parameters to compensate for the multi-path fading in wireless high-speed movement.

General frame structure is described in Fig. 2; Physical resources consist of sync signal, pilot signal, control data and shared data. Synchronization signal is used to establish data transmission link quickly; discrete pilot structure is designed to estimate parameters of fast fading channels; control data is used to broadcast the system configuration information; all the remaining physical resources is allocated to the shared channel for the maximum data rate, it can also be developed to implement more specific functions. Besides, the main challenges in the implementation of the base-band system are analyzed as follows.

Data processing efficiency: To support high-speed data transmission in wireless environment, the base-band system requires a lot of real-time data processing. When the bidirectional bandwidth reaches 10 MHz, the base-band system must complete two million bits of data processing in 1 msec. In addition, the base-band system must support the algorithm implementation of synchronization, channel estimation, resource scheduling, MIMO merging and so on which means that in resource-limited circumstances, the base-band system need to complete a large number of complex multiplication in a short time. Thus, the base-band architecture should be carefully designed to provide high data processing capability with limited hardware resource consumption in Virtex®-6 FPGA.

Clock performance: Another major concern is the clock performance of base-band system; it is the keyfactor of parallel processing in FPGA, on thepremiseof resource consumption unchanged. The clock performance mainly depends onthe longest delay path of logic. Too long logic path delay will cause the sharp decline of highest clock frequency. Hardware resources are not fully utilized.

Resource consumption: The chip trends to be a high degree of integration. More and more functions need to be integrated in one chip, for example, the chip needs to integrate multiple processors to support the operating system running. In addition, according to the different demand, the chip needs to remain enough space to develop specific module. This requires strict control of FPGA resources consumption, especially BRAM, FIFO, DSP48E and other hard-core resources. When the hard-core resources are used up, ISE will consume generic LUT resources to replace them which means, more and more FPGA resources will be occupied. What is worse, the programmable file of base-band system can't be generated successfully. Therefore, we must design a more optimal algorithm to cost FPGA hard-core resources as less as possible.

Scalability: In order to integrate more functional modules, we must consider the compatibility of base-band system to avoid unnecessary subsequent re-development. Learn from the developmental model of Linux, the base-band system requires better compatibility, to integrate more

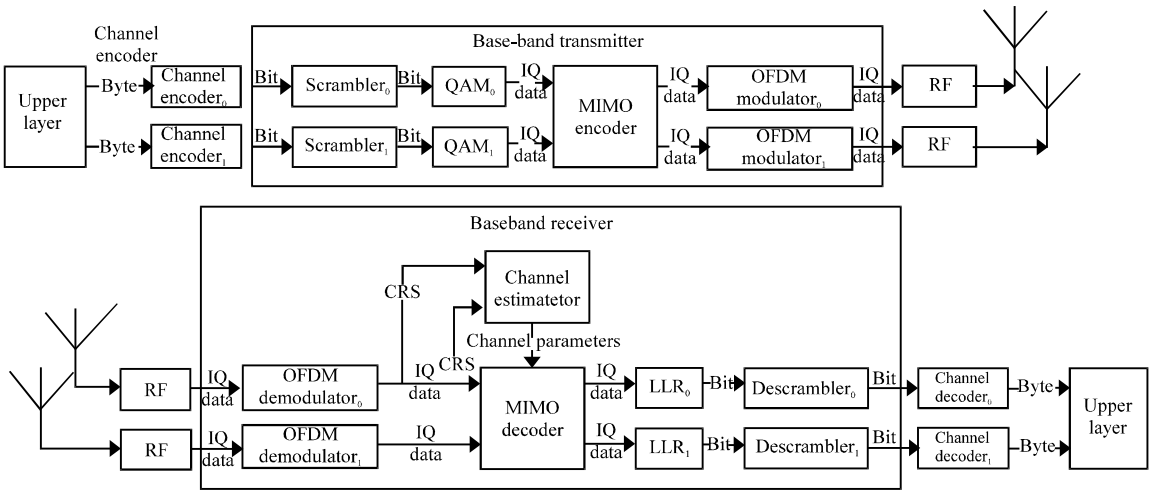

Fig. 1: An overview of OFDM-MIMO base-band system

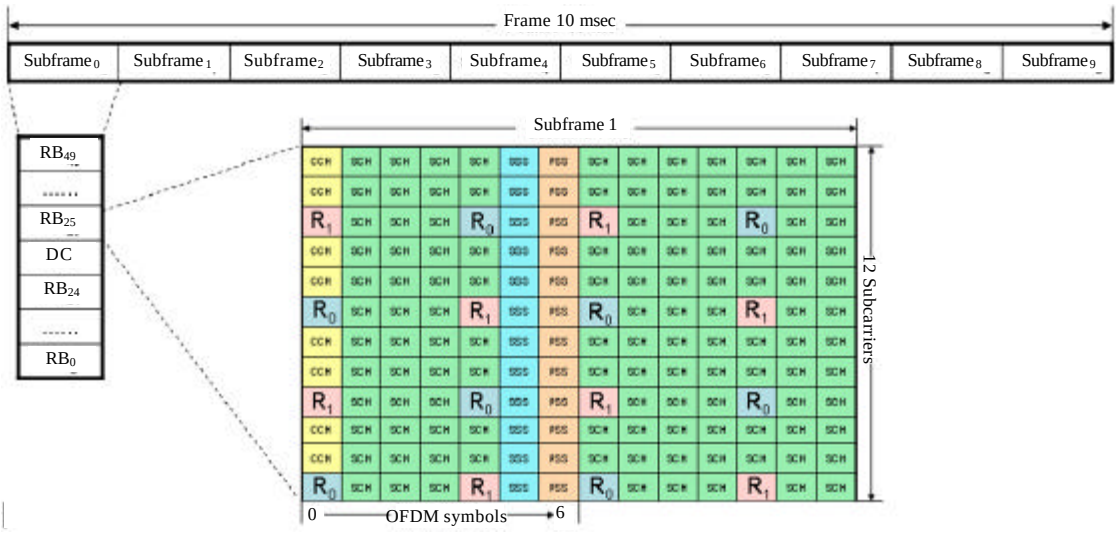

Fig. 2: General frame structure for OFDM-MIMO base-band system

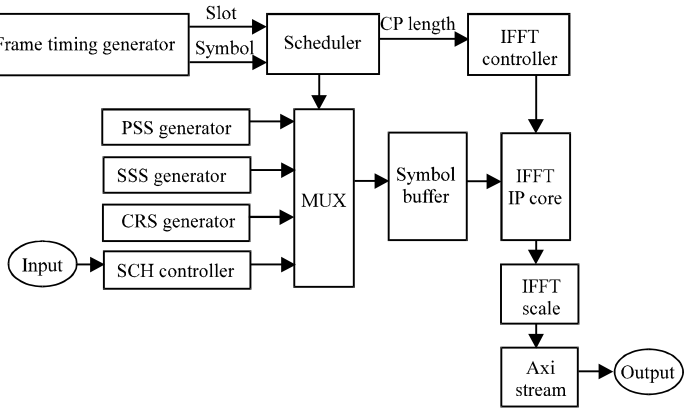

Fig. 3: Proposed architecture of OFDM system

high-performance modules developed by more and more talented programmer. Only in this way can base-band system have a broader space for development.

PROPOSED OFDM-MIMO BASE-BAND SYSTEM

OFDM system: In the proposed OFDM system, the physical resource scheduler starts to work after it receives an OFDM symbol, therefore the shared data can be scheduled in advance without waiting for the completion of receiving an entire sub-frame. When the bandwidth reaches 10 MHz, only 4 KB RAM resources are allocated to buffer an OFDM symbol. Meanwhile, 56 KB RAM resources have to be taken if we try to save the whole sub-frame. This not only saves memory spaces, but also effectively improves the data processing efficiency. As shown in Fig. 3, PSS generator, SSS generator, CRS generator and SCH controller are implemented by independent process. Each of them produce data and corresponding address and then write to the RAM in consecutive clock cycles. The proposed scheme of resource scheduling is described in Fig. 4. According to the index of current OFDM symbol and the slot, the scheduler decides modules that have the authority to operate the RAM through the shared bus. When the clockfrequency goes to 100 MHz, each OFDM symbol must be processed completely in 7142 clock cycles; IP core requires 2155 clock cycles to accomplish a 1024-point IFFT operation. An OFDM symbol is scheduled in 600 clock cycles. There are still approximately 4387 idle clock

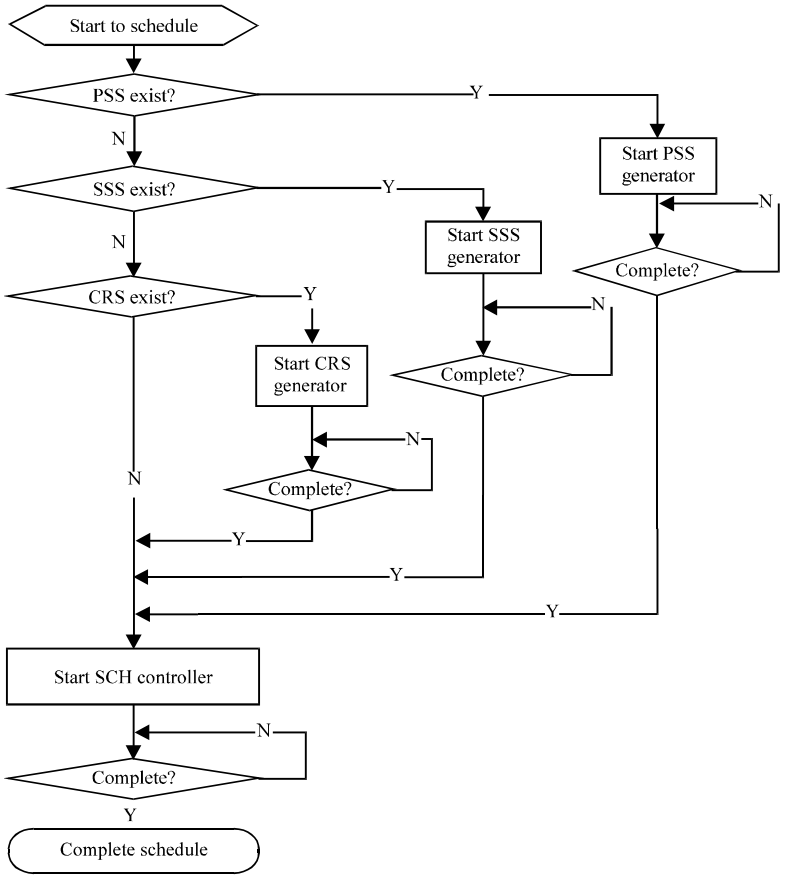

Fig. 4: Proposed scheme of resource scheduling

cycles. There will be more idle clock cycles if the clock frequency rises to 200 MHz. Therefore, OFDM module not only has ability to finish the basic data processing, but also has adequate capacity to achieve more complicated algorithms and protocols.

MIMO system: MIMO system supports two modes of space multiplexing and transmits diversity. The space multiplexing is introduced to increase the data rate and transmit diversity is to enhance the anti-jamming performance. In MIMO system, expansion of 4×4, 8×8 and more antenna configuration should be taken into account. And with the increasing number of antenna, more and more real-time complex multiply and accumulate operations are inevitable. In addition, the multi-stage pipeline structure will lead to large processing delay which will lead to more consumption of RAM resources. As shown in Fig. 5, SFBC decoder is a part of MIMO system, its pipeline architecture is designed by using the idea of binary tree. The decoding algorithm is split into smaller multiply operation. Then merge the result by add operation (or subtract operation). This process is repeated until the constellation points are calculated completely. When multiply and accumulate operations need to repeat N times, the clock cycles of pipeline delay is:

$$\frac{\log_2 N}{2} + 2$$

Test results show that, the maximum data rate of MIMO decoding engine reaches 1.2 Gbps and the pipeline processing delay is only 6 clock cycles. Besides, only total 40 DSP48E1s are consumed.

IMPLEMENTATION AND OPTIMIZATION METHODS

Aiming to solve the technical challenges stated in an OFDM-MIMO base-band overview, special schemes are proposed and implemented. First of all, pipelined architecture of binary tree and bit-level operations are proposed to improve the data processing efficiency and reduce the hardware resource consumption. Secondly, state machine decomposition is introduced to improve the

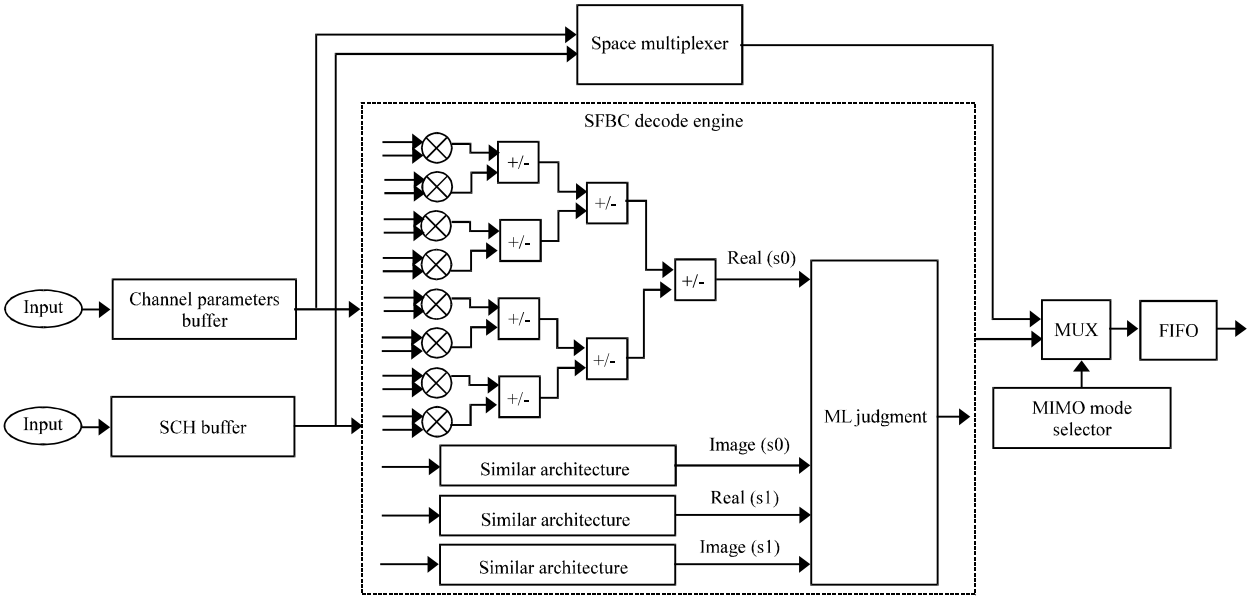

Fig. 5: Proposed MIMO decoding architecture

performance of system clock. Finally, AXI-stream interface is employed to keep good compatibility between OFDM-MIMO base-band system and other module which well be developed in the future.

Pipelined architecture of binary tree: Pipelined architecture of binary tree can take full advantage of parallel processing and effectively improve the data processing efficiency. Firstly, in order to shorten the processing delay, pipeline stages need to be selected appropriately. Secondly, each pipeline stage should avoid too heavy tasks of data processing. Finally, additional memory resources consumption is also necessary to be minimized. Such as the MIMO decoding architecture described in proposed OFDM-MIMO base-band system, the pipelined processing architecture of binary tree is designed by using the idea of partition and merger, has the shortest processing delay. Algorithm is split into minimum operations and then repeats merger until getting the correct results.

State machine decomposition: State machine decomposition is proposed to optimize the performance of system clock. For shortening the longest logic delay path, a large control system is split into smaller parts appropriately; each one is implemented by independent state machine. The smaller state machine is controlled by bigger one which only responsible for sending signals of starting and aborting without accessing internal semaphore. The sub-state machine can also be divided into smaller ones. It is more appropriate that each minimum state machine owns 6-10 states. The system achieves very high performance when its state machines are controlled by red-black tree architecture. The entire control system is composedof a plurality of parallel processing state machine; they share the signal and running state of entire base-band system. State machine decomposition is an effective way to shorten the longest logic delay and raise the maximum frequency. For example, physical resource scheduler of OFDM system is achieved by state machine decomposition, its maximum frequency can reach 319.693 MHz, while the reference frequency of ML605 platform is only 200 MHz.

Bit-level algorithm: Bit-level algorithm is applied to save resources. For example, Maximum Likelihood (ML) decision algorithm has the best BER performance, but it can not be implemented because of excessive resources consumption. Thetraditional MLdecision,usuallyneed to calculate the Euclidean distance between theIQ dataand all standard points in constellation and then select the point which has the shortest Euclidean distance as the result of judgment, finally bits are recovered based on the constellation. A pipelined processing architecture of QPSK ML decision costs more than 8 multipliers, 12 adders.

Bit-level algorithm is designed by using the idea of partition, each bit data is calculated separately. As shown

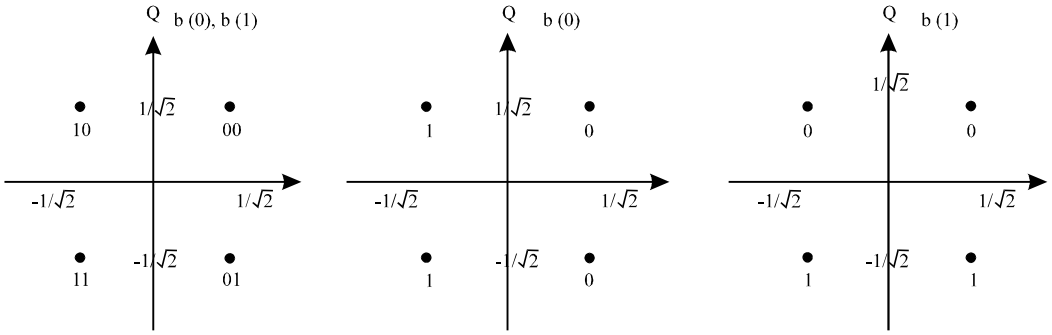

Fig. 6: QPSK constellation

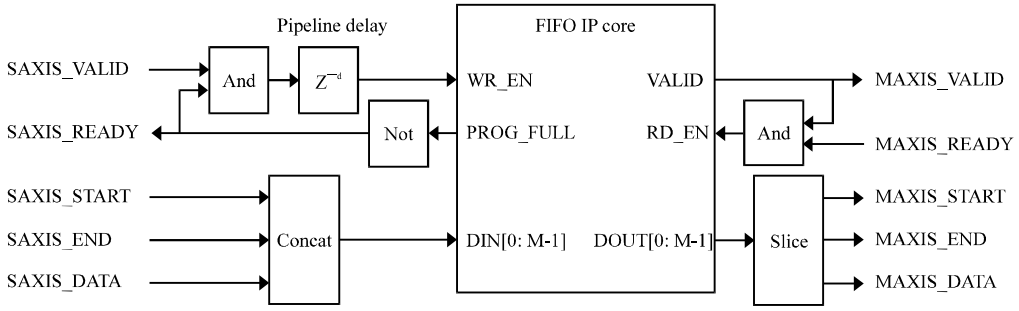

Fig. 7: General architecture of simplified AXIS-stream

in Fig. 6, b (0) can be regarded as 0 when real part of the constellations is greater than 0 or 1 in another case, the same as b (1). In FPGA, the real and imaginary part are independent of each other, determining whether a real number is greater than 0, only need to extract its sign bit. Bit-level algorithm not only remains the performance of ML decision, it even does not need multiply operation. When using high-order modulation, the advantages of bit-level algorithm is more obvious. For instance, a pipelined processing architecture of 64QAM ML decision requires more then 128 multipliers, 64 adders; meanwhile, the same processing architecture of bit-level algorithm only consumes 6 adders.

Simplified AXI-stream: The interface of OFDM-MIMO base-band system is implemented by simplified AXI-stream which can keep good compatibility with more modules developed in the future. In AXI-stream, data exchange occurs only when both master and slave module are ready, data in processing can always be saved in a node of AXI link. General architecture of AXIS-Stream is shown in Fig. 7. PROG_FULL signal indicates whether the FIFO has enough space and determines when to stop the FIFO writing operation. To avoid data loss, when the pipeline processing delay is too long, a larger FIFO space has to be configured, to buffer the processing data when the base-band system is busy. SAXIS_START and SAXIS_END signal indicates the head and tail of the code block. The width of SAIXS_DATA can be adjusted according to specific application. AXI-Stream can be well adapted to high-speed data transmission; other module which follows the AXI-Stream protocol can be well integrated into the OFDM-MIMO base-band system.

PERFORMANCE EVALUATION

To verify the proposed base-band design and evaluate the performance, a prototype is developed and tested in laboratory environment.

System setup: The testing environment for OFDM-MIMO base-band system is built in ML605 platform. The parameters of OFDM-MIMO base-band system are described in Table 1. The testing system is shown in Fig. 8; Channel emulator is added between the base-band transceiver links. Large amounts of random data generated by the PC1 are inputted to the base-band system. Real-time running status of the base-band system and measure result of the maximum data processing rate are monitored in PC2. System clock performance and resource consumption are gotten after finishing the ISE synthesizes process.

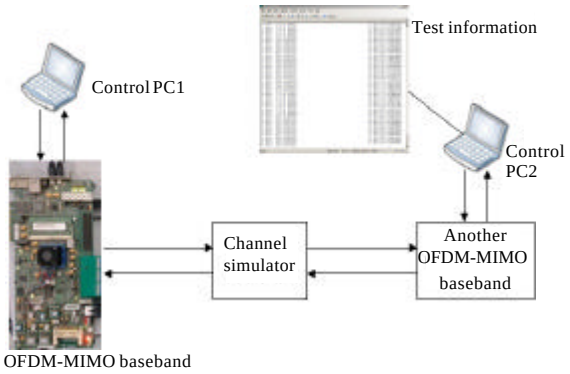

Fig. 8: Testing platform of OFMD-MIMO base-band system

Table 1: System configurations

System clock frequency	100 MHz
System bandwidth	10 MHz
IFFT transform points	1024
No. of subcarriers	600
No. of RB	50
MIMO config	2×2
Modulation type	BPSK, QPSK, 16QAM, 64QAM

Table 2: Resource consumption

Logic utilization	Used	Available	Utilization (%)
No. of slice registers	34314	301440	11
No. of slice LUTs	30155	150720	20
No. of fully used LUT-FF pairs	23340	41129	56
No. of bonded IOBs	72	600	12
No. of block RAM/FIFO	135	416	32
No. of BUFG/BUFGCTRLs	3	32	9
No. of DSP48E1s	148	768	19

In OFDM-MIMO base-band system, the modulation order mainly determines the data rate, the maximum data rate when system using different modulation orders is measured and then compared with the LTE physical layer in both uplink and downlink (E-UTRA, 2010a).

Results analysis: Comparison of data rate between the proposed OFDM-MIMO base-band system and LTE physical layer is shown in Fig. 9. In base-band system, there is not fully linear relationship between data rate and modulation order, because not all the modules are ready for data transmission in a moment. If slave module is unable to receive new data, the data which have been completely processed, must be saved in master module; data transmission has to be paused temporarily in partial module. Testing results show that, the maximum data rate of OFDM-MIMO base-band system can reach 221.776 Mbps when its clock frequency is 100 MHz.

The results of ISE synthesis process show that, the maximum frequency of OFDM-MIMO base-band system can reach 283.046 MHz. Meanwhile, reference frequency of ML 605 platform is only 200 MHz. OFDM-MIMO base-band system has the capacity to run accurately when clock frequency raise to 200 MHz. High clock performances is help to maximize data processing efficiency. As shown in Table 2, only 19% of DSP48E1, 32% Block RAM/FIFO and 20% Slice LUT of Virtex®-6 FPGA are used up. There is enough space for the Virtex®-6 FPGA to achieve further development.

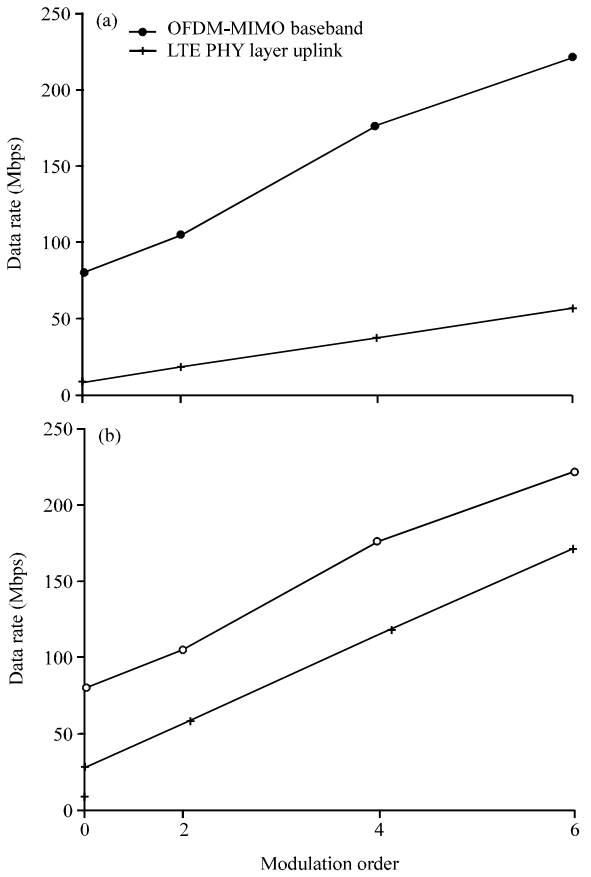

Fig. 9: Data rate of the base-band system

CONCLUSION

This study proposes a high-performance implementation of OFDM-MIMO base-band system. It is achieved and optimized by the methods of binary tree pipeline, state machine decomposition, bit-level algorithm and AXI-stream. Moreover, it supports up to 221.776 Mbps data rate and 283.046 MHz clock frequency. In addition, the Virtex®-6 FPGA still has plenty of space to support more wireless algorithms and the development of specific functions. Therefore, the OFDM-MIMO base-band system can be applied to a variety of scenarios such as wireless transmission of real-time high-definition video and has commercial value.

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