A New Leakage Power Reduction Technique for CMOS VLSI Circuits

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ABSTRACT

A robust method which is equally effectual for static power control in CMOS VLSI circuits for System on Chip (SoC) applications in deep submicron technologies is proposed. Referring to the International Technology Roadmap for Semiconductors (ITRS), the total power dissipation may be significantly contributed by leakage power dissipation. To reduce leakage the proposed method introduces two self controlled stacked leakage control transistors (LT) between $V_{dd}$ and ground, which offers high resistance, when it is in off state. The gate and substrate of each LT’s are tied together to introduce Dynamic Threshold voltage MOSFET (DTMOS). This proposed method is intuitively momentous and leads to better performance measure in terms of dynamic power, leakage power propagation delay and Power Delay Product (PDP) with standard threshold devices. The experiment and simulation results show that the proposed method effectively outperforms than the base case with little area overhead.

Key words: Leakage power, subthreshold, CMOS, dynamic power, threshold voltage

INTRODUCTION

Not so long ago, research had been focused on developing portable applications which favor high performance, thus increasing system complexity. Natural fallout of this process has been shortened battery life and long term reliability issues. Analysis of such systems points to increased power consumption as the main factor (Rabaey and Pedram, 1996) also causes tunneling effects. These realizations spurred interest in the area of low power design thus creating a new field of electronics. Thus, along with area and speed, power consumption is an important criterion in measuring system performance.

The quadratic nature of dynamic power consumption on the supply voltage $V_{dd}$ implies that lowering $V_{dd}$ leads to significant power savings and scaling $V_{dd}$ results in drastic reduction of device speed. To combat this, threshold voltage $V_{th}$ has to be reduced. To ensure optimum performance of circuits, it is essential that the ratio of $V_{dd}$ to $V_{th}$ is around 4-5 (Rabaey and Pedram, 1996). The maintenance of this ratio avoids hot carrier effects and leads to better noise margins. Scaling $V_{th}$ leads to an increase in the subthreshold leakage current exponentially. Thus, there is an inevitable trade-off between leakage current and power supply for an application. Various schemes have been tried to neutralize the effect of lowering supply and threshold voltages. The sub-threshold leakage $I_{SUB}$ is given as Eq. 1:
\[ I_{MB} = I_e \frac{V_{gs} - V_a - \eta V_{a} - \gamma V_a (1-e^{-\frac{V_{gs}}{V_a}})}{nV_a} \]  

\[ I_s = \mu C_{ox} \left( \frac{W}{L} \right) V_{gs}^2 e^{\frac{V_{gs}}{V_a}} \]  

where, \( C_{ox} \) represents the gate oxide capacitance, \( \mu \) denotes carrier mobility, \( W \) denote the width and \( L \) denote the length of the transistor, \( V_T = kT/q \) is the thermal voltage, \( n \) is the slope shape factor sub-threshold swing, \( \eta \) denotes the DIBL (Drain Induced Barrier Lowering) coefficient and \( \gamma \) is body effect coefficient. The leakage reduction techniques are broadly classified based on the mechanism for leakage reduction, mode of operation (Fallah and Pedram, 2005) and abstraction level of the design (Elgharibawy and Bayoumi, 2005), where the technique is applied.

In this work, we present a circuit level design technique that reduces the overall leakage power in conventional CMOS cells. The focus of this study is on static power dissipation using self controlled stack transistors in DTMOS fashion.

**REVIEW OF DTMOS**

The DTMOS is formed when the gate and body of a MOSFET is tied together as shown in Fig. 1. Because of the body effect, the threshold voltage of MOSFETs can be changed dynamically during modes of operation. When the device is OFF, the leakage is low and the leakage is high when the device is ON. When \( V_{gs} = 0 \), the threshold voltage \( V_{th} \) is high resulting in low leakage current (Assaderaghi et al., 1994, 1997). However, the current drive is high when the gate voltage is raised for low \( V_{DD} \) values. The threshold voltage \( V_{th} \) increases when the body (substrate) to source reverse bias \( V_{BB} \) is made bigger. By connecting the gate to the body, a forward bias is achieved between body to source compelling the threshold voltage \( V_{th} \) to drop resulting in high performance. This lower threshold voltage of DTMOS does not increase the off-state leakage. The DTMOS and a regular device have the matching threshold voltage when \( V_{g} = V_{gs} = 0 \).

**PROPOSED METHOD**

The proposed method employs 2 self controlled stacked Leakage control Transistors (LTs) for every CMOS gate in the path \( V_{DD} \) to ground. This method is based on the examination that stacking

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Fig. 1: SOI NMOSFET with substrate and gate tied together
of transistors result in low leakage as the resistance offered by the OFF transistors is very high (Hanchate and Ranganathan, 2004; Narendra et al., 2001; Sirichotiyakul et al., 2002). The gate of each LT is driven by the source of the other LT which ensures that one of the LT is always near its cutoff, offering high resistance in the path $V_{dd}$ to ground. However, a significant delay is encountered due to the two additional Leakage control Transistors (LTs) connected in series in the output path. The LTs are required to be sized accordingly to keep the delay minimum in LECTOR (Hanchate and Ranganathan, 2004). The LTs are modified to operate as DTMOS when the floating body and gate of the respective LTs are tied together which eliminates the need for sizing of LTs. The gate and body of the LTs are held at the same potential in the proposed method as shown in case of a general CMOS gate in Fig. 2. The additional delay introduced due to the leakage control transistors is reduced as the threshold voltage is modified dynamically during different modes of operation (active and standby) by DTMOS as given by the Eq. 3:

$$\text{Delay} \propto \frac{V_{th}}{V_{dd} - V_{th}}$$

(3)

Hence, the Leakage control Transistors (LTs) modified in to DTMOS offers very less leakage and reduced delay without the need for transistor sizing. Figure 3 shows a 2-input NAND circuit implemented with the proposed method. The LTs and other logic gate devices are standard $V_{th}$
Fig. 3: Two input NAND gate with proposed method

devices. The DC characteristics for a basic 2-input NAND circuit (Fig. 4a) and proposed 2-input NAND circuit (Fig. 4b) using HSPICE is shown in Fig. 4(a-b), with input A fixed in 1 volt and input B varied from 0-1 volt. The exact output logic level is maintained in the proposed method without any degradation of the voltage levels. The input-output logic for the proposed NAND circuit is shown in Fig. 4c. The ON-OFF state of the transistors for every input vectors of proposed NAND circuit is shown in Table 1.

RESULTS

In order to compare the results of the proposed method with the base case and LECTOR, the experiment was carried out with a CMOS 2-input NAND gate. Schematics are designed for all the mentioned methods using Custom Designer in Synopsys for TSMC 0.18 μm technology. Netlists obtained from the schematics are used for HSPICE simulation and performance testing. The original net lists are modified according to the process technology requirement using the TSMC 0.18 μm device process technology and BPTM (Berkeley Predictive Technology Model) 0.09 μm process. The modified net lists are simulated using Synopsys HSPICE for power and delay estimations.

The worst case power and delay measurements are made in all the cases. The leakage power for all the input vectors, average dynamic power dissipation with delay and the PDP are given in Table 2 for 90 nm process technology. Table 2 shows that the proposed method has more leakage savings, reduced dynamic power and optimum PDP than the base case and LECTOR.
Fig. 4(a-c): DC characteristics for (a) Basic and (b) Proposed 2-input NAND gate and (c) Input-output Logic for Proposed NAND gate

### Table 1: State Table of Proposed 2-Input NAND gate for 90 nm Process Technology

<table>
<thead>
<tr>
<th>Transistor label</th>
<th>Input vector (A,B)</th>
<th>(0,0)</th>
<th>(0,1)</th>
<th>(1,0)</th>
<th>(1,1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>M2</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>LT1</td>
<td>Near cut-off</td>
<td>Near cut-off</td>
<td>Near cut-off</td>
<td>On</td>
<td></td>
</tr>
<tr>
<td>LT2</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Near cut-off</td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td>M4</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>On</td>
</tr>
</tbody>
</table>
Table 2: Power, delay and PDP for 2-input NAND gate, 90 nm process technology, supply voltage = 1 volt

<table>
<thead>
<tr>
<th>NAND gate type</th>
<th>(0,0)</th>
<th>(0,1)</th>
<th>(1,0)</th>
<th>(1,1)</th>
<th>Average leakage power (W)</th>
<th>Average dynamic power (W)</th>
<th>Delay (ps)</th>
<th>PDP_{dynamic} (J)</th>
<th>PDP_{static} (J)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td>4.7335</td>
<td>4.1155</td>
<td>3.2091</td>
<td>1.0979</td>
<td>1.3707</td>
<td>5.7733</td>
<td>11.67</td>
<td>16</td>
<td>67.37</td>
</tr>
<tr>
<td>CMOS NAND</td>
<td>E-09</td>
<td>E-10</td>
<td>E-10</td>
<td>E-11</td>
<td>E-09</td>
<td>E-06</td>
<td>E-21</td>
<td>E-18</td>
<td></td>
</tr>
<tr>
<td>LECTOR</td>
<td>4.1964</td>
<td>3.5736</td>
<td>2.6488</td>
<td>0.5876</td>
<td>13.3254</td>
<td>4.9676</td>
<td>17.85</td>
<td>23.7</td>
<td>88.13</td>
</tr>
<tr>
<td>E-09</td>
<td>E-10</td>
<td>E-10</td>
<td>E-11</td>
<td>E-11</td>
<td>E-10</td>
<td>E-06</td>
<td>E-21</td>
<td>E-18</td>
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<td>E-11</td>
<td>E-11</td>
<td>E-12</td>
<td>E-12</td>
<td>E-10</td>
<td>E-06</td>
<td>E-22</td>
<td>E-18</td>
<td></td>
</tr>
</tbody>
</table>

Dynamic power consumption is estimated with arbitrary input vectors. Similar to leakage power estimation, the dynamic power dissipation is measured using four possible input vectors.

CONCLUSION

Throughout logic design, the proposed method could be used to reduce the static power and dynamic power of CMOS circuits. Minimal additional circuitry is used to amend the original CMOS logic design to operate into a low-leakage state during both active and idle mode of operations. Experimental results show that the proposed method provides an efficient power savings and is easier to fabricate due to its standard $V_{th}$ implementation.

REFERENCES


