Journal of Applied Sciences

ISSN 1812-5654

science alert

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Journal of Applied Sciences 10 (18): 2136-2146, 2010
ISSN 1812-5654

The Future of Non-planar Nanoelectronics MOSFET Devices: A Review

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Abstract: This study was focused on the evaluation of present development of nanoelectronic devices and the projection of future devices, ultimately for non-planar geometry. The recent scaling of IC technology was limiting the employment of conventional, planar structure, thus implies in the wake of the research in non-classical architecture. The present status of extended planar silicon devices, including the insertion of high-k dielectric, metal gate and SOI MOSFET in the recent manufacturing process is elaborated. The alternative path in the enhancement of IC device performance, merely in the sub-50nm dimension is shown, with the role of double gate MOSFET and non-planar structure devices, including vertical FETs, is expected to take greater share, as well as several emerging nanostructures. The possibility to implement the non-planar devices generation heavily depends on the maturity of each technology and the ability to clear the obstacles in processing.

Key words: Nanoelectronics, non-planar structures, vertical MOSFET, double gate, emerging devices

INTRODUCTION

The progress of semiconductor electronics devices has been marked by the rapid improvement of performance and low cost application, along with the tremendous down-scaling of the transistor size, mainly for the channel length. The scaling of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) device as the main device in electronic circuits has led to increasing performance in electronic systems with more features and higher processing speed, while the performance-to-cost ratio is also rising. Moore's Law predicted that the transistor density on Integrated Circuit (IC) would be doubled every two years, which drives the great development in semiconductor industries (Moore, 1995; Schaller, 1997). It is expected that the prediction will still valid for the next decade, according to the latest International Technology Roadmap for Semiconductors (ITRS, 2009).

Recently, Intel's commercial silicon process has employed 45 nm MOSFET technology (Intel, 2004) and soon will be in full production for 32 nm technology (Intel, 2010). However, some challenges on the conventional lateral MOSFET arose enormously for the nanoscale (Wong *et al*., 2005; Oda and Ferry, 2006). The biggest impact of dimension reduction goes to the lithography which is limited by the wavelength of light source used in its system. The commercial optical lithography has resolution of 70 nm using Deep/eXtreme UltraViolet (DUV/XUV) wavelength (Lin, 2006a), but it is hard to meet the challenge of smaller geometries. Other lithography techniques exist, such as scanning electron beam (Cord *et al*., 2009), immerse (Lin, 2006b) and x-ray lithography (Taur *et al*., 1997; Wong *et al*., 2005), but all contain technical problems that remain to be solved for smaller resolution, not to mention the very complicated and sophisticated equipments and facility installment required which dramatically increase the manufacturing cost and complexity. Other challenges over the channel scaling are lying on the fundamental physical limitations of the device and also the presence of short channel effects (SCE), including threshold voltage (V_T) roll-off, increasing leakage current (I_{off}) roll-off, drain induced barrier lowering (DIBL) and rising dissipation power (P_{disp}) (Frank *et al*., 2001). The presence of the deteriorating effects has been the key problem that threatens to degrade the performance in the next generation of devices.

Alternative technologies are essential as well as advanced device physics approach for continuing the progress in nanoscale. For this purpose, many researches were conducted extensively in new materials and new device structures. With the limitation of conventional structure, several innovative devices emerge as new

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promising structure with nanoscale gate length dimension in order to keep pace with Moore's Law in maintaining the performance progress. Thus, this review will be focused on the present state of planar MOSFET devices and elaboration of non-planar MOSFET architecture, as well as the emerging nanodevices for channel length down to nanoscale.

PLANAR MOSFET IN NANOSCALE

The planar bulk MOSFET with a symmetrical source and drain region divided by the channel area has been around for more than four decades and it retains almost the same basic structure design. For years, the successful development of MOSFET has been largely dominated by the size shrinking of its physical properties (Wong *et al*., 1999; Liu and Chang, 2009). Initially, all dimensions and also voltages are reduced by a factor α and the doping is increased by the same factor (originally proposed by Dennard *et al*. (1974)). But voltage scaling has been slow because the subthreshold slope, the OFF current and built-in potentials are not scalable (Frank *et al*., 2001). Moreover, the device widths and wiring dimensions have not been scaled as fast as the channel lengths. As a result, the scaling strategy is more complex in these days, when the channel length approaches sub-100 nm (Zeitzoff, 2006). The scaling of MOSFET leads to SCE in its electrical characteristics, due to the increased electric field in the channel and the unscalable factors that led to shifting of current-voltage relationship and deteriorate the power consumption.

Several techniques were developed to reduce SCE and also maintain superior device performance in nanometer scale. Figure 1 shows some improvements of conventional CMOS to reduce unwanted scaling effects. However, the limits to MOSFET scaling keep approaching. The t_{ox} cannot be less than 1 nm due to higher tunneling current and significant statistical variation (Yu *et al*., 2000). Ultra shallow junction tends to increase parasitic resistance and poses reliability issue between devices in a batch (Wong *et al*., 2005). Nevertheless, the lowering of carrier mobility cannot be avoided in channel of very high impurity doping, which in turn reduce the drain current. The substrate doping is high (>10^{19} cm^3) that leakage and tunneling currents are becoming unacceptable for certain applications (Moers, 2007). The current scaling rate, if sustained, will release heat at the chip's surface as strong as the sun's surface, in this decade (Masahara *et al*., 2008). Moreover, the ultimate physical limit of the scaling is believed to be the distance of atoms in silicon crystals which is around 0.3 nm (Iwai *et al*., 2006). Thus, up to certain point, further scaling will be unrealistic and very difficult to predict.

The Silicon on Insulator (SOI) technique was introduced to improve the conventional MOSFET design. It has been around at least since 1980's and been applied in AMD's commercial processors (AMD, 2002). Many fabrication methods has been proposed to for SOI, which was elaborated in length by (Celler and Cristoloveanu, 2003). By inserting dielectric below the transistor, it is expected that the problem due to exaggerated field can be hold, while the fringing capacitance is suppressed, that in

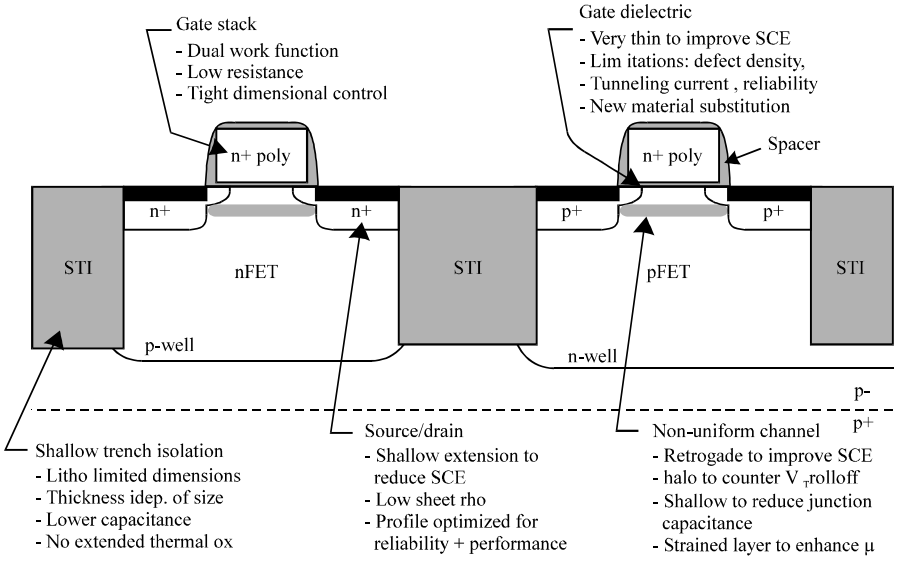

Fig. 1: Several techniques in CMOS fabrication in reducing unwanted effects (Oda and Ferry, 2006; Wong *et al*., 1999)

turns give better speed (Yu *et al*., 2007). It also improves devices isolation which combines the STI and the back oxide (Ioannou, 2005). The SOI design goes further by thinning the body, to achieve fully depleted regime; an attempt to increase the performance. The Ultra Thin Body (UTB) Silicon on Insulator (SOI) MOSFET could reduce subthreshold swing near ideal value (60 mV/decade) (Oda and Ferry, 2006). However, it also contain problem in the power dissipation issue as the heats resulted by the devices cannot be absorbed by the substrate due to the temperature resistance of the back oxide, which may affect the operating temperature of the device.

The strained Si layer is another option introduced for increasing the mobility, which has been applied in recent AMD production (AMD, 2002) as well as in Intel (Mistry *et al*., 2007). By growing epitaxial silicon layer on $Si_{1-x}Ge_x$ layer, the grown Si lattice constant follows that of the layer beneath and creates energy band splitting:

$$\frac{\Delta E \approx 67meV}{10\%\ Ge}$$

which enhances the low field effective mobility μ_{eff} and reduces scattering (Hoyt *et al*., 2002; Thompson *et al*., 2004). The strained Si is strongly correlated with the portion of Ge in the $Si_{1-x}Ge_x$, with optimum value found to be around 15-25% (Olsen *et al*., 2004). However, due to higher demand of current drive, the strained silicon is still approaching its physical limit (Yang *et al*., 2007). In addition, some current process techniques in strained Si tend to be less effective with scaling.

Other non-classical MOSFET technologies have also been emerged, while retaining the conventional planar structure. The junction engineering along with source or drain extension were applied to prevent the charge sharing effect and to control S/D junction (Wu *et al*., 1995; Koo *et al*., 2003; Muller *et al*., 2003). The introduction of new materials was also popular, although the compatibility with standard CMOS fabrication is an issue. In the recent technology generation, high-κ gate dielectrics (e.g., zirconia, HfO_2 (Verheyen *et al*., 2005)) have been implemented as replacement to SiO_2 in order to maintain the acceptable dielectric thickness while keeping gate leakage currents within tolerable limits. Metal gates (Cheng *et al*., 1999; Hou *et al*., 2004) or dual work function gates (Polishchuk *et al*., 2001) have also been re-introduced to avoid the polysilicon depletion effect which creates unwanted parasitic gate capacitance. However, threshold voltage control with metal gate and high-κ material has been very challenging, especially for low threshold voltage devices, mainly because of difficulties in setting the effective work function at the conduction and valence band edges for n-type and p-MOSFETs, respectively (ITRS, 2009).

EMERGING NON-PLANAR DEVICE STRUCTURE

The non-planar structures option seems viable to be a contender in prolonging the future progress of MOSFET. While the scaling of the dimension is still seen by most major manufacturers as a cost-effective way to maintain the progress than to invest with completely new technology, the emergence of novel structures have strengthened in recent years. Now that the scaling of the conventional bulk silicon MOSFET starts slowing down, the non-planar device structures become inevitable in continuation of performance improvement.

DOUBLE-GATE STRUCTURE

Double Gate (DG) structure has been considered as a main way to improve the performance of single gate classical MOSFET. The DG-FET is electrostatically more robust than the classical MOSFET since both gates act as shields to the channel so that they suppress field penetration from the gate, which leads to reducing short-channel effects (low DIBL) (Wong *et al*., 1999; Solomon *et al*., 2003). It produces close-to-ideal subthreshold slope (60 mV/dec) due to a high gate-to-substrate coupling and it offers flexible V_T control by separation of two gates (Masahara *et al*., 2008). Better SCE immunity implies that DG structures may use low-doped/undoped channels, which reduce dopant fluctuation problems usually found in very high doping, improves carrier transport properties of channel and reduces band-to-band tunneling (BTBT) leakage current near the drain (Schulz *et al*., 2002; Cho *et al*., 2008).

The double-gate FET can be formed on bulk silicon CMOS by connecting the doped well to the gate (Solomon *et al*., 2003), but it is much more effective to use a true insulated gate. As discussed by Frank *et al*. (2001), stricter requirements for oxide leakage in low power applications, as well as and subthreshold and substrate tunneling currents, lead to larger estimates for minimum channel length and boost the application of DGFET. Moreover, both gates of DGFET may be biased independently to improve the device control (Schulz *et al*., 2002). The threshold voltage can be controlled by this scenario to increase performance or raised to reduce standby power. The separate biasing can also be used to achieve increased logic function from a single FET. In the standard configuration, although a

biased well can be used for similar function, it is rarely applied due to the impact on capacitance, circuit density and leakage current when forward biased (Solomon *et al*., 2003).

A projection of the I_D-V_{GS} characteristics of single and double gate FETs is shown in Fig. 2a. The DG-FET provides sharper slope resulting from the gate coupling advantage, which also gives lower threshold voltage for a given off-current. This in turn gives higher drive currents at lower power-supply voltages V_{DD}. It is clearly evident in Fig. 2b for shorter channel length, where the MEDICI-projected DIBL and subthreshold swing for the DG device are significantly improved relative to those of the bulk-silicon counterpart (Nowak *et al*., 2004).

Some DG topologies are shown in Fig. 3. It describes the current direction relative to the substrate plane and the position between gates. Type I expresses the lateral DGFET, while Types II and III are vertical double gate FET (VDGFET) and FinFET, respectively. The comparison of each type is shown in Table 1. The VDGFET or the FinFET are easier to fabricate than the lateral DGFET. In the vertical and fin geometries the body thickness is controlled by lithographic and etching processes, respectively. The gates must be precisely aligned (to within one quarter of the gate length), to avoid compromised performance (Wong *et al*., 1999; Frank *et al*., 2001). The feature for self-alignment between gates is more easily produced by VDGFETs and FinFETs but harder to make in the lateral double gate FETs. On the other hand, the lateral DG FETs and FinFET depend heavily on lithography in defining the channel length, thus the critical problem in the lithography give bigger impact on further device design.

Vertical MOSFET: The vertical structure offers several advantages as well as challenges over the conventional/planar structure, according to published results. The main advantage is the possibility to further downscale the device with relaxed lithography for channel length definition. The channel definition of vertical MOSFET is achieved using careful layer deposition or other thin film definitions, in which the lithography is not very critical (Schulz *et al*., 2001; Gili *et al*., 2004; Moers *et al*., 2004; Masahara *et al*., 2006). The second

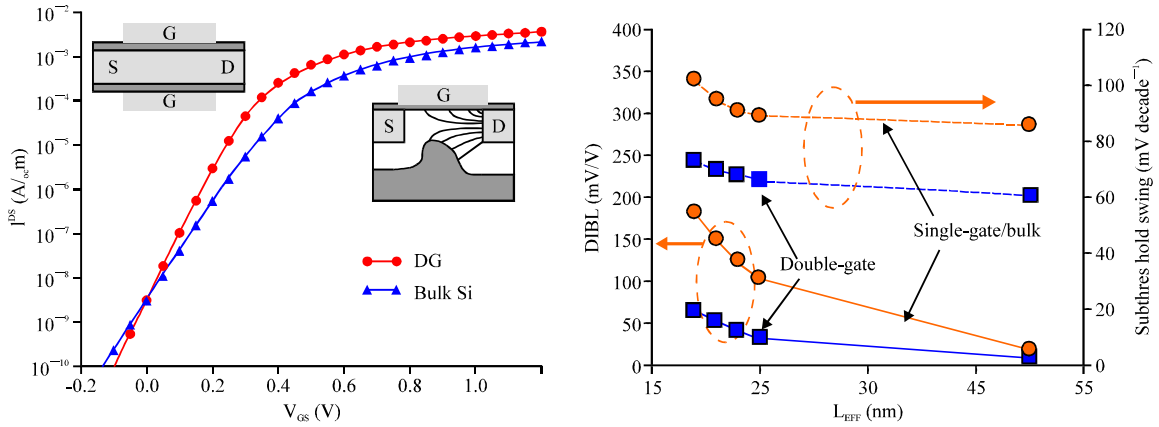

Fig. 2: (a) Transfer characteristic of MEDICI-predicted performance of bulk and double-gate MOSFETs and (b) the DIBL and subthreshold swing for different channel length (Nowak *et al*., 2004), (with permission. ©2004 IEEE)

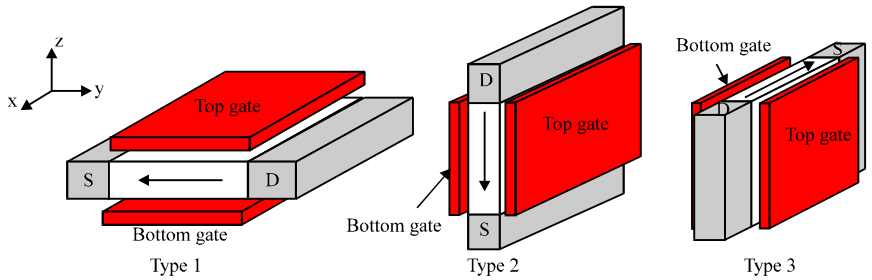

Fig. 3: Double Gate types, according to current direction and the position of both gates: lateral DG (Type I), Vertical DG FET (Type II) and FinFET (Type III) (Wong *et al*., 1999)

advantage of vertical MOSFET is that it could reduce the required space, depending on the application, as well as doubling the channel width per transistor area. This leads to an increase of packing and integration density and drive current as compared to the planar MOSFET (Moers, 2007; Ertosun *et al*., 2008). Other important advantage is the prospect of having easier implementation of double/multiple gates formation in the structure than in conventional MOSFET, added with the possibility to make self-aligned gates accordingly (Masahara *et al*., 2005; Cho *et al*., 2008) which directly affect the performance, as previous sub-section suggests.

Conventional MOSFET has a symmetric structure of source and drain related to the channel region. In the vertical structure, there is a slight difference in device performance, depending on whether it is Source on Top (SOT) or drain (DOT), as revealed by some reports (Gili *et al*., 2006a). Another issue is the control of excessive overlap capacitance of gate over source and drain (Schulz *et al*., 2001; Hall *et al*., 2004). The definition of source and drain in one side and the deposition of gate material without proper aligning in vertical direction by and large lead to this crucial problem.

Vertical MOSFETs are commonly fabricated using layer epitaxy, ion implantation and solid source diffusion methods (Fig. 4). Generally, the epitaxy growth methods (Behammer *et al*., 1996; Risch *et al*., 1996; Fink *et al*., 2000; Jayanarayanan *et al*., 2006) produce sharp junction, easily crafted to get sub-nm channel and requires simpler step in making pillar and gate. However, its low throughput and high overlap capacitance are major problems, added with floating body effect conceded, which leads to degraded performance. The solid source diffusion techniques (Hergenrother *et al*., 2002; Liu *et al*., 2004) provide better self-aligned S/D extensions via sacrificial deposited layer but in a complex process and it sets thermal budget limitation for following processing steps due to out-diffusion concern. Both previous methods lacks from CMOS processing compatibility due to different layer sequences for n and p-channels. On other hand, the implantation methods (Mori *et al*., 2002; Schulz *et al*., 2002; Gili *et al*., 2006b; Saad and Ismail, 2008) offer easy self alignment (both for S/D extension and also for multi gate formation) and also maintains CMOS compatible possibility. It is also possible to do selective implantation by masking the unwanted area with resist layer. However, tight junction control is needed in defining the channel. It also has a probable defect by high energy implant (Table 2).

Parasitic overlap capacitance problem is a drawback in most vertical DGFET structure. A method of sacrificial polysilicon oxidation (Fig. 5) was proposed to reduce the overlap problem (Cho *et al*., 2008). Another technique by formation of fillet local oxidation (FILOX) above source/drain region (Fig. 6a, b) was successfully introduced to reduce the problem (Gili *et al*., 2004; Hall *et al*., 2004). Subsequently this work was enhanced by other works such as by incorporating dielectric pocket (Donaghy *et al*., 2004; Gili *et al*., 2005; Jayanarayanan *et al*., 2006; Riyadi *et al*., 2008a) or by

Table 1: Comparison of double gate structure variations, from Fig. 3

Parameters	Type I	Type II	Type III
Current direction	Lateral	Vertical	Lateral
Gate-gate formation	Top-down	Left-right	Left-right
Self-aligned gates	Difficult	Possible	Possible
Lithography-bound channel length	Yes	No	Yes
Compatibility to existing process technology	Difficult	Moderate	Moderate
S/D overlap capacitance	-	+	-

Table 2: Performance comparison of several published data using implantation method

Parameter characteristics	IBRE (Masahara *et al*., 2004)	Mori *et al*. (2002)	Cho *et al*. (2008)	ORI (Saad and Ismail, 2008)	FDDG (Riyadi *et al*., 2009)
Channel length (nm)	100(DG)	100 (DG)	250 (DG)	90 (DG)	70 (DG)
Pillar (nm)	18	- (trench)	45	136	25
$N_{substrate}$ (cm^{-3})	10^{15}	2.10^{18}	2.10^{17}	5.10^{18}	10^{19}
t_{ox} (nm)	5	7	8	3	3
V_T (V)	- 0.2	0.8	-0.3	0.56	0.43
I_{off} (A)	10^{-13}				
(V_g = -1.0 V)	10^{-11}	$8.6.10^{-14}$			
(V_g = -0.9 V)	10^{-14}	2.10^{-13}			
S (mV dec^{-1})	72	97	65	94	66
DIBL (mV V^{-1})	50	70	13	100	20
Body contact	No (FD)	No (floating)	No (FD)	Yes	No (FD)

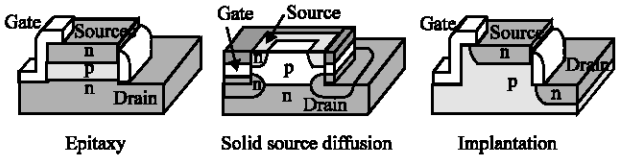

Fig. 4: Vertical MOSFET fabrication methods (Schulz *et al*., 2001), (with permission ©2001 IEEE)

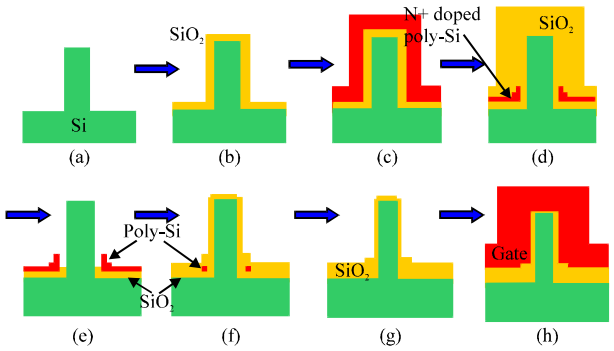

Fig. 5: Overlap capacitance reduction technique proposed by Cho *et al.* (2008): (a) Si pillar. (b) Oxidation or LTO deposition. (c) N+ -doped poly-Si deposition. (d) Oxidation until the top poly-Si is fully consumed. (e) HF dip, remaining poly-Si acts as a hard mask. (f) Sacrificial oxidation. (g) HF dip, gate oxidation. (h) Gate polydeposition. (©2008 IEEE, with permission)

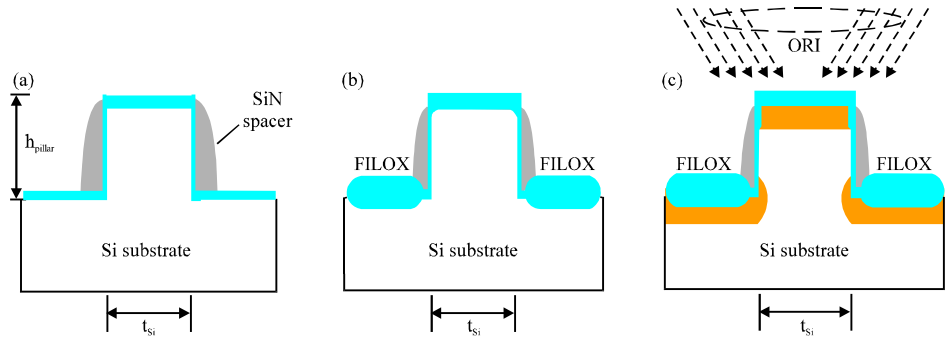

Fig. 6: The combination of FILOX and ORI techniques: (a) spacer is formed on the sidewall, (b) oxidation to form FILOX and (c) the ORI to improve the doping of source/drain region

introducing Oblique Rotating Implantation (ORI) method (Riyadi *et al*., 2008b; Saad and Ismail, 2008). While the ORI method (Fig. 6c) suggests good tendency in producing vertical MOSFET, by combining the benefit of the fully depleted feature in this compatible process (Riyadi *et al*., 2009), a better device performance is revealed while keeping the possibility to further scaling, as shown in. In the Fully Depleted (FD) DG FET, the majority carrier concentration in the channel region is depleted when a certain gate voltage is applied. This phenomenon provides reduced junction capacitance and also offers near ideal subthreshold swing with reduced kink effect (Xiangli *et al*., 2003). The FD DGFETs have higher punch through immunity in the short gate length region, compared to the conventional single gate MOSFET case. This device is also able to eliminate Floating Body Effect (FBE) (Pretet *et al*., 2002; Hakim *et al*., 2006). In Partial Depleted (PD) devices, floating body can charge up which will eventually cause dc effects such as premature breakdown and increasing subthreshold swing at high drain bias. It could also ignite parasitic bipolar mechanism, as the majority carrier in body is pulled down and concentrated in the bottom and later cause greater leakage current over the body. Therefore, the tendency of further device development is toward the fully depleted configuration and the drive toward this settlement is stronger for nanocale device.

Multiple-gate FET: Several multiple-gate FET concepts which are mostly based on SOI technology have been around, e.g. triple-gate FETs, Ω/Π-gate and gate-all-around (Jong-Tae and Colinge, 2002; Colinge, 2004; Poiroux *et al*., 2005; Im *et al*., 2008), as shown in Fig. 7. These devices offer a higher current drive per unit silicon area than conventional MOSFETs. In addition they offer optimal short-channel effects (reduced DIBL and subthreshold slope degradation). A variant of multiple-gate FET, gate-all-around (GAA) FET (Song *et al*., 2006) is often considered as quasi-1D devices. Its physics are similar to the nanowire, with the main channel in inner material surrounded by the dielectrics and gate material, from which the

surrounded-gate FET name comes. The construction of GAA FETs is easily obtained with vertical FET-like processing, as the dielectric and gates can be grown around the cylindrical or rectangular channel with homogeneous thickness, while in horizontal scheme, the homogeneous thickness of dielectrics are hard to fabricate. The cylindrical GAA FETs is particularly of interest due to its uniform field in the channel, offering the simplicity in design and modeling.

The multiple-gate FETs are able to provide higher current drive than the double gate FETs. However, the multiple-gate FET suffers from the practicality of the fabrication (except for the vertical GAA FET), a drawback that seems to be biggest obstacle for adoption. Moreover, the double gate structures have the flexibility to separate the gates (Poiroux *et al*., 2005), thus enabling the adjustment of threshold voltage by controlling separating gates.

Emerging nanostructures and materials: In the search for extending the progress of nanoelectronic devices, materials other than silicon has been under intense scrutiny. Several candidates have been promoted with the FET-like operation, e.g., carbon nanotubes (Javey *et al*., 2003, 2004), graphene (Grassi *et al*., 2009), nanowires (Wan *et al*., 2009), etc, all in quasi-1D devices. Carbon Nanotube (CNT) FETs features high carrier mobility and high quasi-ballistic charge carrier velocity which has the potentials to overcome the short channel effects. However, several challenges lay on its development as it requires process for gate and dielectric to wrap the channel, similar to horizontal nanowire, which is hard to get in lateral direction. It is also extremely difficult to produce reliable single wall semiconducting nanotubes and control the band gap energy. With very different material properties than Si, controlling the carrier type and density cannot be made as in regular FET. The control of chirality in carbon nanotube and the growth of nanotube position are another big obstacle. Nanowire FETs with various materials offer an appealing approach to scaling MOSFETs with features similar to CNT FETs. However, it poses challenges related to its growth and manufacturing process, added with the reliability issue, whilst contain severe parasitic resistances and capacitances. Graphene nanoribbon (GNR) is also under intense research nowadays. It is used as a channel replacement material with prospective properties to be an alternative for silicon. Unfortunately, the technology has not reach a mature stage while facing several important challenges. Unless several materials and process challenges have been overcome, these alternatives may not offer sufficient device gain to be competitive in mass production, at least for next decade.

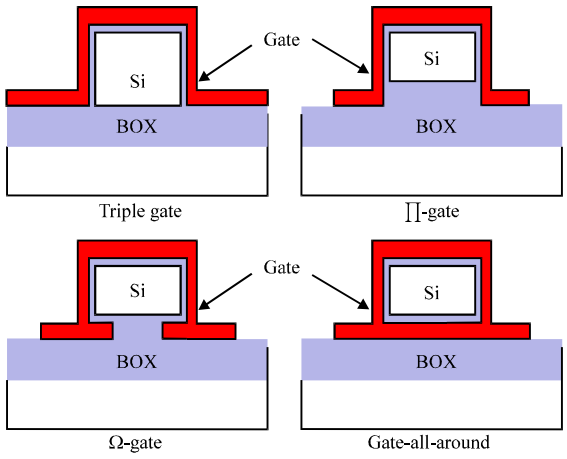

Fig. 7: Several multiple-gate FET concepts

CONCLUSIONS

The recent progress of nanoelectronic devices has revealed many novel devices under consideration. Even though some devices have achieved experimental results comparable with some of the best silicon FETs, these devices have yet to show electrical characteristics beyond the basic, functional level (Wong, 2005). In several years from now, the planar MOSFET, combined with high-k dielectric and coupled with strained layer technology, is expected to maintain its domination the market, due to the fact that the manufacturers still attempt to exploit their existing manufacturing capabilities and seem reluctant to adopt new technology. However, the double- and multi-gate MOSFET scaling is superior to recent planar MOSFET and also to UTB FD MOSFET scaling, thus the double and multi-gate device is projected as the ultimate MOSFET. The role of double gate MOSFET and non-planar will take greater share, as this technology become mature and the risk are more understandable in near future.

On the other hand, several issues on fabrication in adoption route to standard fabrication have to be solved for every other technology. Figure 8 indicates the projection for the first year of full scale production for future nanoelectronic devices by ITRS, which reflect the degree of complexity in fabrication for each technology. New MOSFET structures, starting with UTB-SOI MOSFETs and followed by multi-gate MOSFETs, will be implemented soon. The next generation devices, e.g. carbon nanotubes, graphene, spin transistor etc are promising, due to their performances shown by many researches. However, the processing issues force them to

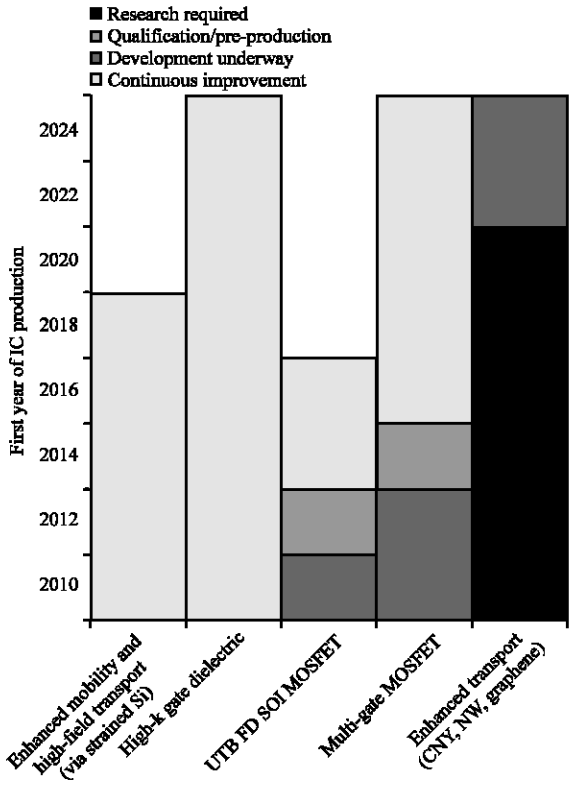

Fig. 8: Projection for the first year of full scale production for future nanoelectronic devices (ITRS, 2009)

take longer step to be main devices for nanoelectronics. In addition, different companies may take different timing in extending planar bulk and then switching to the advanced technologies, depending on their technological strengths. Understanding the reliability issues for all these innovations in a timely manner is very crucial and a great task that remains to be solved.

ACKNOWLEDGMENTS

The authors would like to acknowledge the financial support from E-Science grant (Vot. No 79178) of Malaysia's Ministry of Science, Technology and Innovation (MOSTI). The authors express their gratefulness to the Research Management Centre (RMC) of UTM for providing research environment in conducting this work.

REFERENCES

AMD, 2002. AMD demonstrates next-generation processor. http://www.amd.com/us/press-releases/Pages/Press_Release_15118.aspx.

Behammer, D., L. Vescan, R. Loo J. Moers, A. Muck, H. Luth and T. Grabolla, 1996. Selectively grown vertical Si-p MOS transistor with short channel-lengths. Electron. Lett., 32: 406-407.

Celler, G.K. and S. Cristoloveanu, 2003. Frontiers of silicon on insulator. J. Applied Phys., 93: 4955-4955.

Cheng, B., M. Cao, R. Rao A. Inani and P.V. Voorde *et al.*, 1999. The Impact of High-κ Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFET's. IEEE Trans. Electron Devices, 46: 1537-1537.

Cho, H., P. Kapur, P. Kalavade and K.C. Saraswat, 2008. A low-power, highly scalable, vertical double-gate MOSFET using novel processes. IEEE Trans. Electron Devices, 55: 632-639.

Colinge, J.P., 2004. Multiple-gate SOI MOSFETs. Solid-State Electron., 48: 897-905.

Cord, B., J. Yang, H. G. Duan D.C. Joy and J. Klingfus, 2009. Limiting factors in sub-10 nm scanning-electron-beam lithography. J. Vac. Sci. Technol. B, 27: 2616-2621.

Dennard, R.H., F.H. Gaensslen, V.L. Rideout, E. Bassous and A.R. Le Blanc, 1974. Design of ion-implanted MOSFET's with very small physical dimensions. Solid-State Circ. IEEE J., 9: 256-268.

Donaghy, D., S. Hall, C.H. de Groot, V.D. Kunz and P. Ashburn, 2004. Design of 50-nm vertical MOSFET incorporating a dielectric pocket. IEEE Trans. Electron Devices, 51: 158-161.

Ertosun, G.M., H. Cho, P. Kapur and K.C. Saraswat, 2008. A nanoscale vertical double-gate single-transistor capacitorless DRAM, IEEE Electron Device Lett., 29: 615-617.

Fink, C., K.G. Anil, W. Hansch, S. Sedlmaier, J. Schulze and I. Eisele, 2000. MBE-grown vertical power-MOSFETs with 100-nm channel length. Thin Solid Films, 380: 207-210.

Frank, D.J., R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur and H.S.P. Wong, 2001. Device scaling limits of Si MOSFETs and their application dependencies. Proc. IEEE, 89: 259-288.

Gili, E., V.D. Kunz, C.H. de Groot, T. Uchino and P. Ashburn *et al.*, 2004. Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance. Solid State Electron., 48: 511-519.

Gili, E., T. Uchino, M.M.A. Hakim, C.H.D. Groot, P. Ashburn and S. Hall, 2005. A new approach to the fabrication of CMOS compatible vertical MOSFETs incorporating a dielectric pocket. Proceedings of the 6th International Conference on ULtimate Integration of Silicon (ULIS), April 7-8, Bologna, Italy, pp: 127-130.

Gili, E., T. Uchino, M.M.A. Hakim, C.H. Groot, O. Buiu, S. Hall and P. Ashburn, 2006a. Shallow junctions on pillar sidewalls for sub-100-nm vertical MOSFETs. IEEE Electron Device Lett., 27: 692-695.

Gili, E., V.D. Kunz, T. Uchino, Hakim, M.M.A., C.H. de Groot, P. Ashburn and S. Hall, 2006b. Asymmetric gate-induced drain leakage and body leakage in vertical MOSFETs with reduced parasitic capacitance. IEEE Trans. Electron Devices, 53: 1080-1087.

Grassi, R., S. Poli, E. Gnani, A. Gnudia, S. Reggiania and G. Baccarania, 2009. Tight-binding and effective mass modeling of armchair graphene nanoribbon FETs. Solid-State Electron., 53: 462-467.

Hakim, M.M.A., C.H. de Groot, E. Gili, T. Uchino, S. Hall and P. Ashburn, 2006. Depletion-isolation effect in vertical MOSFETs during the transition from partial to fully depleted operation. IEEE Trans. Electron Devices, 53: 929-933.

Hall, S., D. Donaghy, O. Buiu, E. Gili and T. Uchino *et al*., 2004. Recent developments in deca-nanometer vertical MOSFETs. Microelectron. Eng., 72: 230-235.

Hergenrother, J.M., S.H. Oh, T. Nigam, D. Monroe, F.P. Klemens and A. Kornblit, 2002. The vertical replacement-gate (VRG) MOSFET. Solid State Electron., 46: 939-950.

Hou, Y.T., M.F. Li, T. Low and K. Dim-Lee, 2004. Metal gate work function engineering on gate leakage of MOSFETs. IEEE Trans. Electron Devices, 51: 1783-1789.

Hoyt, J.L., H.M. Nayfeh, S. Eguchi, I. Aberg and G. Xia *et al*., 2002. Strained silicon MOSFET technology. Proceedings of the Technical Digest of the IEEE International Electron Devices Meeting, Dec. 8-11, Washington, pp: 23-26.

ITRS, 2009. The international technology roadmap for semiconductors. http://www.itrs.net/reports.html.

Im, M., J.W. Han, H. Lee, L.E. Yu and S. Kim *et al*., 2008. Multiple-gate CMOS thin-film transistor with polysilicon nanowire. IEEE Electron Device Lett., 29: 102-105.

Intel, 2004. Intel drives moore's law forward with 65 nanometer process technology. http://download.intel.com/museum/Moores_Law/Articles-Press_Releases/Press_Release_Aug2004.pdf.

Intel, 2010. Intel® 32nm logic technology. http://www.intel.com/technology/architecture-silicon/32nm/index.htm.

Ioannou, D.E., 2005. Scaling limits and reliability of SOI CMOS technology. J. Phys. Conf. Ser., 10: 1-6.

Iwai, H., K. Kakushima and H. Wong, 2006. Challenges for future semiconductor manufacturing. Int. J. High Speed Electron. Syst., 16: 43-82.

Javey, A., J. Guo, D.B. Farmer, Q. Wang and D. Wang, 2004. Carbon nanotube field-effect transistors with integrated ohmic contacts and high-gate dielectrics. Nano. Lett., 4: 447-450.

Javey, A., J. Guo, Q. Wang, M. Lundstrom and H. Dai1, 2003. Ballistic carbon nanotube field-effect transistors. Nature, 424: 654-657.

Jayanarayanan, S.K., S. Dey, J. P. Donnelly and S.K. Banerjee, 2006. A novel 50 nm vertical MOSFET with a dielectric pocket. Solid State Electron., 50: 897-900.

Jong-Tae, P. and J.P. Colinge, 2002. Multiple-gate SOI MOSFETs: device design guidelines. IEEE Trans. Electron Devices, 49: 2222-2229.

Koo, H., K. Lee, K. Lee, T.A. Fjeldlyc and M.S. Shurd, 2003. Analysis of the anomalous drain current characteristics of halo MOSFETs. Solid-State Electron., 47: 99-106.

Lin, B.J., 2006a. Optical lithography-present and future challenges. C. R. Phys., 7: 858-874.

Lin, B.J., 2006b. The ending of optical lithography and the prospects of its successors. Microelectron. Eng., 83: 604-613.

Liu, H., J.K. O. Sin, P. Xuan and J. Bokor, 2004. Characterization of the ultrathin vertical channel CMOS technology. IEEE Trans. Electron Devices, 51: 106-112.

Liu, T.J.K. and L. Chang, 2009. Transistor Scaling to the Limit. In: Into the Nano Era, Huff, H.R. (Ed.). Springer, Berlin Heidelberg, pp: 191-223.

Masahara, M., L. Yongxun, S. Hosokawa, T. Matsukawa and K. Ishii *et al*., 2004. Ultrathin channel vertical DG MOSFET fabricated by using ion-bombardment-retarded etching. IEEE Trans. Electron Devices, 51: 2078-2085.

Masahara, M., L. Yongxun, K. Sakamoto, K. Endo and T. Matsukawa *et al*., 2005. Demonstration, analysis and device design considerations for independent DG MOSFETs. IEEE Trans. Electron Devices, 52: 2046-2053.

Masahara, M., Y. Liu, K. Endo, T. Matsukawa and E. Suzuki, 2006. Vertical double-gate MOSFET device technology. Trans. Inst. Electrical Eng. Japan C, 126: 702-707.

Masahara, M., Y. Liu, K. Endo, T. Matsukawa and E. Suzuki, 2008. Vertical double-gate mosfet device technology. Electron. Commun. Jpn., 91: 46-51.

Mistry, K., C. Allen, C. Auth, B. Beattie and D. Bergstrom, 2007. A 45nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning and 100% Pb-free packaging. Proceedings of the IEEE International Electron Devices Meeting, Dec. 10-12, IEEE, pp: 247-250.

Moers, J., S. Trellenkamp, M. Marso, A. Hart and S. Mantl *et al*., 2004. Vertical double-gate MOSFETs, ASDAM 2004. Proceedings of the 5th International Conference on Semiconductor Devices and Microsystems, Oct. 17-21, Smolenics Castle, Slovakia, pp: 215-218.

Moers, J., 2007. Turning the world vertical: MOSFETs with current flow perpendicular to the wafer surface. Applid Phys. A, 87: 531-537.

Moore, G.E., 1995. Lithography and the future of Moores law. Proc. SPIE, 2437: 1-8.

Mori, K., A.K. Duong and W.F. Richardson, 2002. Sub-100-nm vertical MOSFET with threshold voltage adjustment. IEEE Trans. Electron Devices, 49: 61-66.

Muller, M., B. Froment, V. Carron, A. Beverina and R. Palla *et al*., 2003. New junction concepts for sub-50 nm CMOS transistors: Slim spacers and Ni silicide. Proceedings of the 33rd Conference on European Solid-State Device Research ESSDERC'03, Sept. 16-18, Philips Semicond, Crolles, France, pp: 31-34.

Nowak, E.J., I. Ludwig, T. Kim, K. Joshi and R.V.C.T.C. Bernstein *et al*., 2004. Turning silicon on its edge [double gate CMOS/FinFET technology. IEEE Circuits Devices Magazine, 20: 20-31.

Oda, S. and D. Ferry, 2006. Silicon Nanoelectronics. CRC Press, Boca Raton, FL.

Olsen, S.H., K.S.K. Kwa, L.S. Driscoll, S. Chattopadhyay and A.G. O'Neill, 2004. Design, fabrication and characterisation of strained Si/SiGe MOS transistors. IEE Proc. Circ. Devices Syst., 151: 431-437.

Poiroux, T., M. Vinet, O. Faynot, J. Widiez and J. Lolivier *et al*., 2005. Multiple gate devices: advantages and challenges. Microelectron. Eng., 80: 378-385.

Polishchuk, I., P. Ranade, T.J. King and C Hu, 2001. Dual work function metal gate CMOS technology using metal interdiffusion. IEEE Electron Device Lett., 22: 444-446.

Pretet, J., D. Ioannou, N. Subba, S. Cristoloveanua, W. Maszarad and C. Raynaude, 2002. Narrow-channel effects and their impact on the static and floating-body characteristics of STI- and LOCOS-isolated SOI MOSFETs. Solid-State Electron., 46: 1699-1707.

Risch, L., W.H. Krautschneider, F. Hofmann, H. Schafer, H. Schafer, T. Aeugle and W. Rosner, 1996. Vertical MOS transistors with 70 nm channel length. IEEE Trans. Electron Devices, 43: 1495-1498.

Riyadi, M.A., I. Saad and R. Ismail, 2008a. Silicon pillar thickness effect on vertical double gate MOSFET (VDGM) with oblique rotating implantation (ORI) method. Proceedings of the IEEE International Conference on Semiconductor Electronics, (ICSE'08), Johor Bahru, Malaysia, pp: 475-479.

Riyadi, M.A., Z.A.F.M. Napiah, I. Saad and R. Ismail, 2008b. Characterization analysis of a novel approach in fabrication of CMOS compatible vertical MOSFETs incorporating a dielectric pocket. Proceedings of the IEEE International Conference onSemiconductor Electronics, Nov. 25-27, Johor Bahru, Malaysia, pp: 639-642.

Riyadi, M.A., I. Saad, M.T. Ahmadi and R. Ismaila, 2009. Vertical double gate MOSFET For nanoscale device with fully depleted feature. AIP Conf. Proc., 1136: 248-252.

Saad, I. and R. Ismail, 2008. Self-aligned vertical double-gate MOSFET (VDGM) with the oblique rotating ion implantation (ORI) method. Microelectron. J., 39: 1538-1541.

Schaller, R.R., 1997. Moore's law: Past, present and future. IEEE Spectr., 34: 52-59.

Schulz, T., W. R?sner, E. Landgraf, L. Rischa and U. Langmannb, 2002. Planar and vertical double gate concepts. Solid State Electron., 46: 985-989.

Schulz, T., W. Rosner, L. Risch, A. Korbel and U. Langmann, 2001. Short-channel vertical sidewall MOSFETs. IEEE Trans. Electron. Devices, 48: 1783-1788.

Solomon, P.M., K.W. Guarini, Y. Zhang, K. Chan and E.C. Jones *et al*., 2003. Two gates are better than one. IEEE Circ. Devices Mag., 19: 48-62.

Song, J.Y., W.Y. Choi, J.H. Park, J.D. Lee and B.G. Park, 2006. Design optimization of gate-all-around (GAA) MOSFETs. IEEE Trans. Nanotechnol., 5: 186-191.

Taur, Y., D.A. Buchanan, W. Chen, W. Chen and D.J. Frank *et al*., 1997. CMOS scaling into the nanometer regime. Proc. IEEE, 85: 486-504.

Thompson, S.E., M. Armstrong, C. Auth, C. Auth and S. Cea *et al*., 2004. A logic nanotechnology featuring strained-silicon. IEEE Electron Device Lett., 25: 191-193.

Verheyen, P., G. Eneman, R. Rooyackers, R. Loo and L. Eeckhout, 2005. Demonstration of recessed SiGeS/D and inserted metal gate on HfO2 for high performance pFETs. Proceedings of the Technical Digest, IEEE International Electron Devices Meeting, (IEDM'05), Piscataway, New Jersy, pp: 907-910.

Wan, S., Y. Yu and J. Zhang, 2009. The synthesis of aligned silicon nanowires under ambient atmospheric pressure. J. Non-Cryst. Solids, 355: 518-520.

Wong, H.S.P., D.J. Frank, P.M. Solomon, C.H.J. Warm and J.J. Welser, 1999. Nanoscale CMOS. Proc. IEEE, 87: 537-570.

Wong, H.S.P., 2005. Beyond the conventional transistor. Solid-State Electron., 49: 755-762.

Wong, B. P., A. Mittal, Y. Cao and G. Starr, 2005. Nano-CMOS Circuit and Physical Design. John Wiley, Inc., Hoboken, New Jersey.

Wu, Z.Y., L.J. McDaid and S. Hall, 1995. Reverse heterojunction engineering: A novel technique for the suppression of the parasitic bipolar transistor in deep sub-micron MOSFETs. IEE Seminar Digests, 1995: 12-12.

Xiangli, L., S.A. Parke and B.M. Wilamowski, 2003. Threshold voltage control for deep sub-micrometer fully depleted SOI MOSFET. Proceedings of the IEEE 15th Biennial University/Government/Industry Microelectronics Symposium, June 30-July 2, Boise, Idaho, pp: 284-287.

Yang, Y.J., W.S. Ho, C.F. Huang S.T. Chang and C.W. Liu, 2007. Electron mobility enhancement in strained-germanium n-channel metal-oxide-semiconductor field-effect transistors. Applied Phys. Lett., 91: 102103-102103.

Yu, B., H. Wang, C. Riccobene, Q. Xiang and M.R. Lin, 2000. Limits of gate-oxide scaling in nano-transistors. Proceedings of the Symposium on VLSI Technology, 2000 Digest of Technical Papers. 2000, (SVTDTP'00), USA., pp: 90-91.

Yu, T., H. Ru, Z. Xing and W. Yang-Yuan, 2007. Tradeoff between speed and static power dissipation of ultra-thin body SOI MOSFETs. China Phys., 16: 1743-1747.

Zeitzoff, P.M., 2006. Trends and challenges in MOSFET scaling. Solid State Technol., 49: 42-44.