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# VLSI Design of Pipelined R2MDC FFT for MIMO OFDM Transceivers

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**Abstract:** In this study, an area-efficient low power FFT (Fast Fourier Transform) processor is proposed for MIMO-OFDM (Multi Input Multi Output-Orthogonal Frequency Division Multiplexing) that consists of a modified architecture of radix-2 algorithm which is described as Radix-2 Multipath Delay Commutation (R2MDC). Orthogonal frequency-division multiplexing is a popular method for high-data-rate wireless transmission. OFDM may be combined with multiple antennas at both the access point and mobile terminal to increase diversity gain and/or Enhance system capacity on a time-varying multi path fading channel, resulting in a multiple-input multiple-output OFDM system. This study described the VLSI design of R2MDC FFT for high throughput MIMO OFDM transceivers targeted to future wireless LAN systems. The proposed system is pipelined Radix 2 multipath delay commutation FFT has been designed for MIMO OFDM. The MIMO OFDM transceivers have been designed according to the proposed OFDM parameters. A low-power efficient and full-pipelined architecture enables the real-time operations of MIMO OFDM transceivers. The FPGA board has been developed to verify their circuit behavior and implementation of MIMO OFDM Transceivers.

**Key words:** Radix-2 multipath delay commutation, frequency division multiplexing, inverse fast Fourier transform, fast Fourier transform, discrete Fourier transform

## INTRODUCTION

MIMO-OFDM is the efficient solution for transmitting and receiving the data over the long distance. The sub-carrier frequency has been chosen in our proposed OFDM transceivers so that cross-talk between the sub-channels are eliminated, hence the inter carrier guard bands are not required. Jongren *et al.* (2002) was also used such type of guard band for eliminating the cross-talk between channels. This greatly simplifies the design of both the transmitter and the receiver; unlike conventional FDM, a separate filter for each sub-channel is not required. The orthogonally allows for efficient modulator and demodulator implementation using the FFT algorithm. OFDM Transceivers is popular for wideband communications today by way of low-cost MIMO OFDM Transceivers requires very accurate frequency synchronization between the receiver and they have their reduced the complexity. This matter has also discussed clearly by Bolcskei *et al.* (2002). In this study, a Pipelined FFT processor is proposed for MIMO-OFDM. The proposed FFT Processor is based on radix-2 multipath delay commutation. The Radix-2 algorithm with MDC Architecture is to support 4-channel 8, 16, 32, 64, 128, 512, 1024 and 2048-point FFT operations. We compare this proposed architecture with existing 8-point radix 2 and radix 4 FFT and also give the design and implementation results of the proposed FFF processor. The FPGA design and implementation has been studied by Coulton and Carline (2004) and Dick and Harris (2003).

## ABOUT MIMO OFDM

The general transceiver structure of MIMO OFDM is presented in Fig. 1. The system consists of N transmitter antennas and M receiver antennas. According to Alamouti (1998) and Kirubanandasarathy *et al.* (2010), the cyclic prefix is assumed to be a longer than the channel delay spread. The OFDM signal for each antenna is obtained by using IFFT and can be detected by Fast Fourier Transform (FFT).

OFDM is a multi-carrier system where data bits are encoded to multiple sub-carriers. Unlike single carrier systems, all the frequencies are sent simultaneously in time. OFDM offers several advantages over single carrier system like better multipath effect immunity, simpler channel equalization and relaxed timing acquisition constraints. But it is more susceptible to local frequency offset and radio front-end non-linearity. The above discussion is fully based on Blum *et al.* (2001); they have also analyzed the above said matter. The frequencies used in OFDM system are orthogonal. Neighboring frequencies with overlapping spectrum can therefore be used. This property is shown in the Fig. 2, where A, B, C, D and E orthogonal. This results in efficient usage of BW. The OFDM is therefore able to provide higher data rate for the

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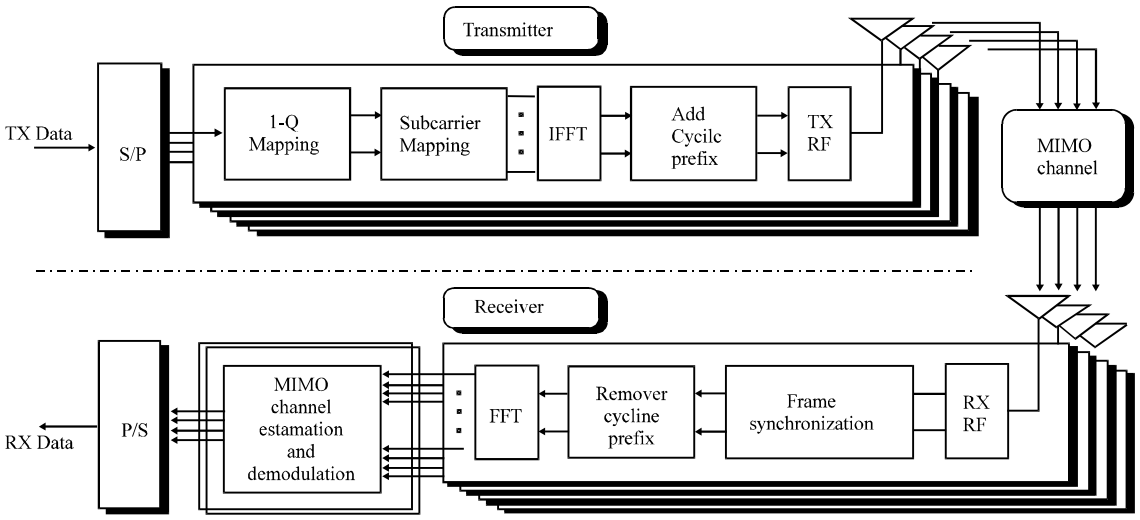


Fig. 1: Architecture for MIMO-OFDM

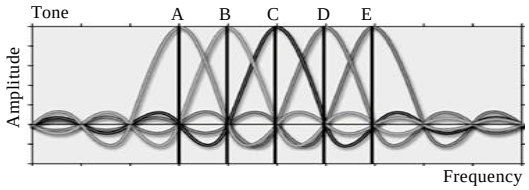


Fig. 2: OFDM wave

same BW. Terry and Heiskala (2002) also gave detailed discussion about OFDM Wireless LANs.

## PROPOSED PIPELINED ARCHITECTURE FOR MIMO-OFDM

The radix-2 multipath delay commutation (R2MDC) is one of the commutated architectures of radix-2 FFT algorithm which is used to commutate the values as fast as possible in order to process the values and to commutate the FFT inputs, the architecture shown in the Fig. 3 is consists of different blocks which must be used in the R2MDC. Kirubanandasarathy *et al.* (2010) was investigated Radix-2 pipelined streaming FFT block, which is used in the baseline MIMO-OFDM system. But we use radix-2 multipath delay commutation in the proposed system.

One of the most straightforward approaches for pipelined implementation of radix-2 FFT algorithm is Radix-2 Multi-path Delay Commutator (R2MDC) architecture. Figure 4 shows the radix-2 multipath delay commutation architecture with butterfly II structure. It is the simplest way to rearrange data for the FFT/IFFT algorithm. Becker (2002) and Han *et al.* (2005) says that the input data sequence are broken into two parallel data stream flowing forward, with correct distance between data elements entering the butterfly scheduled by proper delays. The 8-point FFT in R2MDC architecture is shown in Fig. 3. At each stage of this architecture half of the data flow is delayed via the memory (Register) and processed with the second half data stream.

The A input comes from the previous component Twiddle Factor Multipliers (TFM). The B output is fed to the next component, normally BFII. In first cycles, multiplexors direct the input data to the feedback registers until they are filled (position "0"). On next cycles, the multiplexors select the output of the adders/sub tractors (position "1"), the butterfly computes a 2-point DFT with incoming data and the data stored in the feedback registers. The detailed structure of BFI is shown in Fig. 5a.

The B input comes from the previous component, BFI. The Z output fed to the next component, normally TFM. In first cycles, multiplexors direct the input data to the feedback registers until they are filled (position "0"). On next cycles, the multiplexors select the output of the adders/sub tractors (position "1"), the butterfly computes a 2-point DFT with incoming data and the data stored in the feedback registers. The multiplication by -j involves real-imaginary swapping and sign inversion. The real-imaginary swapping is handled by the multiplexors

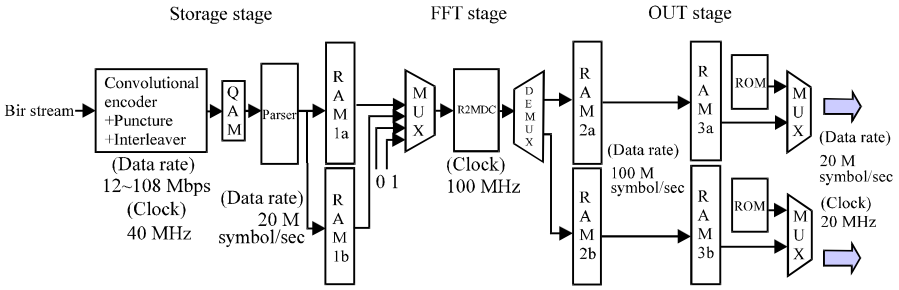


Fig. 3: Proposed FFT Architecture block

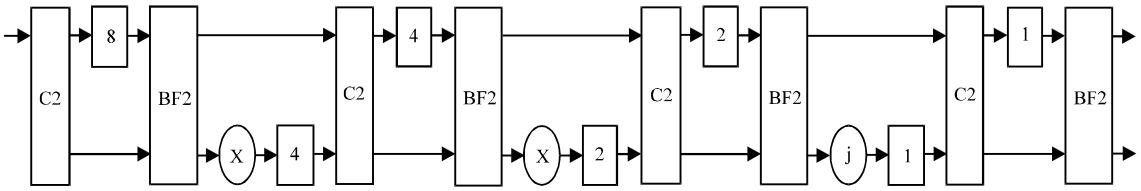


Fig. 4: Radix-2 multipath delay commutation architecture

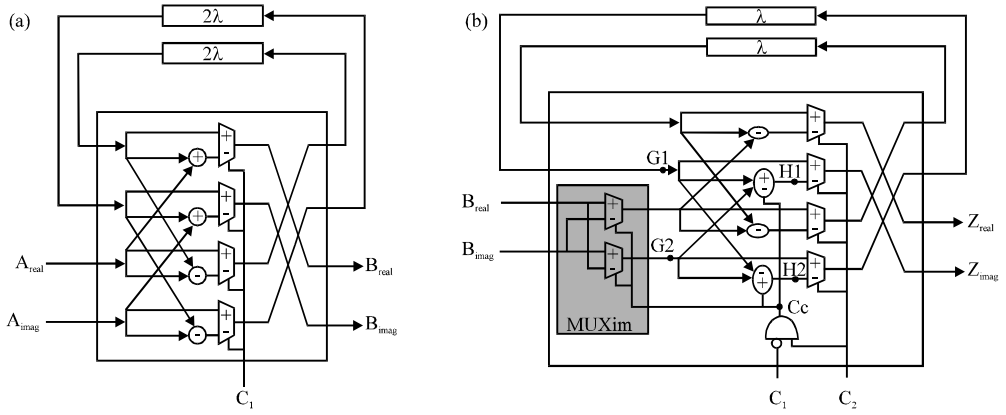


Fig. 5(a-b): (a) BFI structure and (b) BF II structure

MUX in efficiently and the sign inversion is handled by switching the adding-subtracting operations by mean of MUX. When there is a need for multiplication by -j, all multiplexors switches to position "1", the real-imaginary data are swapped and the adding-subtracting operations are switched. The detailed structure of BFI and BFII are shown in Fig. 5a and b. The adders and sub tractors in BFI and BFII are fully-pipelined and followed by divide-by-2 and rounding. The divide-by-2 is used. The algorithm used here is to commutate the radix-2 algorithm in the IFFT architecture and to replace by R2MDC architecture in order to get a low area than the existing system. Kirubanandasarathy and Karthikeyan (2012) have discussed Radix-2 pipelined streaming FFT block versus a Radix-4 FFT block without multi delay commutation.

## RESULTS

The results consists of three different types of architectures that can be implemented in the Xilinx Virtex-4 Xc4vlx25-12ff668 FPGA. We have designed all coding using Hardware Description Language (HDL). To get power, and area report, we use Xilinx ISE Design Suite 10.1 as synthesis tool and Model-Sim 6.3 c for simulation. The comparison of Radix-2 FFT and Radix-4 with Proposed R2MDC FFT is shown in the Fig. 6. The Proposed FFT gives better result than Radix-2 FFT and

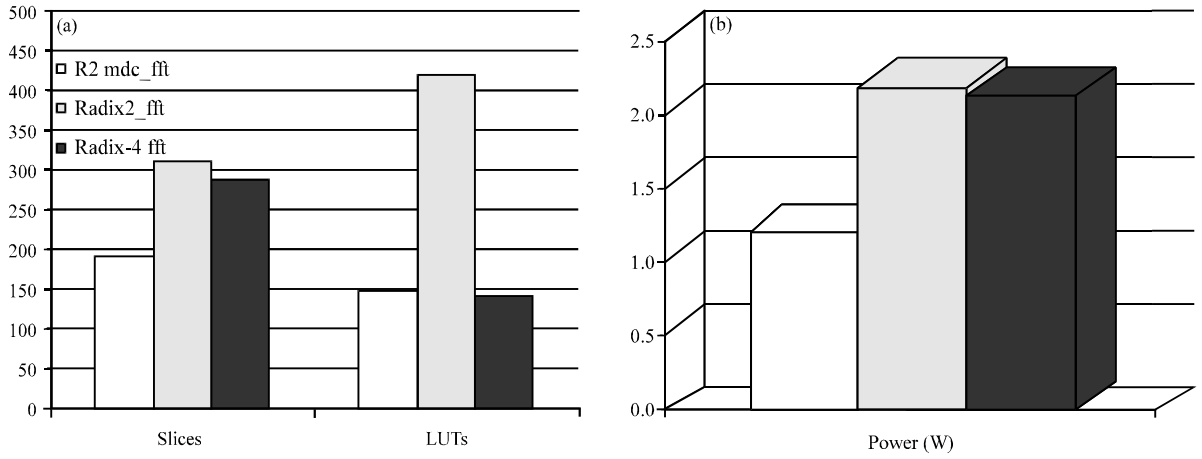


Fig. 6: Comparison results of proposed R2MDC IFFT architecture with existing radix-2 and radix-4 architecture

Radix-4 FFT in terms of area and power consumption as shown in the Fig. 6. The FPGA board has developed to verify their circuit behavior and implementation of MIMO OFDM Transceivers.

## CONCLUSION

The study concludes that the proposed R2MDC architecture is taken a low area and less power than the existing radix-2 and radix 4 algorithm architecture; the results are concluded that the proposed architecture is shows that it can be used in for low power applications such as MIMO-OFDM transceivers.

## REFERENCES

Alamouti, S.M., 1998. A simple transmit diversity technique for wireless communication. IEEE J. Selecl Areas Commun., 16: 1451-1458.

Becker, J., 2002. Configurable systems-on-chip. Proceedings of the 15th Symposium on Integrated Circuits and Systems Design, (SICSD'2002), Karlsruhe University, Germany, pp: 379-384.

Blum, R.S., Y.G. Li, J.H. Winters and Q. Yan, 2001. Improved space time coding for MIMO-OFDM wireless communications. IEEE Trans. Commun., 49: 1873-1878.

Bolcskei, H., D. Gesbert and A.J. Paulraj, 2002. On the capacity of OFDM-based spatial multiplexing systems. IEEE Trans. Commun., 50: 225-234.

Coulton, P. and D. Carline, 2004. An SDR inspired design for the FPGA implementation of 802.11a baseband system. Proceedings of the IEEE International Symposium on Consumer Electronics, September 1-3, 2004, Reading, UK., pp: 470-475.

Dick, C. and F. Harris, 2003. FPGA implementation of an OFDM PHY. Proceedings of the 37th Asilomar Conference on Signals, Systems and Computers, Volume 1, November 9-12, 2003, Pacific Grove, CA, USA., pp: 905-909.

Han, W., T. Arslan, A.T. Erdogan and M. Hasan, 2005. Multiplier-less based parallel-pipelined FFT architectures for wireless communication applications. Proceedings of the IEEE International Conference on Acoustics, Speech and Signal Processing, Volume 5, March 18-23, 2005, Edinburgh University, UK., pp: v/45-v/48.

Jongren, G., M. Skoglund and B. Ottersten, 2002. Combining beam forming and orthogonal space-time block coding. IEEE Trans. Inform. Theory, 48: 611-627.

Kirubanandasarathy, N. and K. Karthikeyan, 2012. VLSI design and implementation of MIMO OFDM system for wireless communication. Eur. J. Sci. Res., 73: 269-277.

Kirubanandasarathy, N., K. Karthikeyan and K. Thirunadanasikamani, 2010. VLSI Design of Mixed Radix FFT for MIMO OFDM In the wireless communication. Proceedings of the IEEE International Conference on Communication Computing Control Technologies, October 7-9, 2010, Ramanathapuram, Indian, pp: 98-102.

Terry, J. and J. Heiskala, 2002. OFDM Wireless LANs: A Theoretical and Practical Guide. 2nd Edn., Sams Publishing, USA., ISBN: 13-9780672321573, Pages: 315.