Journal of Applied Sciences

ISSN 1812-5654

science alert

ANSInet
an open access publisher
http://ansinet.com

Journal of Applied Sciences 13 (21): 4393-4398, 2013
ISSN 1812-5654 / DOI: 10.3923/jas.2013.4393.4398

Design and Application of USB 3.0 on UM-BUS Test System

Chunliang Wang, Weigong Zhang, Ya Li and Zhe Deng
College of Information Engineering, Capital Normal University, Beijing, China

Abstract: This article is based on the UM-BUS which is a high-speed dynamic reconfigurable serial Bus, design the test system and application a USB 3.0 port. The test system can collect the data in the case does not affect the transmission characteristics under un-filter monitor function; inject the fault mechanism according to bus protocol specially use the failure test mode; at last through the USB 3.0 or PCI-E realize the high-speed transmission with computer or relation facilities. In addition, the design also comes with a storage function, the overall data acquisition and storage process in the case of without relying on computer.

Key words: UM-BUS, USB 3.0, FPGA, FX3014

INTRODUCTION

With embedded systems developed and widely used in the national economy, aerospace, military, industrial control, transportation and other fields, increasing the requirements high reliability and fail-safe in embedded systems. To guarantee the high reliability of the bus system, bus testing is essential. The test information processing board is a critical hardware on the systemwhich is used to complete bus information integrated, resource sharing, data processing, task coordination and fault-tolerant reconfigurable. However, these traditional methods on record of the data transfer process between the bus and the capacity for failure reproduction and analytical processing capacity is weak; what's more, these methods are not perfect for fault injection (Malekpour, 2006).

Typically dealing with it by redundant, UM (Unite Module)-BUS is a high-speed computer internal bus with the highly reliable capabilities of failure self-healing. The test system must have a strong ability to deal with a storage of high-speed data that will be a big challenge both to the process part and the data channel. To be sure the design can satisfied the demand, chose the Virtex-LX85T as the data process core and USB 3.0 as the main path with PCI-E to be alternate (Li and Wang, 2011). With the function of test board FPGA get the data which is passing on the UM-BUS, then it can send the processed data out. The test board either contact with PC or other storage with USB 3.0 cable or PCI-E (Niu, 2011). What's more, the test system can work without any other controller, thus it can storage the data directly to the CF card. From the following Fig. 1 we can know the data flow of the entirety test procedure.

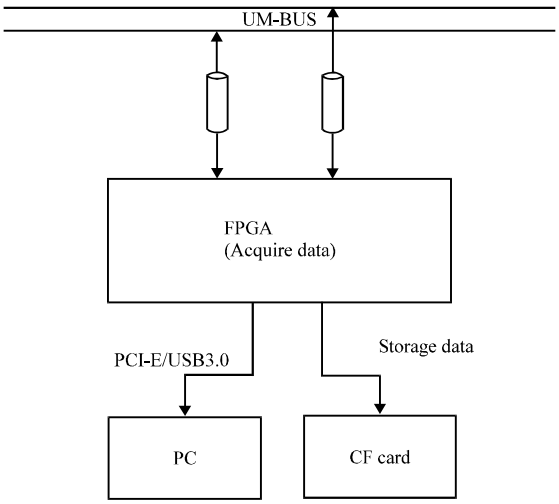

Fig. 1: Topology of the test system

OVERALL DESIGN OF TEST SYSTEM WITH USB 3.0

Based on SOC technology which is used to specialized satisfy test demand for UM-Bus, design the information process platform. The main functions the platform contains affairs library, Bus task library and test stimulus generation functional modeling part. Its core is lead the concept of transaction into the verification process, abstract the pin level to a specified high levelwhich can effectively support the development and reuse of the test platform. The establishment of the bus task library treat measured bus object to complete the description of the basic functions of abstraction and sequential logic (Zhen, 2011). Completion of the test on the SOC bus timing stage data acquisition, by the output

Corresponding Author: Weigong Zhang, College of Information Engineering, Capital Normal University, Beijing, China

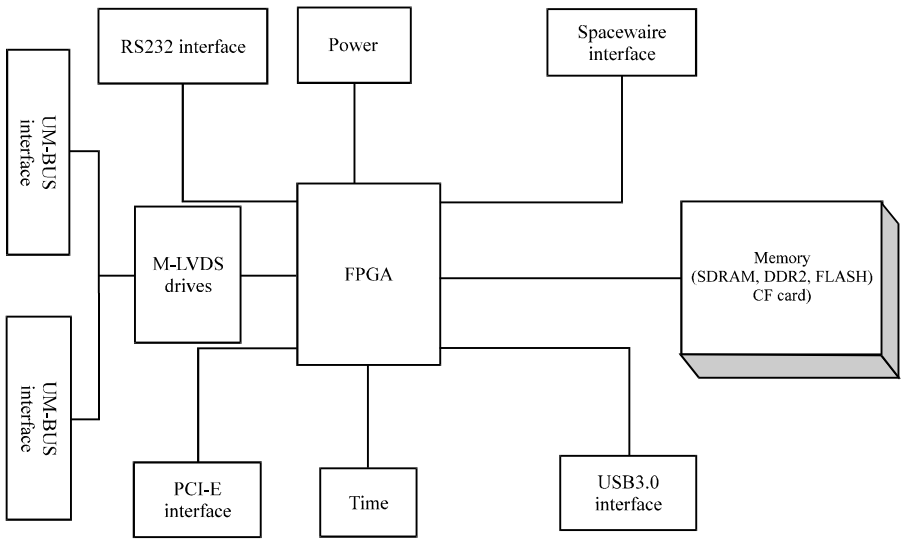

Fig. 2: Schematic diagram of the test platform

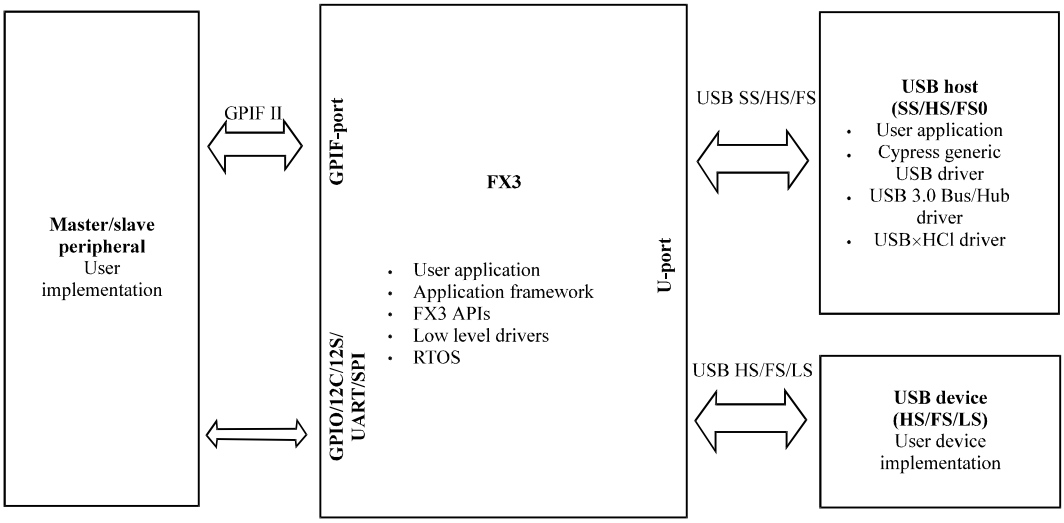

Fig. 3: Overview of the FX3 firmware system

detection module will transfer data to the computer prepare the further analysis by a bus function model. The following Fig. 2 give us the structure of the test data processing platform.

Above all, the system can real-time acquisition, processing, monitoring and recording bus signals on UM-BUS, assist in the completion of post-hoc analysis and signal simulation, speed up bus error positioning, shorten the data processing cycle, reduce the number of experiments and experimental costs. The following Fig. 3 give us the structure of the test information process platform.

The system using EZ-USB-F3 as USB 3.0 host interface chip which is produced by Cypress. It is the next generation USB 3.0 peripheral controller providing high integrated and flexible features that enable developers to add USB 3.0 to our system. This chip has a fully configurable, parallel general programmable Interface called GPIF II which can connect to any processor just like FPGA. The general programmable Interface GPIF II is an enhanced version of the GPIF in FX2LP, Cypress's flagship USB 2.0 product. It provides easy and glue less connectivity to popular interfaces such as asynchronous SRAM, asynchronous and synchronous Address Data Multiplexed interface, parallel ATA and so on (Cypress, 2011).

Overall the system can be divided into three parts

Un-filter monitor function design: First, the system can be used as un-filter monitor of the UM-BUS system,

collect information between the transmitting and receiving terminal. Un-filter monitor function including the meaning of two levels: One is that it can read all the data passing the UM-BUS which is not directed against one or several terminal devices, nor for one or several bus command, but including all types of commands and responses to the commands; the other is the transmission data on the bus, due to various factors, not only have the correct line UM-BUS transfer predetermined data, including some does not comply with the provisions transfer datawhich is considered erroneous data. Un-filter on the other hand, refers to, regardless of the data is correct or not, the system will get the processing data and storage them.

The FPGA function module into the signal converter when the system operates this mode. The data on the UM-BUS driven by M_LVDS processed by the FPGA and finally transfer to the PC for storage. To meet the needs, directly storage from the UM-BUS communication, great amount high-speed test data need the system to transfer. So select the two high-speed interface that is, USB 3.0 and PCI-E interface design can be connected with the computer to be able to complete the demand when transmission. To be able to make the test system can meet the requirement of some special test situations without computer, acquisition and storage data to the CF card (Heidi *et al*., 2006).

Multifunctional design: The board can be used to completed the receive and send terminal function at the same time, that is, at the same time to achieve a combination of bus terminal and test the data acquisition system, the completion of the bus filter data acquisition system front-end functionality.

When the system work in this module, the hardware settings each terminal has its own unique terminal ID and Synchronous transmission of real-time access to the UM-BUS network, transmission real-time data of on the bus controller and the receiving end to no filter receiver module synchronization. What's more, the board prepared the Space wire and RS232 Interface also, so it can spread the test function to more instances.

Fault injection mechanism: The platform can implement the UM-BUS test system fault generation mode. According to dynamically reconfigurable high reliability for UM-BUS, how we can better achieve fault injection will be a huge challenge. The system is directly connected in series to the bus system between the receiving and transmitting terminal does not interfere with the actual communication which can be realized in accordance with the predetermined program fault injection function, verify the compliance of the UM-BUS for completion of the specific fault responses with intended design.

HARDWARE DESIGN AND PERFORMANCE ADJUSTMENT

To successfully add this high throughput pipe to the system, the design must take care many details. We should apply techniques for high-speed to systems that use the EZ-USB FX3 device. Because of the packaging and high performance Characteristics of the device and follow the guidelines for trace width, stack up and other layout considerations to make sure the system will perform as expected.

The hardware platform design includes mainly includes three parts, the first is the master power supplywhich can supply for the entire test system and be able to meet the requirements of each system module voltage conversion; secondly, the design of the storage section, take into account the real-time processing of large amounts of data but also storage these data directly, cache design is required to complete the intermediate data buffer; Finally the board interfaces which are able to complete a variety of different needs and supporting with kinds of interface circuits, so you can make the test board to multifunction.

Structure design with FX3: USB 3.0 also known as super speed data bus, its transmission speed can reach 5 Gbps bandwidth up to 600 MB/S(USB 3.0, 2008). This platform uses Virtex5-LX85T FPGA as the core. It will control the data flow and chose the function models and operate some calculate. We chose the FX3 series CYUSB3014 chip from Cypress as the USB 3.0 controller and the interface complies with USB 3.0 specification (Cypress, 2013). The lines between the FPGA and FX3 chip and chip with external IO with equilong design to ensure reliable transmission of high-speed signals. The following schematic shows the application of the USB on the test system (Fig. 4).

PCB design of USB 3.0: High-speed USB operates at 480 Mbps with 400 mV signaling. For backwards compatibility, devices that are high-speed capable must also be able to communicate with full-speed USB products at 12 Mbps with 3.3 V signaling. High-speed USB hubs are also required to talk to low-speed products at 1.5 Mbps. Designing printed circuit boards that meet these requirements can be challenging. PCB design influences USB signal quality test results more than any other factor. Here addresses five key areas of high-speed USB PCB design and layout: Controlled Differential Impedance; USB Signals; Power and Ground; Crystal or Oscillator; Troubleshooting.

Controlled differential impedance of the D+ and D- traces is important in USB PCB design. The impedance of the D+ and D- traces affect signal eye

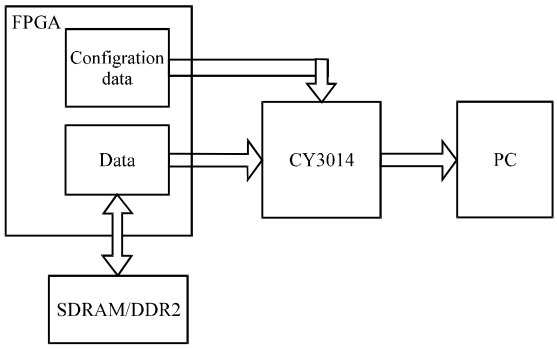

Fig. 4: Schematic diagram of USB application

Table 1: USB signals

Signal	Description
VBUS	Device power, +5 V, 500 mA (max)
D+ and D-	Data signals, mostly differential
GND	Ground return for VBUS
SHIELD	Cable shielding and receptacle housing

pattern, end-of-packet (EOP) width, jitter and crossover voltage measurements. It is important to understand the underlying theory of differential impedance to achieve a 90 Ù±10% impedance. There are five USB signals: VBUS, D+, D-, GND and SHIELD. Their functions are shown in the following Table 1 (Cypress, 2012).

The proper Vcc and GND planes are required for high-speed USB PCB design. They can reduce jitter on USB signals and help minimize susceptibility to EMI and RFI. A crystal and a oscillator provides the reference clock for the Cypress high-speed USB chip. It is important to provide a clean signal to the USB chip and to not interfere with other high-speed signals, like D+ and D- (Cypress, 2012).

The Printed Circuit Board (PCB) as the carrier and the signal of the electronic device and data transmission medium, the station has an important position in the vast majority of electronic products. The logical structure is correct, compact and ideal for high-speed signal transmission function of the PCB prototype electronic products and validation testing completed quality and speed have played a very important role.

Mentor EE toolswhich is Mentor Graphics introduced advanced PCB design tools based on the Windows interface, identified cable smooth software by engineers, it contains a very powerful automatic routing tool Expedition which is a very professional wiring rules, known as the best route tools. Dxdesigner introduced by Mentor Graphics schematic entry tool, its powerful, user-friendly, can support a variety of PCB Layout tools. The design uses the Mentor software Dxdesigner and Expedition complete schematic and PCB layout. The following Fig. 5 shows the layout of USB crucial part.

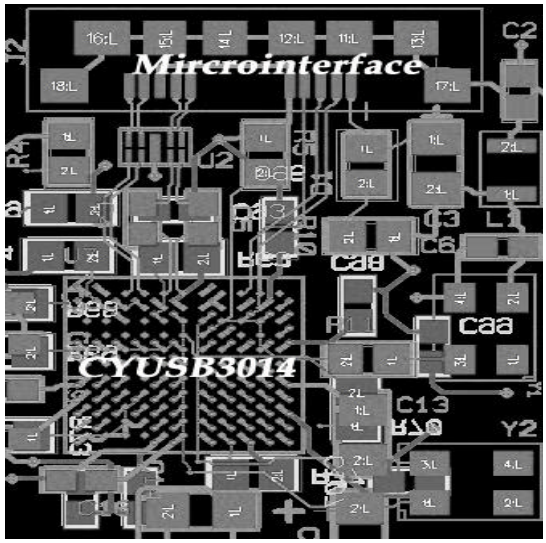

Fig. 5: Layout of the USB design

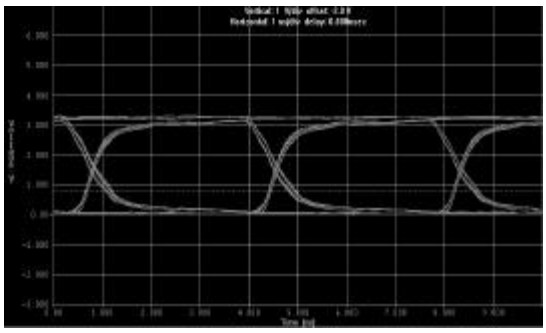

Fig. 6: Eye diagram of high-speed signal

Anylsis of signals: One key measurement of USB data signal quality is the eye pattern. The eye pattern is a representation of USB signaling that provides minimum and maximum voltage levels as well as signal jitter. Using signal integrity tool analysis the board after the layout is necessary to ensure the integrity of the signal and shorten the design cycle. Adopt the Mentor company's Hyperlynx7.1 simulation software wiring simulation tools of this article, analysis the crucial differential transmission lines to verify whether them can meet the communication requirements of the signal (USB 3.0, 2008). The following Fig. 6 is the eye diagram of high-speed signaling as measured on the USB component.

PERFORMANCE OF USB 3.0

Using the UM-BUS Test System Software test the performance of the USB interface on the platform. First of

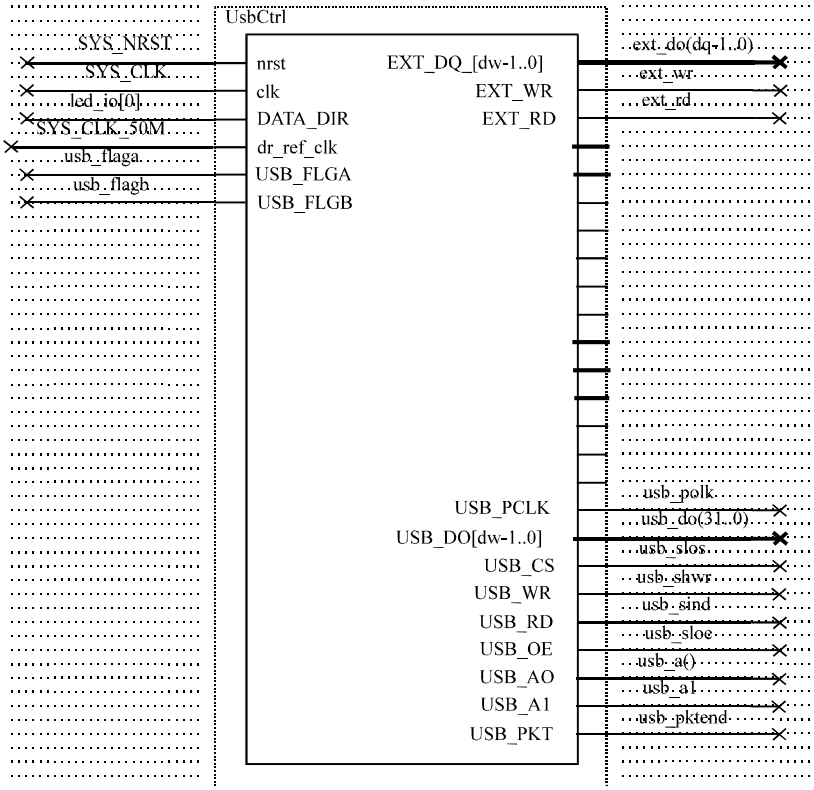

Fig. 7: Package of the test program

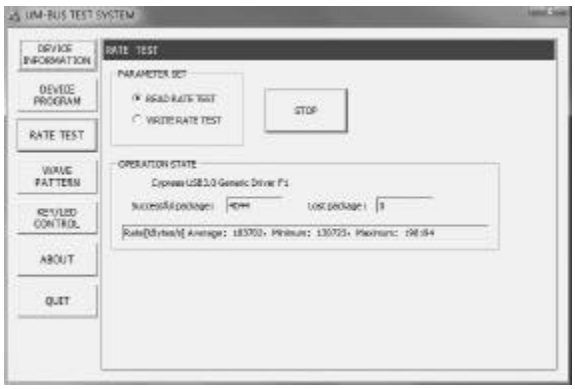

Fig. 8: Speed test result

all, we must set the parameter of the chip and download to the CYSUSB3014 by USB mode (Cypress, 2011). And then, we set two mode of the test. One is that transfer data from the FPGA to PC: the FPGA generate test data (32-bit data, the high 16-bits set 0, in the higher 4 bits of low 16-bits set cyclic changes between 0-15, the other 12 bits set cycle between 0-4095change), to generate test data, the data transfer process is Data Generate--FIFO--FX3 Chip-USB 3.0 Interface-PC. The purpose of testing, we can write external data to FIFO as the test data, external data is uploaded to the PC. Data transfer control from PC to FPGA: FPGA read the data from FX3 interface and then transmitted directly to the external interface (Fig. 7).

After the download the relation program both chip and FPGA, Start the test course. We can get the device information, read and write speed both from FPGA or PC, the number of package of success and lost during the transferring, even more the wave form of the channel. The following figure shows the result of the speed test (Fig. 8).

CONCLUSION

In this study, design a bus test system with USB 3.0 to the high speed dynamically reconfigurable serial buswhich are able to complete the high-speed data transmission and real-time storage, fault injection and to be able to as the bus data transmission, receiving and data collection terminals at the same time. Completed by Mentor Graphics' high-end PCB design software EE development. Simulation by Hyperlynx for high-speed signal lines, designed to achieve the scheduled communication design requirements. This study analyzes the structure of the entire test system design and complete hardware platform. The application of USB 3.0 give a great help on the data transfer and complete the expect requirement. These works will have a guiding significance for the completion of the entire test system and high-speed bus test systems engineering practice.

ACKNOWLEDGMENTS

The authors wish to thank Ya Li, Zhe Deng and Professor Weigong Zhang. This work was supported in part by the National Natural Science Foundation, No. 61170009; Beijing Natural Science Foundation, No. 4132016; the Project of Construction of Innovative Teams and Teacher Career Development for Universities and Colleges Under Beijing Municipality.

REFERENCES

Cypress, 2011. EZ-USB® FX3 superspeed usb controller. http://classes.engineering.wustl.edu/cse462/images/a/a2/FX3_Datasheet.pdf

Cypress, 2012. AN1168-high-speed USB PCB layout recommendations, Cypress. http://www.cypress.com/?rID=12982.

Cypress, 2013. AN70707-EZ-USB® FX3™/FX3S™ hardware design guidelines and schematic checklist. Cypress, http://www.cypress.com/?rID=53203.

Heidi, F., M. Geruso and M. Wetzel, 2006. A survey of high speed bus technologies for data movement in ATE systems. Proceedings of the IEEE System Readiness Tecnnology Conference on Autotestcon, September 18-21, 2006, Anaheim, CA., pp: 655-657.

Li, J. and J.W. Wang, 2011. PCI express interface design and verification based on Spartan-6 FPGA. Proceedings of the 12th IEEE International Conference on Communication Technology, November 11-14 2010, Nanjing, pp: 305-307.

Malekpour, M.R., 2006. A byzantine-fault tolerant self-stabilizing protocol for distributed clock synchronization systems. Report NASA/TM-2006-214322, NASA Langley Research Center, Hampton, VA 23681, USA. http://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20070000531_2006259417.pdf

Niu, Z., 2011. The design of the monitoring system for the 1553B bus on FPGA. Master's Thesis, University of North.

USB 3.0, 2008. Universal Serial Bus 3.0 specification, Revision 1.0. November 12, 2008. http://www.gaw.ru/pdf/interface/usb/USB%203%200_english.pdf

Zhen, X., 2011. A design of PCI target interface based on FPGA. Adv. Mater. Res., 186: 342-347.