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CMOS VLSI Implementation of Adders with Low Leakage Power

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Abstract: Due to the semiconductor technology revolution, portable consumer electronic products are made with more features. The power dissipation factor is important since those systems are built with plenty of transistors. As the sizes of the transistors shrink and the technology scales, leakage current increases considerably thereby dominates dynamic power. Since most of the leakage currents like gate channel leakage, diode junction reverse-biased current and sub-threshold channel leakage are process dependent, sub-threshold leakage alone is concentrated here as a major concern. This study provides performance comparison analysis of a single-bit adder using sleep, stack, sleepy stack and sleepy keeper approaches. To achieve power reduction during the sleep or standby mode, the operating supply voltage can be disconnected to the rest of the circuit with an additional sleepy transistor. A leakage power reduction can also be achived by stack method in which the transistor length can be increased or by increasing the width of the corresponding transistors. A dynamic power reduction will also be achieved by implementing methods like clock gating, multiple threshold CMOS (Complementary Metal-Oxide-Semiconductor) and dynamic threshold CMOS, etc. A small amount of power reduction in a full adder will result a dramatic change of overall power of the system. A sleepy method provide a better leakage power reduction with 12.486 μW as compared to other techniques. All the results can be verified using Electronic Design Automation (EDA) tools like DSCH (Digital Schematic) and Microwind layout editor software tool. Results show that sleepy stack approach provide better leakage reduction at the cost of area.

Key words: Adders, chip technology, layout tool, leakage power, sleepy stack

INTRODUCTION

High speed design is not an issue nowadays like past decades. Since the technology shrinks, device density becomes a huge factor in turn the power involved in the design increases exponentially (Anis and Elmasry, 2003; Peiravi *et al*., 2009). The need for reducing power dissipation in electronic systems varies from application to application. In mobile phones and personal digital assistants i.e., battery operated portable systems, power dissipation must be reduced because of the use of limited backup time batteries. Also due to the expensive packaging technique and cooling management system, circuit designers are looking for optimized algorithms to reduce the power (Kumar *et al*., 2012; Hu *et al*., 2011).

In CMOS VLSI design, the speed or performance was the major issue during the past decades. But once the systems are built using millions and millions of transistors, the power dissipation is become a crucial factor. Due to the rise in temperature, reliability of an electronic device decreases. So, timing i.e., performance degrades with temperature. Also when the technology shrinks further and further, leakage current become dominant compared to switching current (Keating *et al*., 2007; Vigneswaran *et al*., 2006).

The two broad categories of power estimation involve switching power and static power. The first one is caused by switching activities of circuits. Logical states are important rather than the switching activities in the second one. Current may flow even via the OFF transistor. Because of leakage in CMOS devices, static power occurs (Keating *et al*., 2007; Reddy, 2011).

Since the static or dc power act as a important source of energy dissipation in the form of leakage due gate and sub-threshold channel leakage. Because of weak charge inversion, a minimum amount of current flows even through normally OFF transistor, is known as sub-threshold leakage. When electrons tunnel from the poly-silicon to the bulk via thin silicon dioxide, the gate leakage dominates (Priya *et al*., 2012).

A main objective of this work to implement novel techniques to reduce the static power. The importance of leakage power is analyzed as compared to the dynamic power of CMOS logic circuits. This work is implemented with the help of Microwind layout editor and Digital Schematic (DSCH) computer aided design tools.

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SOURCES OF STATIC POWER DISSIPATION

Leakage current in a CMOS device is occurred by four as shown in Fig. 1. During the weak inversion region, the drain to current flows which is known as sub-threshold leakage. Due to the thinnest oxide, the current flows from poly-silicon to the bulk is called as gate leakage. Due to the high potential in the MOSFET drain because of large VDG, the current flows from the drain to the bulk, is known as gate induced drain leakage. The current which flows from drain to the body due to the PN junction reverse biased, is known as reverse bias junction leakage.

Even though the transistor is turned off, a sub-threshold leakage play a role and leaks some current. Sub-threshold current, I_{sub} is given by a good approximation as Eq. 1:

$$I_{sub} = \mu C_{ox} (W/L) V_{th}^{2} e^{(Vgs-Vt/n\,Vth)} \quad (1)$$

where, μ is the electron mobility, W is the width of the transistor, L is the length of the transistor, V_t is the threshold voltage, V_{gs} is the gate-to-source voltage and V_{th} is the thermal voltage. By varying the length and width of the transistors, one can prevent the static power problem which could be a designer's choice. Because, the other parameters involved here are mainly dependent on fabrication.

There are many methods to minimize the leakage current. A large threshold voltage transistors are used when there is no critical path and lower threshold transistors can be used when the performance is the main constraint. The above one is referred as Multi-threshold CMOS (MTCMOS) (Vigneswaran and Reddy, 2006). By blocking the power supply to a specific block which does not contribute to the performance of the system, the much power must be saved. The second one is being referred as power gating which is often used in the design.

Variable Threshold CMOS (VTCMOS) is another method in which the reverse bias is connected to the bulk to reduce ($V_{gs} - V_{th}$), thereby V_{th} is effectively increased which helps to reduce the leakage power. If we place one transistor on the top of an another, the source-to-body potential for the top one may be raised and the threshold voltage raised, in turn the current becomes down. This method is referred as stack effect, or self reverse bias.

SLEEPY AND STACK APPROACHES

First, a conventional CMOS approach is implemented as shown in Fig. 2. The circuit is more compact and has high noise margin. Ideally, there is no static power

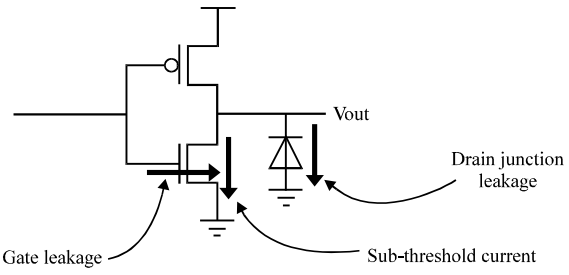

Fig. 1: Sources of static power dissipation

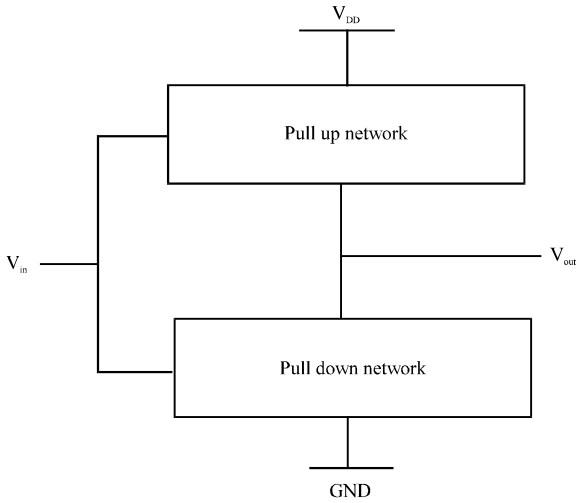

Fig. 2: Standard configuration of a CMOS complementary gate

dissipation. Since, the technology shrinks current flows through OFF transistor which is known as a leakage current. The total leakage current becomes a large if the number of transistors are more in a circuit. The total leakage power, P_{leak} can be expressed as a multiplication of leakage current, I_{leak} and the operating supply voltage, V_{dd} as in Eq. 2:

$$P_{leak} = I_{leak} \times V_{dd} \quad (2)$$

Transistor sizing is the best possible solution to reduce the leakage power but at the cost of performance. So, we try with other techniques which will be more efficient than the transistor sizing approach.

Sleepy approach: In between the pull-up network and the power supply, the PMOS transistor is wired. Similarly, in between the ground and the pull-down network, the NMOS transistor is wired (Singh *et al*., 2007) which is in Fig. 3. The leakage power can be reduced effectively by

disconnecting the power supply while in the sleep mode. The problem here is the output data after sleep mode may float. So, additional circuitries like data retention portion may be needed to retrieve back the data.

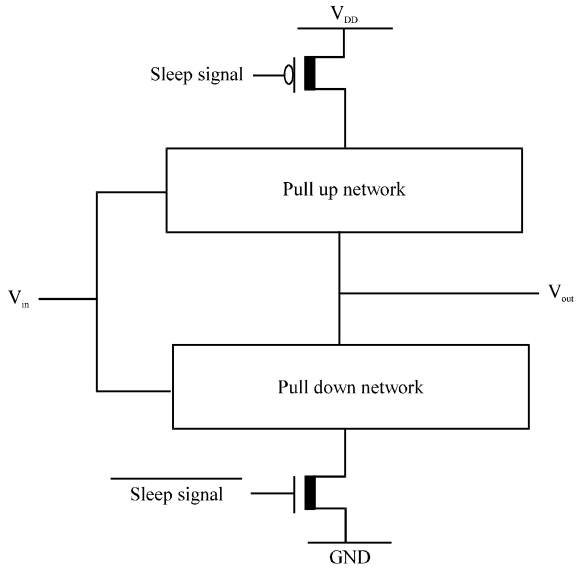

Fig. 3: Leakage power reduction using sleepy approach

Stack approach: In a circuit, all NMOS and PMOS transistors are divided and stacked into two half width size transistors as shown in Fig. 4. So that, due to body effect, the source-to-body potential raises. Thereby, threshold voltage of transistor is increased, in effect the leakage current reduced effectively at the cost of more area and performance degradation (Narendra *et al*., 2004; Khouri and Jha, 2002).

Sleepy stack approach: Both sleep and stack concepts are combined to reduce the leakage power, So that, this one has the advantages of both. Simulation results show that more area is needed for this design which are discussed in the next section with full adder.

Sleepy keeper approach: An NMOS transistor with very high threshold is connected in parallel with the sleep PMOS transistor in a pull-up network and a PMOS transistor with high threshold is connected parallel along with a sleep NMOS transistor in a pull-down topology as in Fig. 5. The present state of the circuit can be retained while in sleep mode and also reduces sub-threshold leakage power significantly.

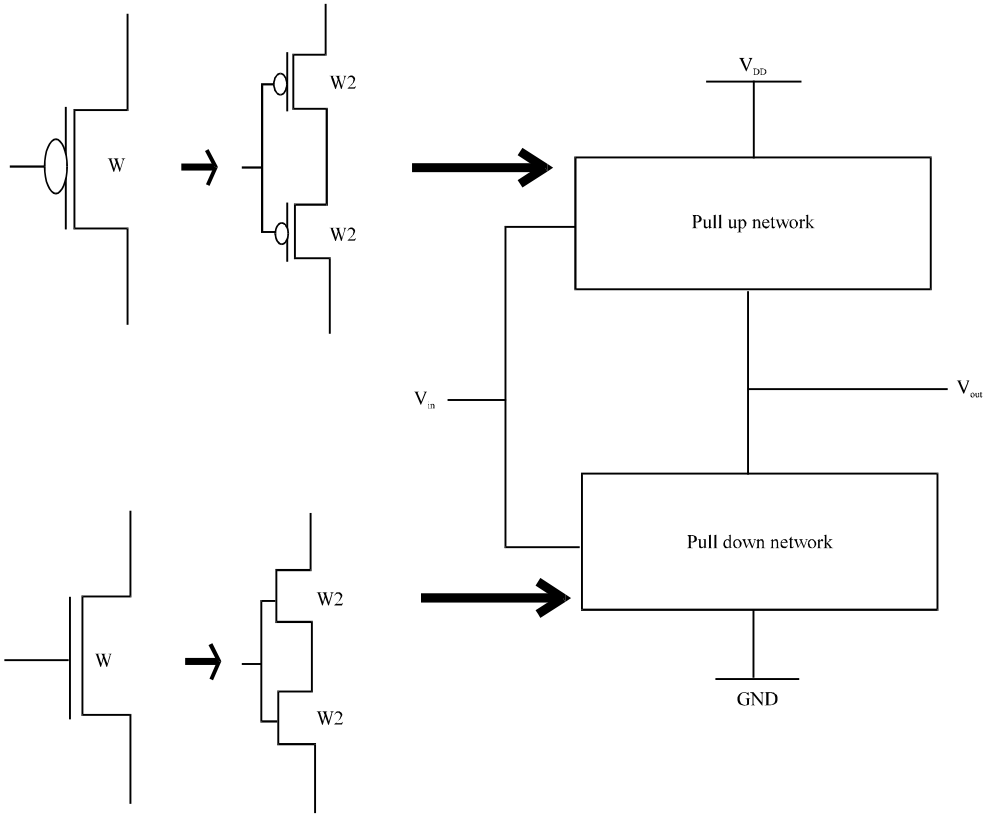

Fig. 4: Leakage power reduction using stack approach

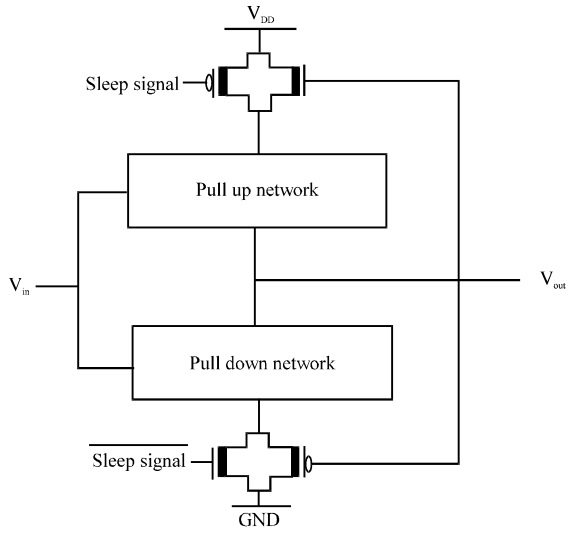

Fig. 5: Leakage power reduction using sleepy keeper approach

Stack keeper and sleepy stack keeper approaches: Similar technique can be applied to the stack circuit style as well as sleepy stack style. Since these approaches occupy more area, we are not presenting these experimental results.

EXPERIMENTS WITH FULL ADDER-SCHEMATIC DESIGNS

All the mentioned previous approaches are applied to a single-bit full adder using Microwind/DSCH CAD tool. For the logic design and to verify the functionality, DSCH tool is used here. A hierarchical circuits can be build based on primitives and simulated. To design and simulate a circuit at layout level, Microwind tool is used. This tool produces results like power dissipation, area, propagation delay and functionality verification.

Figure 6 shows that the simulation result of functionality verification for the full adder. Figure 7 shows that the full adder schematic design using Sleepy Stack approach and Sleepy Keeper approach. Figure 8 shows that the simulation result of functionality verification for the full adder.

Experimental results with layout: Automatic layouts of all the designs are generated by Microwind CAD tool and again the functionality is verified by doing simulation on all layouts which are shown in Fig. 9-11.

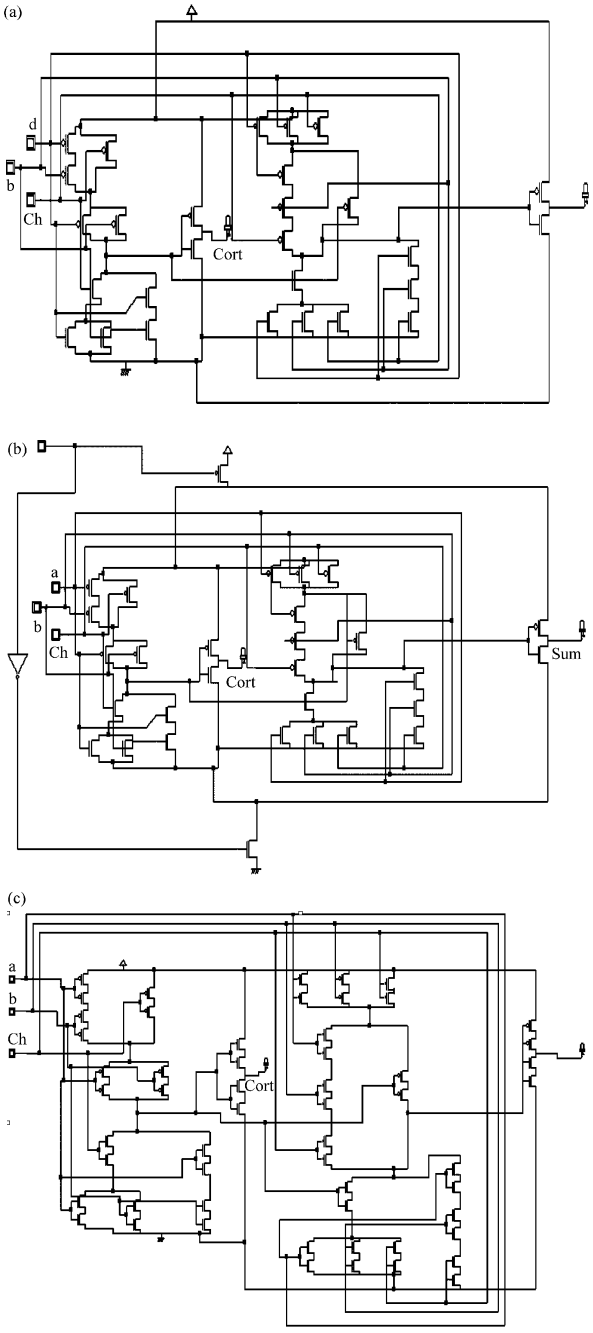

Fig. 6(a-c): Full adder using (a) Conventional CMOS (b) Sleepy approach and (c) Stack approach

SIMULATION RESULTS-POWER ANALYSIS

All the designs are verified using Microwind EDA tool using BSIM4 MOSFET model in 60 nm technology. Performance characteristics such as static (leakage) power dissipation, switching (dynamic) power dissipation, delay

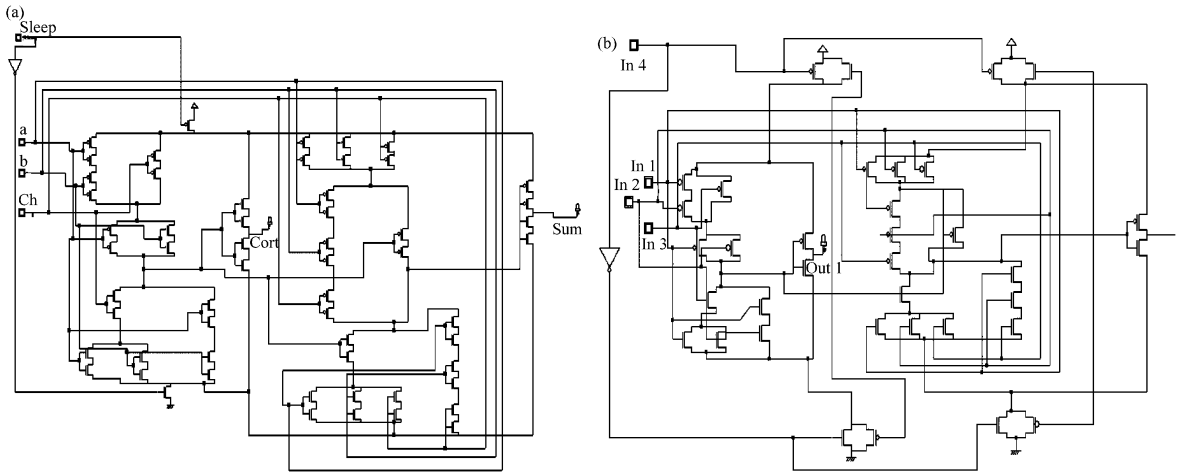

Fig. 7(a-b): Full adder using (a) Sleepy stack approach and (b) Sleepy keeper approach

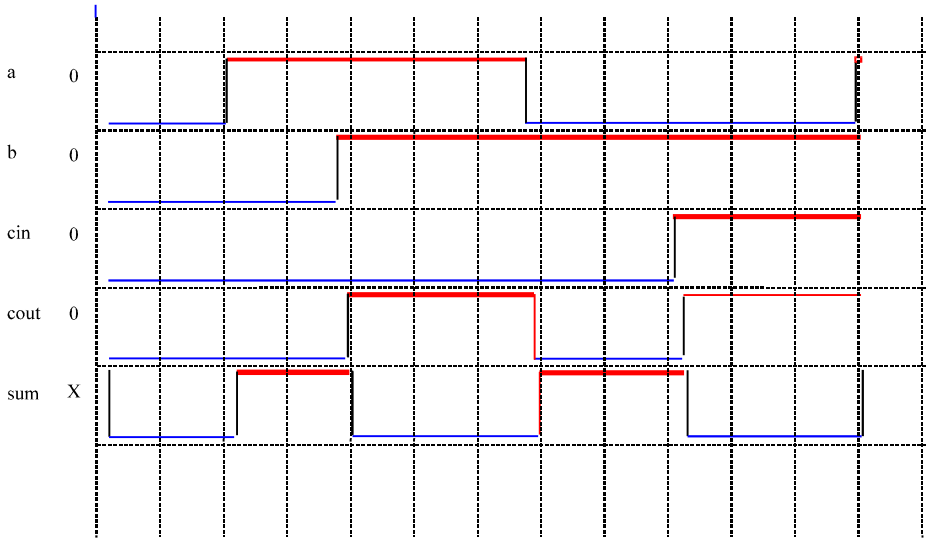

Fig. 8: Functional verification of a full adder

Table 1: Comparison of layout area using different circuit design methods

Design	No. of NMOS transistors	No. of PMOS transistors	Layout area (μm^2)
Conventional CMOS	14	14	546.7
Sleepy approach	16	16	689.8
Stack approach	28	28	1083.7
Sleepy stack	30	30	1313.9
Sleepy keeper	17	17	723.4

(propagation) and area of layout are observed. Since we focus only on static power, dynamic power dissipation results are not provided here. Selection of foundry also can be made by using this tool like 180, 120, 90 and 60 nm etc. But we have implemented all the designs with 60 nm process technology by not violating layout design rules.

Table 1 provide the results of number of transistors involved in each design and layout area in micro square meter. Conventional CMOS circuit occupies less area of 546.7 μm^2 as compared to other designs which is expected. Since there are more complexity in remaining design methods, they occupy more layout area. Sleepy, stack, sleepy stack and sleepy keeper approaches have 689.8, 1083.7, 1313.9 and 723.4 μm^2, respectively.

Stack based designs occupy more area and also with more delay because of many transistors involved in the design. Table 2 shows that the leakage power dissipated in each design when the operating supply voltage is 1.2 V during 10 nsec interval. It shows the Sleepy Keeper approach provide a better result since it does the data

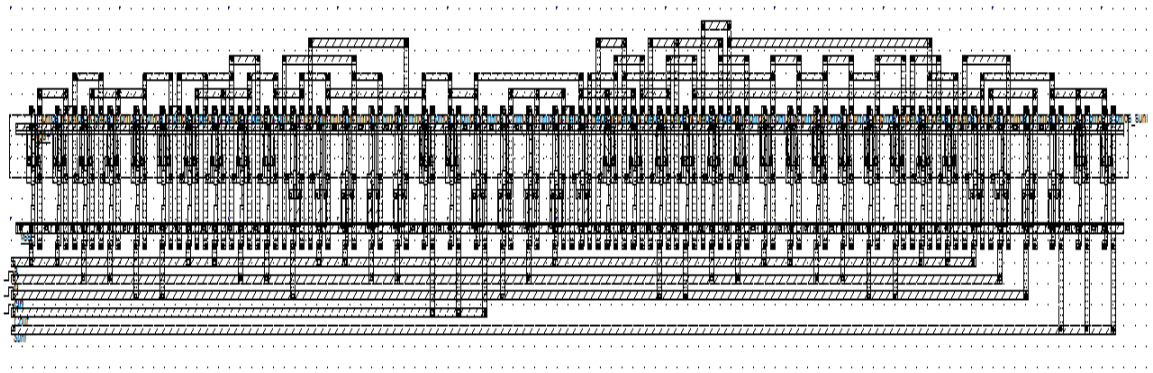

Fig. 9: A full adder layout using conventional CMOS logic style

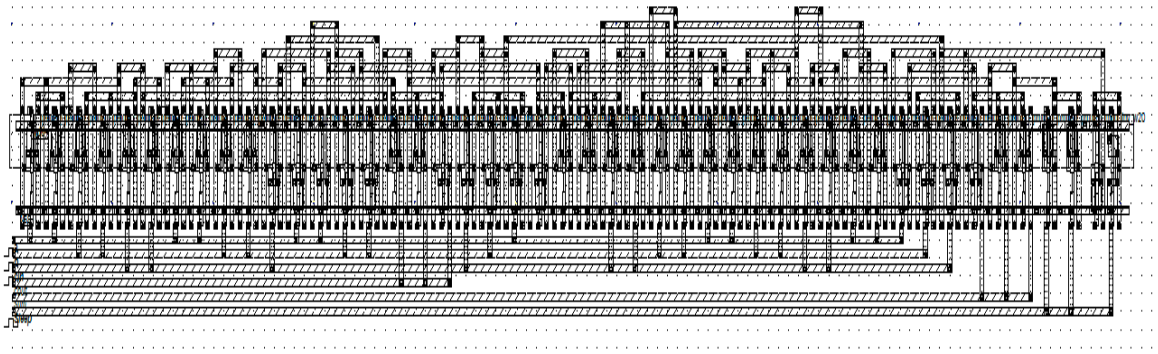

Fig. 10: A full adder layout using sleepy approach

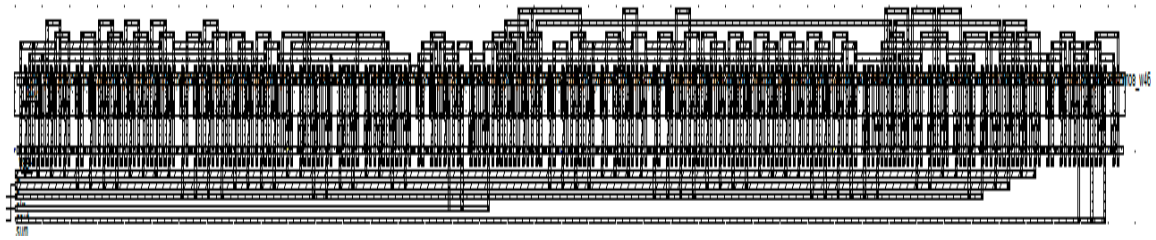

Fig. 11: A full adder layout using stack approach

Table 2: Comparison of static power dissipation using different circuit design methods

Design	Static power (μW)
Conventional CMOS	18.650
Sleepy approach	12.486
Stack approach	12.605
Sleepy stack	13.910
Sleepy keeper	12.525

retention additionally. Stack based designs are often produce more delay and kill much area in a chip. Here, the conventional CMOS style offers more static power dissipation as 18.65 μW. Sleepy technique provide the better leakage power reduction with 12.486 μW. Stack, sleepy stack and sleepy keeper techniques offer the leakage power as 12.605, 13.910 and 12.525 μW, respectively.

CONCLUSION

The trend towards mobile computing and utility of portable consumer electronic devices make the energy problem as more challenging. With the results presented above, a conclusion is made that sleepy keeper approach

is the best suited to minimize the static power in digital VLSI circuits. The main objective for designing keeper technique is to retain the logic state and also lowers the static power. In deep sub-micron technologies, these methods can be used for designing digital logic circuits. Also single and multiple threshold voltage concept can be implemented in sleepy keeper. Multi-threshold voltage designs are more powerful which satisfy both power and speed requirements for the designers. Also dynamic power reduction in all these designs presented here can be achieved.

REFERENCES

Anis, M. and M. Elmasry, 2003. Multi-Threshold CMOS Digital Circuits: Managing Leakage Power. Kluwer Academic Publishers, Norwell, MA., USA., ISBN-13: 9781402075292, Pages: 216.

Hu, J., X. Yu and J. Chen, 2011. New low-leakage flip-flops with power-gating scheme for ultra-low power systems. Inform. Technol. J., 10: 2161-2167.

Keating, M., D. Flynn, R. Aitken, A. Gibbons and K. Shi, 2007. Low Power Methodology Manual: For System-on-Chip Design. Springer Publishers, New York, USA., ISBN-13: 978-0387718187, Pages: 304.

Khouri, K.S. and N.K. Jha, 2002. Leakage power analysis and reduction during behavioral synthesis. IEEE Trans. Very Large Scale Integr. Syst., 10: 876-885.

Kumar, M., M.A. Hussain and S.K. Paul, 2012. Performance of a two input NAND gate using subthreshold leakage control techniques. J. Electron Devices, 14: 1161-1169.

Narendra, S., V. De, S. Borkar, D.A. Antoniadis and A.P. Chandrakasan, 2004. Full-chip subthreshold leakage power prediction and reduction techniques for sub-0.18-im CMOS. IEEE J. Solid-State Circuits, 39: 501-510.

Peiravi, A., F. Moradi and D.T. Wisland, 2009. Leakage tolerant, noise immune domino logic for circuit design in the ultra deep submicron CMOS technology for high fan-in gates. J. Applied Sci., 9: 392-396.

Priya, M.G., K. Baskaran, D. Krishnaveni and S. Srinivasan, 2012. A new leakage power reduction technique for CMOS VLSI circuits. J. Artif. Intell., 5: 227-232.

Reddy, N.S.S., 2011. Minimization of power dissipation in 16 bit processor using low power tecniques. Asian J. Applied Sci., 4: 657-662.

Singh, H., K. Agarwal, D. Sylvester and K.J. Nowka, 2007. Enhanced leakage reduction techniques using intermediate strength power gating. IEEE Trans. Very Large Scale Integr. Syst., 15: 1125-1224.

Vigneswaran, T. and P.S. Reddy, 2006. A novel low power 8 bit adder unit with adaptive supply voltage. J. Applied Sci., 6: 2936-2939.

Vigneswaran, T., B. Mukundhan and P.S. Reddy, 2006. A novel low power and high performance 14 transistor CMOS full adder cell. J. Applied Sci., 6: 1978-1981.