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Design and Implementation of PS-ZVS Full Bridge Converter

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Abstract: A Phase Shifted-Zero Voltage Switching (PS-ZVS) Full Bridge DC-DC Converter (FBDCC) over a wide load variation is proposed. The proposed converter is designed for high efficiency, small size and low switching stress also for no load to wide load variations. In this converter Phase Shifted Pulse Width Modulation (PS-PWM) control is used to reduce the ringing. The transformer leakage inductance is used for resonance where losses are reduced and efficiency is more. The operation of the proposed converter is simulated using Pspice software and verified on a 1 kW (kW) experimental prototype converter operating at 25 kHz with 25 V dc input.

Key words: PSZVS, FBDCC, soft switching

INTRODUCTION

High power conversion efficiency and low switching losses are the essential need for dc-dc converters used in power industries (Nayak and Reddy, 2011). The switching losses in the converters can be reduced by the following methods: Connecting snubbers, resonant converters and soft switching converters (Redl *et al*., 1991).

A conventional (ZVS) full bridge dc-dc converter exploits the seepage inductance of isolating transformer with internal capacitance of switches in lieu of attaining zero voltage switching condition. External inductors are placed in series through isolation transformer to achieve ZVS when the load varies. The following are the harmful possessions on setup of converter due to the addition of external inductance: increases duty cycle loss, introduces parasitic oscillations in the transformer's secondary side, the heat sink size increases, produces sudden rise of current, reduces the reliability and cannot suitable for no load conditions (Jain *et al*., 2002).

The new topology proposed in this work uses an ancillary transformer T_A to increase the range of ZVS. The energy stored in additional inductor L_M which is used for producing ZVS condition is reduced during no load by auxiliary transformer. The proposed method reduces the losses of duty cycle occurred in converter and switching losses of the MOSFET. The pspice simulation results of the new topology verified by the experimental results. Closed loop operation of the proposed converter for constant output voltage with wide load variation is carried out by using Pspice simulation and the results are tested with experimental setup.

MATERIALS AND METHODS

Full bridge dc-dc converter: The simulation model of conventional converter (full bridge) fabricated on pspice is bare in Fig. 1 is to study the zero voltage switching condition at no load. In conventional converter topology ZVS condition is achieved by using the switches with internal capacitance plus seepage inductance of transformer (Ayyanar and Mohan, 2001). The needed energy for achieving ZVS is given by:

$$E = 1/2\ L_M\ I_2^2 \geq 4/3\ C_{moss} Vin^2 \quad (1)$$

Where:
E = Energy needed for zero voltage switching
L_M = Magnetizing inductance
I = Inductor current
C_{moss} = MOSFET internal capacitance
Vin = Input voltage

Importance of zero voltage switching: The results of the simulation studied from conventional converter are bare in Fig. 2a, b, respectively. ZVS condition and secondary voltage of transformer with ringing effect are depicted. It can be observed from the simulation results presented that the duty cycle losses are high under no load condition and magnetizing inductance L_M is not fully charged hence it cannot achieve ZVS condition. During the off condition of the switches the load current glides over the rectifier diodes which causes an undesirable effect Parasitic ringing as shown in Fig. 2b. However, snubbers are used to minimize parasitic oscillations the switching losses become more. Dead time is introduced between switches S_1 and S_2 to avoid switching losses:

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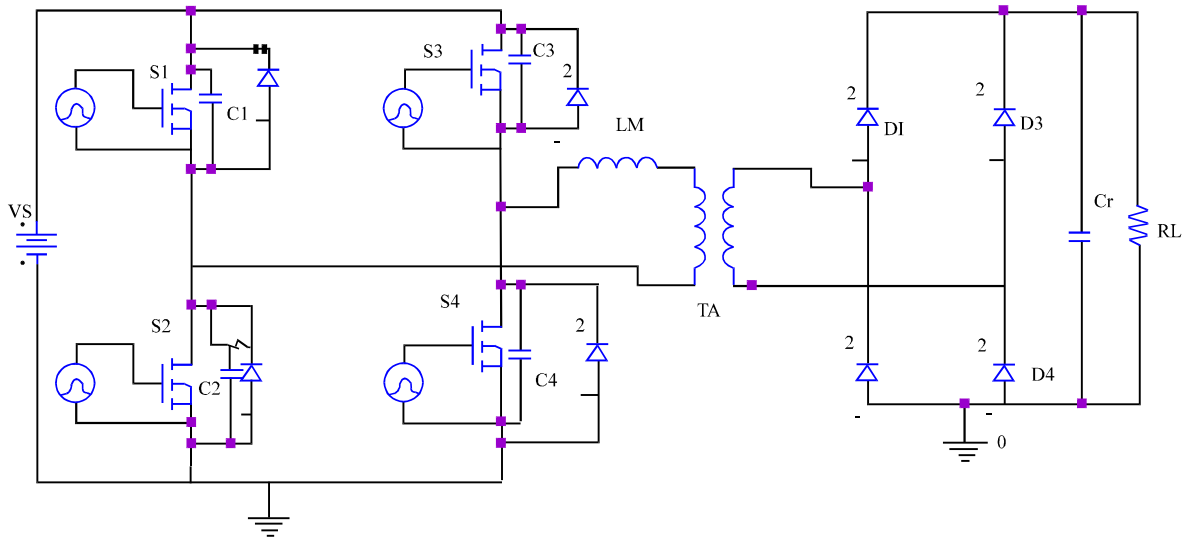


Fig. 1: Full bridge dc-dc converter

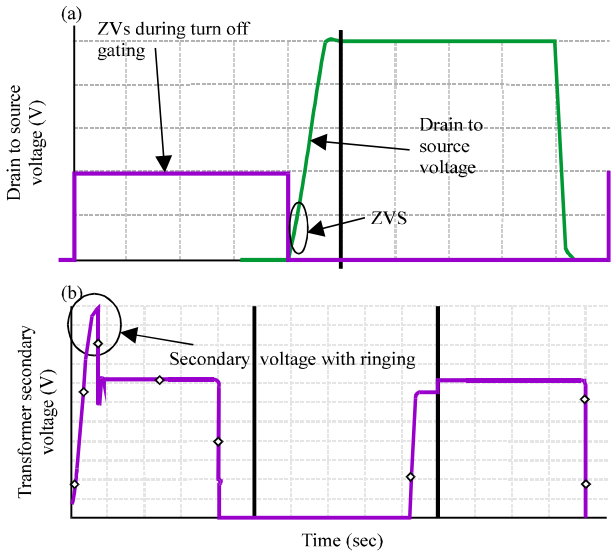


Fig. 2(a-b): (a) Zero voltage switching in the MOSFET switches used in the full bridge dc-dc converter during turn-off condition and (b) Ringing in the transformer secondary voltage for full bridge dc-dc converter

$$\text{Dead time } \delta_{tmax} = T/4 = \Pi/2vL_m.C \quad (2)$$

At no load there is a problem exist when charging and discharging the capacitors connected in parallel to the switches (S_1-S_4). Capacitor C_1isfully charged and C_2 is fully discharged during the turn of S_4. If C_4 is not fully discharged then turn on losses are high. Minimum current is required at no load to charge and discharge the capacitor:

$$I_{ch(min)} = (C_{1+}C_2)\ V_s/td_1 \quad (3)$$

Magnetizing inductance require for charging and discharging of capacitor is given by:

$$L_M = V_s.t_c/4\ I_M{}^2{}_{(max)} \quad (4)$$

where, $t_c = T/2$.

POWER CIRCUIT FOR THE PROJECTED CONVERTER

Figure 3 bare the pspice model for the projected DC-DC converter topology, wherein ancillary transformer T_A is needed to increase the series of ZVS condition in projected converter. The primary of T_A is linked to main transformer T_M centre tap which is grounded through blocking capacitor (C_5). The secondary of ancillary transformer is connected with inductor L_M and primary of the main transformer T_M. The inductor L_M responsible for ZVS is charged using an auxiliary transformer. The Current pass through the inductor Lm by the path provided by diodes D1 and D2. In conventional topology if the load decreases voltage across the isolating transformer decreases which in turn reduces the stored energy in the inductor hence, condition for ZVS cannot be achieved under no-load condition. The topology projected in this study increase the ZVS condition for wide load variations by increase the product of volt second of ancillary transformer (Jang and Jovanovic, 2007).

The result of the simulation studied with projected converter topology is presented in Fig. 4a, b, respectively. It reduces duty cycle losses and achieves the ZVS condition.

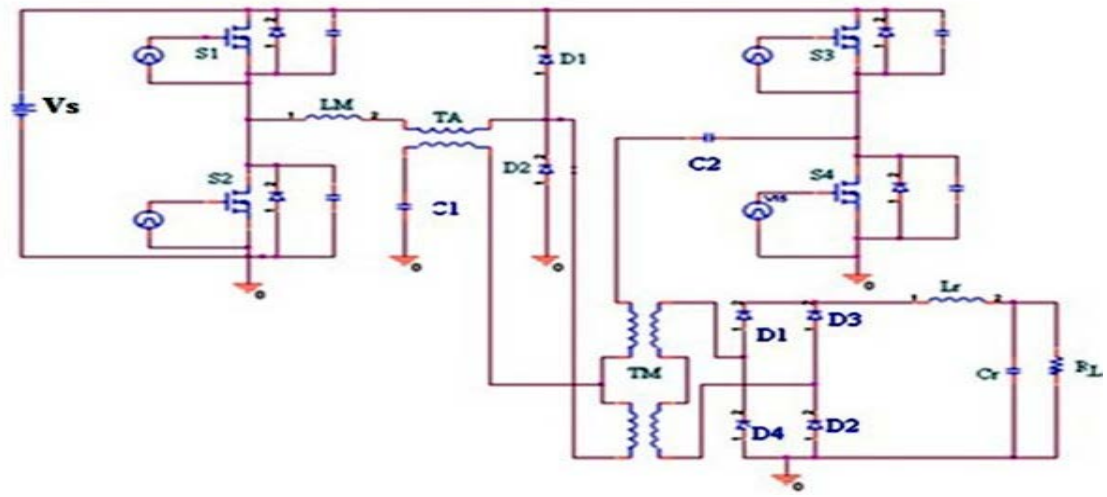
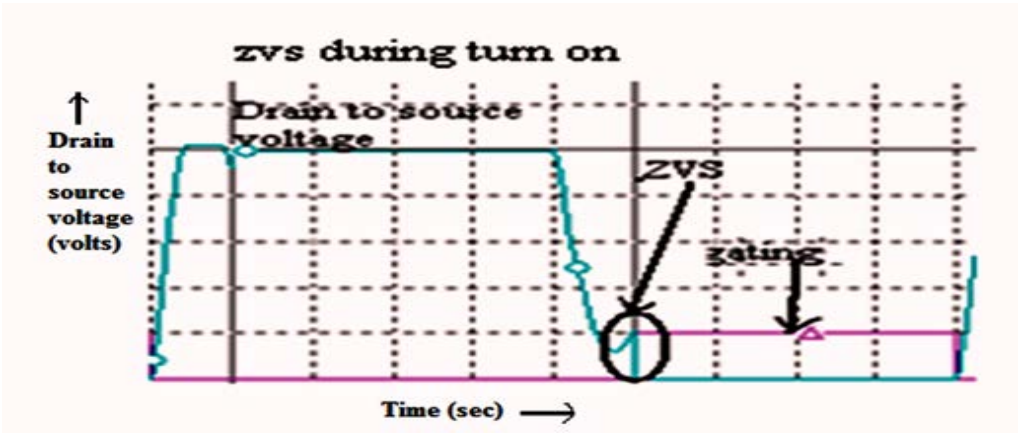


Fig. 3: Pspice simulation of Phase Shifted Zero Voltage Switching (PS-ZVS) full bridge dc-dc converter



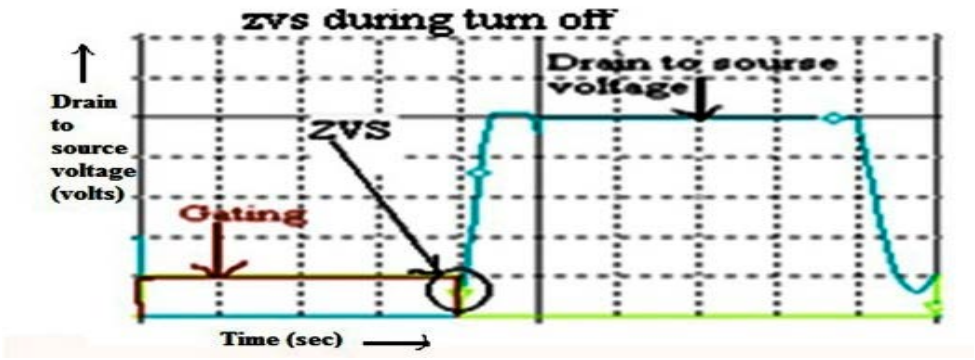


Fig. 4(a-b): (a) Zero voltage switching condition during turn on in phase shifted zero voltage switching (PS-ZVS) full bridge dc-dc converter and (b) Zero voltage switching condition during turn off in phase shifted zero voltage switching (PS-ZVS) full bridge dc-dc converter

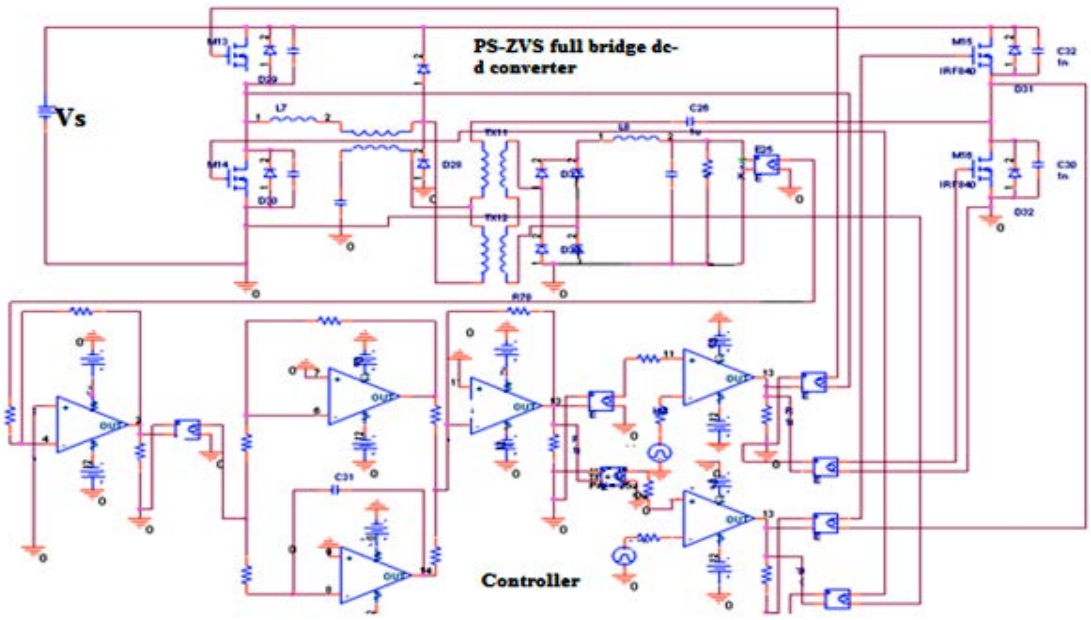


Fig. 5: Closed loop pspice model of the phase shifted zero voltage switching dc-dc converter

CLOSED LOOP OPERATION

In the constant power application like electric vehicle the output voltage should not vary with load variations. Hence, closed loop control using PI controller is proposed in this study as bare in Fig. 5. The comparator compares the output of PS-ZVS Full bridge converter with reference signal. The error signal from the comparator is fed to PI controller. The PWM generator produces the gate pulse for the S_1 and 180° phase shifted pulse is given to the S_2 with dead time (Dudrik and Trip, 2010). The input to the PWM generator is bestowed from the output of PI controller.

The result of closed loop simulation is presented in the Fig. 6. It can be observed from the simulation result, the converter maintains constant output voltage irrespective of the load variation.

RESULTS AND DISCUSSION

The experimental setup of proposed FBDCC is built and tested to verify its function with following specifications. In the proposed PS-ZVS full bridge dc-dc converter switching losses are reduced by zero voltage switching and efficiency is increased. The efficiency of the proposed method is found to be 97% which is better than (Jang and Jovanovic, 2007).

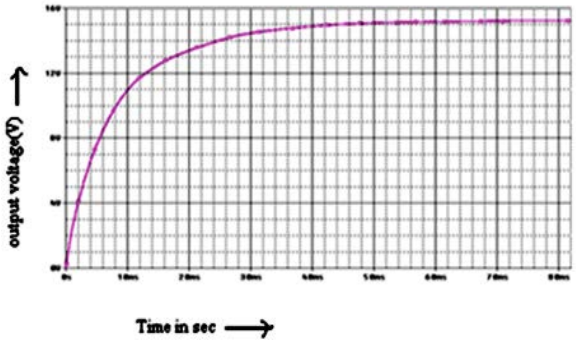


Fig. 6: Output voltage of closed loop operation of phase shifted zero voltage switching dc-dc converter

Parameters:

- Input voltage = 25 V
- Switching frequency = 20 kHz
- Inverter switches = IRF840
- Transformer parameters:
  - Primary inductance L1 = 3 mH
  - Secondary inductance L2 = 0.6 mH
  - Flux density = 0.5 wb m^{-2}
  - Area of the transformer = 3.89×100 mm^2
  - Core type = ferrite E core
- Inductor L_M = 1 μH

Fig. 7: Experimental setup of the PS-ZVS full bridge dc-dc converter

Fig. 8: Load voltage of full bride Dc-Dc converter

Fig. 9: Voltage across the load under zero voltage switching condition

The experimental setup shown in Fig. 7 is tested in open loop as well as in closed loop operation with proposed topology. The switching pulses required for converter operation are generated using PIC6F877A microcontroller. The results obtained from the experiments are bare in Fig. 8 and 9. The experimental result shows projected converter process that achieved the ZVS condition with wide load variation.

Table 1: Comparison of load voltage in the open loop

Input voltage	Load (kΩ)	Simulation output voltage (V)	Experimental output voltage (V)
25	1	9.50	9.82
25	10	10.51	10.80
25	22	11.20	11.22
25	47	16.80	15.11

Table 2: Comparison of load voltage in the closed loop

Input voltage (V)	Load (kΩ)	Simulation output voltage (V)	Experimental output voltage (V)
25	1	15.2	8.21
25	10	15.2	8.29
25	22	15.2	8.23
25	47	15.2	8.28

Pspice simulation and results obtained from experimental data for the proposed PS-ZVS converter in closed and open loop operations are bare in Table 1 and 2. It is observed that closed loop operation provides constant load voltage for various load conditions.

CONCLUSION

The operation and performance of phase shifted zero voltage switching DC-DC converter is analyzed for wide load variations. It employs one auxiliary Transformer to obtain the ZVS condition. It operates well over wide range of load Conditions, ranging from no load to rated load. The operation of the converter was verified by experimental setup. It shows reduced switching losses with improved performance. The closed loop operations of the converter for constant output voltage for wide load conditions are experimentally verified. Proposed topology with closed loop control are suitable for constant output voltage applications.

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