Performance Evaluation of Modified Cascaded Multilevel Inverter

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Abstract: Multilevel inverter has been identified as an attractive topology for high power applications. The main objective of this research work is to compare cascaded 7-level inverter with the modified 7-level inverter. The modified cascaded multilevel inverter topology can reduce the number of required power switches compared to cascaded multilevel inverter topology. The performance evaluation of the two inverter topologies has been done using MATLAB software and it has been verified experimentally. Simulation result shows the superiority of modified multilevel inverter.

Key words: Cascaded multilevel inverter, modified cascaded multilevel inverter, THD

INTRODUCTION

Multilevel inverter synthesizes a desired output voltage from different levels of dc voltages as inputs. As the number of levels increases the synthesized output waveform approaches the sinusoidal wave with the reduced harmonic distortion (Corzine et al., 2004). Also as steps added to the waveform increases, harmonic distortion of the output decreases gives 0 as the level increases. It plays a vital role in high power application and considered to be an active research area because of its well known advantages of low output Total Harmonic Distortion (THD), increase in the amplitude of the output voltage, low voltage stress of devices and low system electromagnetic interference (Rodriguez et al., 2002, Franquelo et al., 2008, Chiasson et al., 2003; Dixon and Moran, 2006).

The 3 basic multilevel inverter topologies available in the literature are: Diode clamped topology (neutral-point-clamped), flying capacitor topology and cascaded topology (Du et al., 2006). The main drawback of diode clamped multilevel inverter topology is the requirement of excessive clamping diodes and restriction in high power range of operation. The main disadvantage of flying capacitor multilevel inverter topology is the requirement of large number of capacitors per phase and control is required to maintain the capacitors voltage balance (Adam et al., 2008; Busquets-Monge et al., 2008; McGrath and Holmes, 2002). Among the 3 the most commonly used topology is the cascaded multilevel inverter topology. Its main features are simple layout, modular structure and the use of minimum number of components. This topology also reduces the problem of unbalance capacitor voltage (Ebrahimi et al., 2010; Babaei, 2010, Khomfoi and Tolbert, 2007; Zhao et al., 2010).

In this study, the comparison shows the superiority of the modified 7-level inverter.

CASCADED MULTILEVEL INVERTER

A single phase cascaded 7-level inverter is shown in Fig. 1. It has 3 separate DC sources and each supply is connected to a full bridge or a H-bridge inverter. Each level can generate the output voltages of \( +V_d \), \( 0 \) and \( -V_d \). By triggering the switches \( S_1 \) and \( S_4 \), \( +V_d \) and \( -V_d \) can be obtained by turning on \( S_2 \) and \( S_3 \). If \( S_1 \) and \( S_2 \) or \( S_3 \) and \( S_4 \) are ON, the output voltage is 0. The AC outputs of each level are connected in series such that the overall output is the sum of the inverter outputs (Corzine et al., 2004).

The number of output voltage levels of multi bridge inverter \( N \) is defined by \( N = 2S+1 \), where \( S \) is the number of DC sources required and the number of switches required is defined by \( 4N \). The main drawback of this topology is the requirement of separate DC source for each H-bridge. The number of semiconductor switches used in the topology is more compared to modified cascaded multilevel inverter.

MODIFIED CASCADED MULTILEVEL INVERTER

The main advantage of modified cascaded multilevel inverter uses less number of switches compared to the conventional cascaded multilevel inverters. Modified cascaded 7-level inverter is shown in Fig. 2. This type of
Fig. 1: Cascaded 7-level inverter

Fig. 2: Modified cascaded 7-level inverter

The inverter consists of a conversion unit with a switching device connected in series with a voltage source and a diode. The number of conversion units is equal to the number of output levels. By triggering $S_{13}$, $V_{DC1}$ is obtained at output which is equal to $V_a$. Similarly, by triggering $S_{11}$ and $S_{12}$, we can obtain the output voltage as the addition of $V_{DC1}$ and $V_{DC2}$ equal to $+2V_a$. If all the switches ($S_{11}$, $S_{13}$ and $S_{12}$) are ON, the $+3V_{dc}$ level is obtained.

The output levels are unidirectional. By using H-bridge, the output is converted into bidirectional. At positive half cycle, switches $S_1$ and $S_2$ are ON and during negative half cycle $S_3$ and $S_4$ are ON in the H-bridge inverter. The switching table for modified 7-level inverter topology is shown in Table 1. Figure 3 shows the output voltage waveform of modified 7-level inverter (Murugesan et al., 2011; Corzine et al., 2003):

No. of levels (N) = (2×No. of DC sources)+1

**HARMONIC REDUCTION**

To reduce the harmonics in the multilevel inverter, the firing angles of various stages can be selected accordingly. For a 7-level inverter, 3 firing angles $\alpha_1$, $\alpha_2$, and $\alpha_3$ can be selected at different values in order to reduce the lower order harmonies (Rashid, 2004). The conditions to select the firing angles are given by the following:

$$\alpha_1 < \alpha_2 < \alpha_3 < 90^\circ$$  \hspace{1cm} (1)

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) = (m-1) \times M/2$$  \hspace{1cm} (2)
where, $M$ is modulation index and $(m-1)/2$ is No. of separate DC sources.

The instantaneous phase voltage is:

$$\frac{4V_{dc}}{\pi} \left[ \sum_{n=1}^{(m-1)/2} \cos(n\alpha_i) \right] \sin(n\omega t) = V_{m_i}(\omega t)$$

And the modulation index $M$ is:

$$M = \frac{2V_{m(peak)}}{(m-1)V_{p}}$$

where, $V_p$ is Peak Carrier Voltage, $m$ is No. of output levels.

For the given 7-level inverter, we have chosen the $M$ value as 0.8 for effective harmonic elimination. Hence, Eq. 2 can be rewritten as:

$$\cos(\alpha_i) + \cos(\alpha_i) + \cos(\alpha_i) = 3 \times 0.8 = 2.4$$

The value of $\alpha_i$, $\alpha_i$, and $\alpha_i$ was selected to satisfy the above condition.

**SIMULATION RESULTS**

The performance of cascaded 7-level inverter and modified 7-level inverter is analysed by creating a model of the above in MATLAB/Simulink platform. Figure 4 and 5 shows the MATLAB schematic of

![Diagram](image_url)

Fig. 4: MATLAB/Simulink model of cascaded 7-level inverter
Fig. 5: MATLAB/Simulink model of modified cascaded 7-level inverter

Table 1: Switching table of modified 7-level inverter

<table>
<thead>
<tr>
<th>Duration</th>
<th>ON switches</th>
<th>ON diodes</th>
<th>Voltage levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive half cycle</td>
<td></td>
<td>D1, D4, D3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>S11, S21</td>
<td>D2, D3</td>
<td>+Vdc</td>
</tr>
<tr>
<td></td>
<td>S11, S21, S31</td>
<td>D1</td>
<td>+2Vdc</td>
</tr>
<tr>
<td></td>
<td>S11</td>
<td>-</td>
<td>+3Vdc</td>
</tr>
<tr>
<td>Negative half cycle</td>
<td></td>
<td>D1, D2, D3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>S11</td>
<td>D3</td>
<td>-Vdc</td>
</tr>
<tr>
<td></td>
<td>S11, S21</td>
<td>D1</td>
<td>-2Vdc</td>
</tr>
<tr>
<td></td>
<td>S11, S21, S31</td>
<td>-</td>
<td>-3Vdc</td>
</tr>
</tbody>
</table>

cascaded 7-level and modified cascaded 7-level inverter. Figure 6 and 8 shows the output voltage waveforms of cascaded 7-level and modified cascaded 7-level inverter and the line voltage is found to be 150 V.
Fig. 6: Output voltage of cascaded 7-level inverter

Fig. 7: FFT analysis of cascaded 7-level inverter

Fig. 8: Output voltage of modified cascaded 7-level inverter
Fig. 9: FFT analysis of modified cascaded 7-level inverter

Fig. 10(a-b): (a) Output voltage and (b) FFT analysis of modified cascaded 9-level inverter

**Table 2: Comparison chart**

<table>
<thead>
<tr>
<th>Topology</th>
<th>THD (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascaded 7-level inverter</td>
<td>13.02</td>
</tr>
<tr>
<td>Modified cascaded 7-level inverter</td>
<td>12.54</td>
</tr>
<tr>
<td>Modified cascaded 9-level inverter</td>
<td>9.65</td>
</tr>
</tbody>
</table>

Figure 7 and 9 shows the FFT analysis of cascaded 7-level and modified cascaded 7-level inverter. Figure 10 shows the output voltage waveform and FFT analysis of modified cascaded 9-level inverter.

From the FFT analysis, it is observed that THD value of modified cascaded 7 and 9-level inverter is found to be less compared to the conventional cascaded 7-level inverter and the comparison chart is shown in Table 2.

**EXPERIMENTAL RESULTS**

Modified cascaded 7-level inverter is fabricated as a prototype model. It consists of 7 switches. Multi-conversion unit consists of 3 power stages. One MOSFET and 1 diode is used as a main switch in each power stage. Each power stage is supplied by a DC source. Gating
Fig. 11: Hardware output voltage waveform of modified cascaded 7-level inverter

signals are generated by PIC 16F877 microcontroller. Based on the signals coming from, the microcontroller the switches are turned ON or OFF. The hardware result of the modified cascaded 7-level inverter is shown in Fig. 11.

CONCLUSION

The performance of cascaded 7-level and modified cascaded 7-level inverter has been evaluated elaborately in MATLAB/Simulink platform. From the simulation and experimental results, modified cascaded multilevel inverter topology is found to be better compared to cascaded multilevel inverter topology in the aspects of Total Harmonic Distortion and the requirement of power semiconductor switches. As steps added to the waveform increases, harmonic distortion of the output decreases as the level increases.

REFERENCES


