Asian Journal of Information Technology 4 (9): 816-822, 2005

Testing of Complex Integrated Circuits (Ics)-the Bottlenecks and Solutions

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Abstract: Miniaturization of Integrated Circuits (ICs) makes physical access for test purpose either difficult or even impossible. Further, the ICs growth along with its increasing complexity encounters the problem of large amount of test data also, number of access ports remains constant hence forcing towards long test application time. High speed ICs further complicates the testing problem enforces the high demand on tester's driver/sensor mechanism and more complicated failure mechanism. This study discusses all such problem of the testing along with the test goal destination; Built In Self Test (BIST)-a final solution.

Key words: Integrated Circuits (ICs), Testing, Design For Test (DFT), Built-In Self-Test (BIST), Linear Feedback Shift registers (LFSRs)

INTRODUCTION

Early Small Scale Integration (SSI) technique evolved was consisted of about ten individual components on a silicon chip of 3mm (0.12-inch) square. The development of Large-Scale Integration (LSI) during the early 1970s made it possible to pack thousands of transistors and other components on a chip of roughly the same size. The technology gave rise to the microprocessor, an Integrated Circuits (ICs) that contains all arithmetic, logic and control circuitry needed to carry out functions of digital computer's central processing unit. Very Large Scale Integration (VLSI) developed during the 1980s, has vastly increased the circuit density in microprocessors (as well as of memory and support chips). The technology has yielded microprocessors containing more than 20 Millions transistors on a chip of less than 2cm (0.79-inch) square. Over the current years there has been a further remarkable growth in VLSI techniques; The Very-Very Large Scale Integration (VVLSI), Ultra-Very Large Scale Integration (UVLSI), and Application Specific Integrated Chips (ASICs) are the coined names of the modern electronic industry. The electronic revolution is driven by the extraordinary strides in the semiconductor technology progress. This attribute is making the IC chip the foundation of modern electronic industries[1-7]

Thus, this is the fact that the tremendous advances in fabrication technologies have led to increased IC densities. The overall impact has been the:

- Decrease in cost per function of digital processing hardware, and
- Greater system reliability

However, as a consequence of higher integration densities, circuits have become very complex. To verify their correct functioning, ICs are required to be thoroughly tested. The cost involved in testing of even LSI chips is a substantial portion of the total manufacturing cost. Further, advances in IC technology are occurring at a rate faster than those in test technology. A direct consequence of this is that testing methods, which are inadequate even for LSI circuits, are grossly unable to cope with the increased circuit sizes because of higher chip densities. Thus, Reliability and testing techniques have become of increasing interest to all applications where digital systems are involved; like computers, telecommunications, consumer products, automotive industry and many more[7-9].

Thus, it is obvious that testing is facing through so many challenges. For example test application time propagates as the function of square of complexity of the circuit whereas; fault-insertion further enhances the time by a power of three.

Design-For Testability (DFT), Built-In Self-Test (BIST) are the solutions but what stages of the design will be appropriate to incorporate them. How the circuits exploits the memory elements of the circuit it self in the process of the testing? Why the testing is bound to look for a response data compaction technique? What are the problems in using the response data compaction techniques? How the testing cost and level of testability can be monitored?

Therefore, through this study we want to highlight the bottlenecks of testing along with the solutions.

BOTTLENECKS

Electronics growth and test complexity: Today's electronic devices are made possible only by the continuing efforts to develop more complex electronic circuit functionality with reduced device geometries, leading to smaller, more power efficient microelectronic circuits capable of use in applications from high-speed communications through to biometric sensing and ambient intelligence. The end-user only sees the final product, but there are many steps involved in the design, fabrication and testing of the devices before the end-user has access to the Microelectronic Circuit i.e. IC, Microchip or Chip. These devices may be digital, analogue or mixed-signal in nature. According to the Semiconductor Industry Association (SIA) Roadmaps 1995, 1997 and 1999, feature size of chips reduces 30% every three years, the overall chip size increase is 12% per year and we have 58% more devices per year. This significantly increases the problem of testing and validating the IC chip to make sure that the logic is correct and there are no fabrication errors. The test data per gate is fast approaching 1kilobyte and million gate designs require 1 Gigabyte of test data. Consequently, the volume of test data is becoming huge and leads to excessively long test application time. The reducing chip size also leads to the increase in the number of physical faults. This is because; the chip defects don't reduce in the same proportion as that of chip size shrinkage. The current available data from SIA Roadmap of 2001 is shown below in Table 1 for extrapolating the complexity of the problems of testing.

Moore's law[10,11] is the de facto driving force of microelectronics, a self-fulfilling prophecy of the arrival of ever-faster CPUs and ever-denser packing electronics. By assuming that one will have to handle the next generation of electronics with today's test generators, one can obtain a maximum fig for the complexity allowed for a test generator (Table 2). This table is based on the fact that it is generally held that the speed of a CPU will increase by a factor of two in eighteen months, while the packing density of gates grows by a factor of four. The implication is that one can choose from a number of approaches to be able to generate tests in the future[12-18].

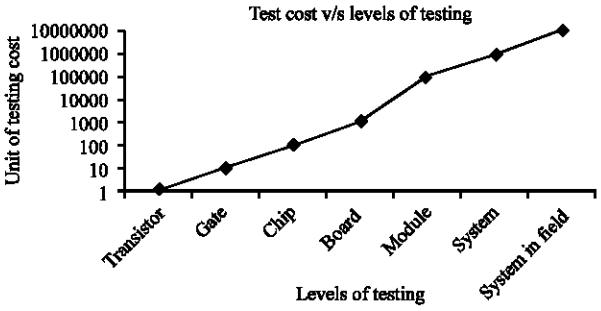

Fig. 1: Test costs v/s levels of testing

The designers' competence with matched knowledge of testing will be a real requirement to cope with the technology-A real challenge.

Test Cost: Test costs 10 times more than to test a component as one move to higher level in the product manufacturing process. Fig. 1 demonstrates this rule of thumb. The possible levels of testing can be categorized and are listed as below:

- Components(resister, inductor, capactors, diodes etc.)
- Transistor
- Gate
- Chip
- Board
- Moudle
- System
- system in field

Table 1: SIA Roadmap 2001 Extrapolation Summary

	Feature size		Internal clock		Logic transistors	Microprocessor	DRAM size		SRAM size		Voltage
	Units		High Performance								
Yesars	Microns	Nanometer	MHz	GHz	Million/cm^2	Millions Transistors/chip	Megabyte	Gigabyte	Megabyte	Gigabyte	V_{dd}
1993	0.50	-	200	-	2.0	05.2	16	-	1	-	5.0
1995	0.35	-	300	-	4.0	12.0	64	-	4	-	3.3
1999	-	180	750	-	6.6	23.8	256	-	16	-	2.5
2001	-	130	-	1.68	13.0	47.6	512	-	64	-	1.2
2003	-	100	-	2.31	24.0	95.2	-	1	256	-	1.0
2005	-	80	-	5.17	44.0	190.0	-	2	512	-	0.9
2008	-	70	-	6.74	109.0	539.0	-	6	-	1	0.7
2011	-	50	-	11.50	269.0	1523.0	-	16	-	4	0.6
2014	-	34	-	19.30	664.0	4308.0	-	48	-	8	0.5
2016	-	22	-	28.70	NA	N/A	-	N/A	-	N/A	0.4

Table 2: Test Scaling Factors

	CPU Speed	Package Gates Density of	Memory Size Requirement	Designer's Competence
Today	1	1	1	1
Next Generation	2	4	4	?

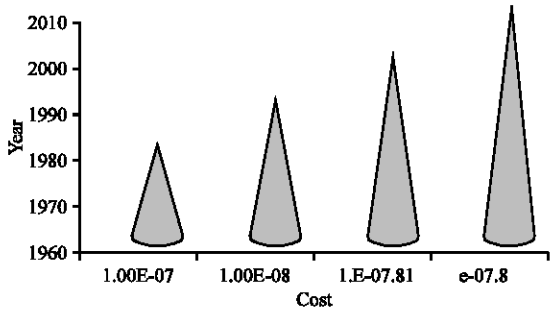

Fig. 2: Moore's law for test capital

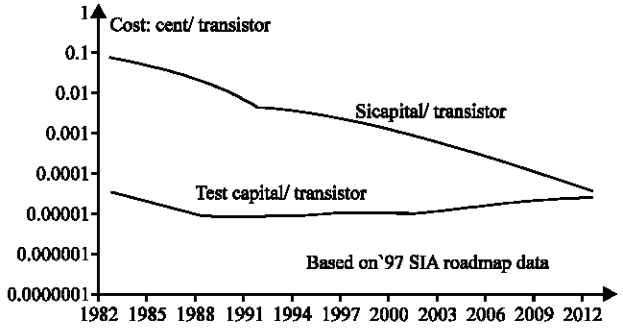

Fig. 3: Moore's law for test: chip fabrication v/s. Test capital

Although there is other ways to define levels-these are important to develop correct fault model and simulation models Chip level testing-is nothing but gate level design:

- Transistor
- Gate
- RTL (Register Transfer Logic)
- Functional
- Behavioral
- Architecture

The semiconductor suppliers face two key cost challenges due to the changing the way VLSI-ICs are tested today. One is that the cost of manufacturing test has not been scaling. Secondly, the engineering effort to generate tests has been growing geometrically along with product complexity. A general rule of thumb is that capital costs run in the range of 50% of the overall IC test cost in the industry, so looking at capital costs is an essential analysis for manufacturing test. Fig. 2 and 3 show the plots extrapolated from the 1997 SIA

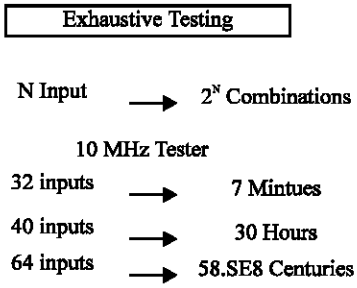

Fig.4: Test time of a circuit related to the number of inputs with 10 MHz clock

technology roadmap for semiconductors[19]. It shows the capital costs for chip fabrication versus the capital costs for manufacturing test, normalized per transistor. The top curve in Fig. 3 shows the consistent reduction in chip fabrication cost per transistor that is the basis for Moore's law, which in turn drives the continued expansion and evolution of the semiconductor business. The bottom curve of this figure, which can be traced back 20 years, indicates capital expenses for IC test have been essentially flat per transistor. Based on the current SIA data, this trend of flat test capital cost per transistor was projected to continue for the foreseeable future Fig. 2.

Test time and memory requirement: The primary problems when testing digital Integrated Circuits (ICs) is the rapid increase in possible input assignments as circuits grow larger. The function table of an N input circuit holds 2^N differentinput vectors, and it soon becomes unfeasible to perform an exhaustive test of a circuit. The process of testing and exhaustive testing scenario with typical 10 MHz tester frequency can be visualized in Fig. 4. The effect of this may be seen in Fig. 5, where the test time of a circuit clocked at 500 MHz is shown as a function of the number of inputs to the circuit. Fortunately, the properties of most combinational circuitry frequently allow one input vector to detect more than one of the possible faults of the circuit. This makes it possible to reduce the set of test vectors to less than 2^N by using clever mathematics and heuristics. The price of obtaining a shorter test time is an increase in test generation time or more complex test hardware.

Since testing can be a bottleneck in IC manufacture, significant amounts of money may be saved by shortening the testing time.

The requirement of memory (M_R) can be thought out by looking to Equation 1. Simulation complexities of circuit simulation (C_S), fault simulation (F_S) and total test simulation (T_S) processes can be adjudged by the Equations 2-4 respectively.

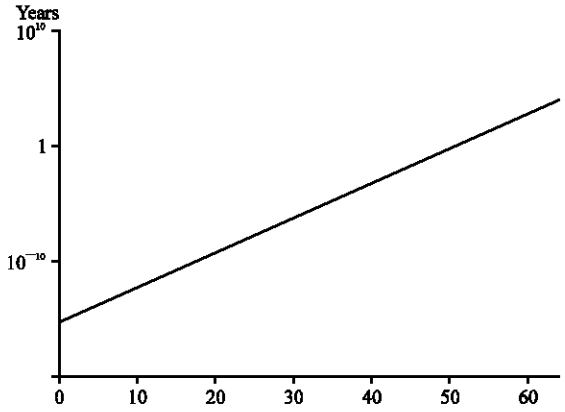

Fig.5: Test time of a circuit related to the number of inputs with 500MHz clock

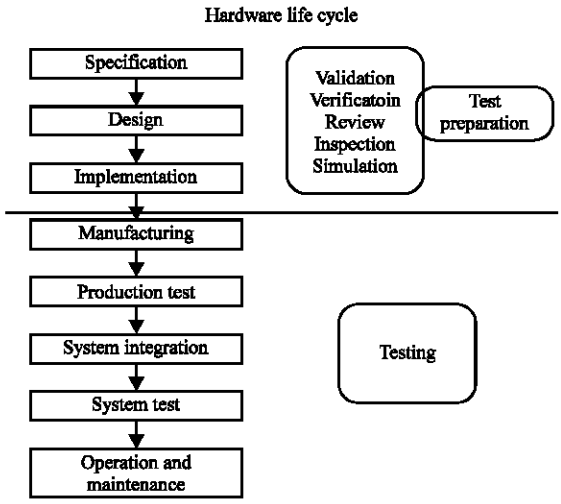

Fig. 6: Design and test hardware life cycle.

$M_R = 2^N * (f + 1)$ (1)
$C_S = K_1 * G^2$ (2)
$F_S = K_2 * G^3$ (3)
$T_S = K_1 * G^2 + K_2 * G^3$ (4)

Where, f is number of faults, G is gate count and K_1, K_2 are constants depends on many factors like fan-ins, fan-outs, yields, redundancies and etc.

SOLUTIONS

Refer to Fig. 6 to understand the whole process of modern design and test process and their relationships. The testing of microelectronic circuits has today greater importance in the overall product development cycle. Whilst in previous years, the test process was considered more an 'after-thought' once the circuit design cycle had been completed; it is now a key factor

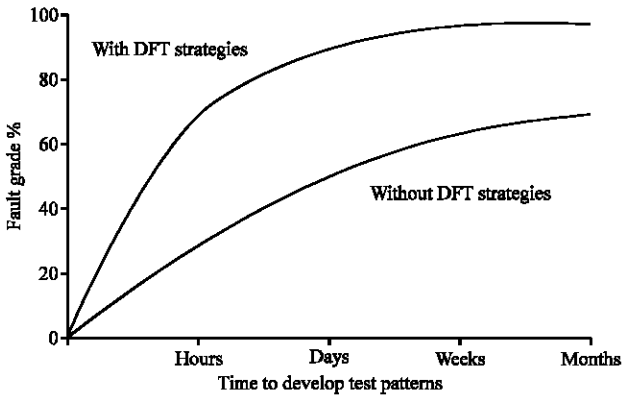

Fig. 7: fault grade v/s test development time

in early design decisions, following a 'Design For Testability' (DFT) approach. The traditional barrier between design and test is gradually being removed, developing a high level of integration between the design and test communities. Testing of the digital portions of a design is supported through structured DFT techniques with good Computer Aided Design (CAD) and Computer Aided Test (CAT) support. In contrast, the analogue and mixed-signal portions of the design present new sets of problems that are not easily addressed.

Design and Test Integration : With the increasing design requirements, new semiconductor technologies, and need for lower costs with improved quality levels, test is becoming a key area in order to solve quality and cost issues. The testing of analogue and mixed-signal integrated circuits has become a topic of great interest in recent years in order to address problems associated with the cost and relevance of conventional test approaches, along with Automatic Test Equipment (ATE) cost and performance issues. A way to reduce test time and costs whilst maintaining or improving test quality is a major challenge. This is leading to the desire, driven by cost and quality requirements, to provide a mechanism for devices to incorporate the capability of testing themselves. Design For Testability (DFT), Built-In Self-Test (BIST) for next generation Mixed-Signal Integrated Circuits (MS-ICs) is an area requiring extensive research thrust to give the solution of some complex issues of test methodology, utilizing semiconductor technologies towards the 90nm technology node. Fig. 7 can be viewed to adjudge the benefit of the DFT[2,7,8,20,21].

Test engineering specific education is an important building-block in order to achieve the above.

The chip is tested from outside by the means of ATE. Most manual methods at test development use fault simulation as their guide to determine the fault coverage achieved. These rely on logic simulation and with the increasing complexity of ICs, it is an impractical method both from the context of computational complexity and run time for simulation.

Scan based designs are more commonly used in modern ICs. Scan is a design technique whereby sequential elements in a circuit can be used to scan data into a portion of the circuit and to scan the results out. There are essentially two modes of operations of a Scan based design. One, the normal mode and the other is the test mode .In the normal mode, the circuit under test performs its normal or regular function .In the test mode, all the sequential elements are connected into one or more shift registers.

The cost of ATE is very high and ATE has not been able to achieve effective fault coverage with access basically only to Input-Output (I/O) pins. Scan based designs allow isolation and testing of IC components to some extent by bringing the I/O pins of the cores and other circuits to the I/O pins of the IC. Also, the problem of verifying the interconnections between the cores and other circuitry is not solved and additional functional testing is required to satisfactorily verify this. All this leads to time consuming and expensive operation.

The problems faced with the present ATE based testing include exploding test data, high cost of equipment and inability to verify chips at speed. Also, there is a question of tester accuracy .It is predicted that tester accuracy will improve in the near future but at as much lower pace than the increase in clock speeds, it could lead to 48% yield loss due to tester accuracy as compared to 10% at present. Such yield losses are unacceptable and can further jack up testing costs. Increasing chip densities also increase the chances of manufacturing defects and further complicate the testing process. All these bring forth the limitations of ATE and point to the need of having a different approach. The answer could be BIST.

Built in Self Test (BIST): To make digital system testing and diagnosis quick an effective we could include test as a functionality of the system itself. Self test is often used in software purely software approach at the system level is however not very good due to the long time it takes and its expense. Implementing self-test in hardware is itself more attractive and challenging.

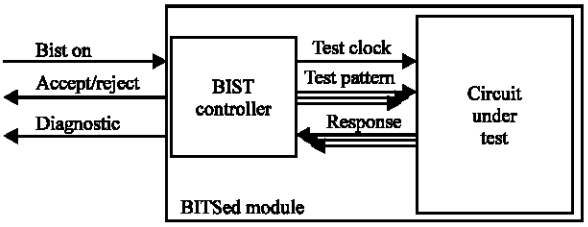

Fig. 8: A general model of BIST structure

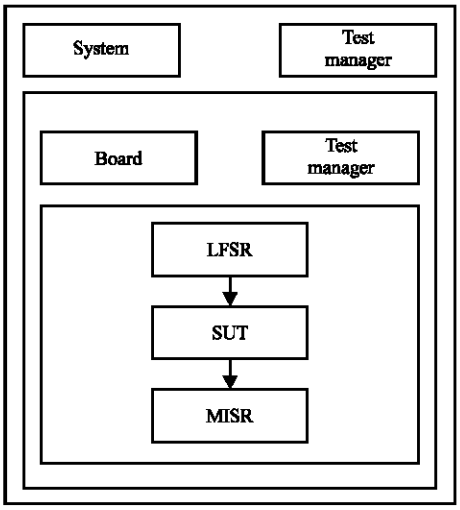

Fig. 9: Hierarchical view of BIST

The general model of BIST is shown in Fig. 8. Looking to the figure it can be said that BIST is such a self-test test technique in which the testing (comprising of test generation and application) is done through built-in hardware features. It can be embedded on a chip and can potentially solve most of the limitations faced by ATE. The basic BIST architecture requires an additional overhead in the circuit. This is in the form of pattern generator usually a pseudo random pattern like that produced by Linear Feedback Shift Registers (LFSRs), a response analyzer usually a Multiple Input Shift Register (MISR) and test controller.

A basic BIST design builds on popular scan design methods by adding the LFSR to produce pseudo random patterns injected at the input of scan chains and the MISR to the output of the chain to compact and analyze the data. A test controller is necessary to activate the pattern generation and response analysis parts of BIST. A hierarchical approach to BIST highlights its distinct advantage in accessing even remotely embedded parts of the chip. The figure below shows the hierarchical view of BIST. Fig.9

Advantages of BIST-A Complete Solution Package: Underlying the BIST technology is the observation that ATE consists mainly of semiconductors akin to the chips and cores they test. BIST integrates some of these semiconductor portions into circuits under test itself. This way each chip now has a tester built into itself. This way the problem of complex interfacing between the ATE and the IC is also eliminated.

The increasing complexity of chips necessitates the partitioning of circuits so that each can be tested separately. This is not practically feasible with the traditional methods. However, using a hierarchical BIST structure facilitates this. Assuming that all the levels use BIST, it is possible to test the circuit under test (CUT) from the system level by sending a control signal to the board, which activates the chip level tester. This activates the chip level test and the result is passed up the hierarchy. This way the embedded portions and interconnections are tested locally and the system level tester need only check the functional accuracy of the system.

A large number of test vectors fed at the I/O of the chip by the ATE may be eliminated because they may not excite the particular CUT. This reduces the test data explosion problem. Only the test vectors that potentially affect the CUT need to be generated locally using BIST.

Test pattern generation and storage is a major problem in ATE. These patterns intended for a particular CUT need to be passed through a number of levels in order to reach the CUT and the results have to again propagate back to an observable point. With the BIST design, the testing is localized and the patterns are generated and applied locally eliminating this problem. This makes it easier and faster to generate and apply test vectors to a CUT. Another problem that is emerging in the use of ATE is that traditionally the testers need to access the pins of the chips mounted on the board. However, this is increasing being impeded by the rise of surface mount technology in which the components are mounted on both sides of the board making a bed of nails structure impractical. BIST, on the other hand can test chips, boards and the entire system without the need for access to all the pins by using the hierarchical structure discussed earlier. The self-test methodology enables a logic block to test itself and also its interconnections with the other blocks on the chip, something that the traditional ATE is not good at doing.

As mentioned earlier, modern ICs are becoming more and more core based. BIST offers distinct benefits in that respect. Having BIST ready cores solves the testing problem because the cores can test themselves when activated by the system test controller and the system integrator need not be concerned about the internal structure of the core. This also resolves the Intellectual property issues that come along with the core-based designs. It is much easier to access embedded memories and other similar structures tucked away inside the chip if BIST is used. At-speed testing is also much easier with BIST. This also improves coverage of signal delay faults. All these features of BIST make it a very attractive contender for quick and effective testing in the time to market driven industry.

The major stumbling block in the acceptance of BIST has been the logic overhead required in each and every chip produced unlike the one time investment in ATE. This overhead is becoming less of a concern now because the overhead does not increase proportionally with the chip size. BIST offers huge savings in product life-cycle costs of chips that are very expensive and need to be debugged during their life. Thus with the larger, more complex circuits coming out, the overhead is relatively small. All things considered, BIST is only on its way to becoming economically and practically the preferred solution for chip testing in the foreseeable future.

CONCLUSION

There is a high ended mismatch in the developmental pace of the test and manufacture technologies. The test methodology needs at moment a high pace of priority in its development and research or otherwise poor test methodology is going to reflect its virus like impact on cost, accident, reliability, life cycle, environmental hazard and on many more related issues. Today, one has to remember that testing accounts almost up to 50% of product development efforts and tomorrow it is going to increase the cost in many folds. So, this is the need of the day is to produce better designers who has competence of test technology too who considers that the key to successful testing lies in the design process.

ACKNOWLEDGEMENTS

The acknowledgements are due to authorities of Sultan Qaboos University (Sultanate of Oman) for providing research support grant (SQU-PGSR/ IG/ENG/ECED/04/04).

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