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Three State Skip Logic Built-In Self-Test Scheme for Combinational Circuits

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Abstract: As technology processes scale up and design complexities grow, system-on-chip integration continues to rise rapidly. According to these trends, increasing test data volume is one of the biggest challenges in the testing industry. In this study, we propose a test data compression based Three State Skip (TSS) Logic for Low Power Built in Self Test (BIST) applications. The Three State Skip (TSS) primarily aims at reducing the switching activity during a scan by skipping preselected test vectors. For improving the compression efficiency, a Reconfigurable Johnson Counter (RJC) is used to reconfigure and skip function. It is useful to reuse previously used data for making present data by using the function of feedback or tapping of the Linear Feedback Shift Register (LFSR). Three State Skip circuit is developed to achieve little scan power by splitting and skipping long scan chain switching activities. This research solves the challenges faced in Fault detection circuits with the proposed Three State Skip logic. The Efficiency of such system is compared with Two Folded State Skip (TFSS) Logic and generates minimum test patterns by skipping the scan chain.

Key words: TFSS, LFSR, RJC, BIST, TSS

INTRODUCTION

An enormous number of various failures experience during the manufacture of ICs and it is totally infeasible to analyze them individually. Thus, failures are clustered according to the obvious fault effect on the functionality of the circuit which in turn leads to the edifice of logical fault models. Defects present in the IC can classify into three types, namely, permanent fault, temporary (transient or intermittent) fault and delay fault. Both permanent and temporary faults were purely time-dependent, the permanent fault exists long enough in the circuit which can observe at test time. On the other hand, the transient faults appear and disappear in the short interval of time. The delay fault will de-perform the operating speed of the circuit. High fault coverage accomplished by techniques such as Design for Test (DFT) and Automatic Test Pattern Generation (ATPG). BIST and DFT methodology is advantageous than another testing scheme because of its testability, testing speed and independent of automatic test equipment.

In the testing process, the broad and complex chips require an enormous amount of test data and dissipate more power during the test. The reason is that the consecutive input test vectors are statistically independent which results in increased switching activity in the circuit during testing. Minimization of test power, test length (test application time), fault test coverage and test hardware area overhead in the testing of VLSI circuits is a challenging problem for the researchers. Thus, the above factors motivated to do research in this area. Most of these techniques to enhance the design of the TFSS method to reduce the transitions in the primary inputs of the Circuit Under Test (CUT) for test-per-clock BIST or inside the scan-chain for scan-based BIST.

Literature review: In the past one decade, researchers have proposed different testing methods of VLSI circuits. The literatures associated to the proposed work have been discussed to a better extent in this study. Testing swears that the role of each manufactured circuit corresponds to the function of the implemented (Lien *et al*., 2013). Final product of a reliable VLSI circuits depends strongly on testing which eliminate various defects caused during the manufacturing process discussed here.

A new variable length ring counter based testing presented in (Zhou *et al*., 2009) which are operated at different speeds. The reduction in average power consumption and switching activity is achieved by driving the state skip LFSR circuit (Nourani *et al*., 2008). Test vector insertion based a new design called Low power methodology in order to generate test patterns with low switching activity (Wang and Gupta, 2002a, b) for scan based BIST application thereby average and peak power is substantially reduced.

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Both Randomized test data (Weiling *et al*., 2010) and control schemes (Wen *et al*., 2010) are designed for low power test compression in ATPG applications.

Test data volume and dictionary volume are reduced by having smaller number of codeword for larger block size (Zhou *et al*., 2007; Wen *et al*., 2010). A new non-uniform cellular automata technique (Kilic and Oktem, 2005) is used for generating less test vectors to detect fault in the circuits. Multiple IP embedded cores with more flexible control code to attain high data compression is called scan slice encoding discussed in (Wang and Chakrabarty, 2005). The analysis of clustered test vectors using repeated sequence test for Hybrid BIST presented by Li and Chakrabarty (2005). The code compression technique is proposed which combines hamming Distance Based Reordering (HDR), Column wise Bit Stuffing (CBS) and Difference Vector (DV). The scheme preprocesses the test data before applying any other compression technique for giving better compression (Gonciari *et al*., 2003; He *et al*., 2003; Das *et al*., 2003; Chakrabarty and Swaminathan, 2000; Chakrabarty *et al*., 2000).

The consecutive reduction of test data scheme (Zorian, 1993; Zhou *et al*., 2007) showed a new DFT scan scheme to reduce shift-in power in linear decompressor based test compression environment. Assume that continuous flow decompression is used in this compression environment. Three-dimensional stacked integrated circuits using Through-Silicon Vias (TSVs) and micro-bumps provide a solution to the growing demand for high performance and low power micro-electronic products (Tenentes *et al*., 2010).

Self test schemes are used to design the overall architecture and basic values of the various compression algorithms which are discussed previous. This scheme has the potential of obtaining useful seeds and don't cares in the self test procedure (Stroele and Mayer, 1997).

MATERIALS AND METHODS

Three state skip methodology: The architecture of the proposed TSS scheme consists of several functional or logical blocks as shown in Fig. 1. The proposed structure has few principal components namely seed from memory, Reconfigurable Johnson Counter (RJC), Spilt test data set, Match test data set, compressed test data set and Circuit Under Test.

Firstly the whole test vectors are stored in memory which is feed to RJC each time of testing. These test sequences are generated randomly using RJC architecture. If the present test sequence length is high, then the data was divided as 10 bit length using spilt test block.

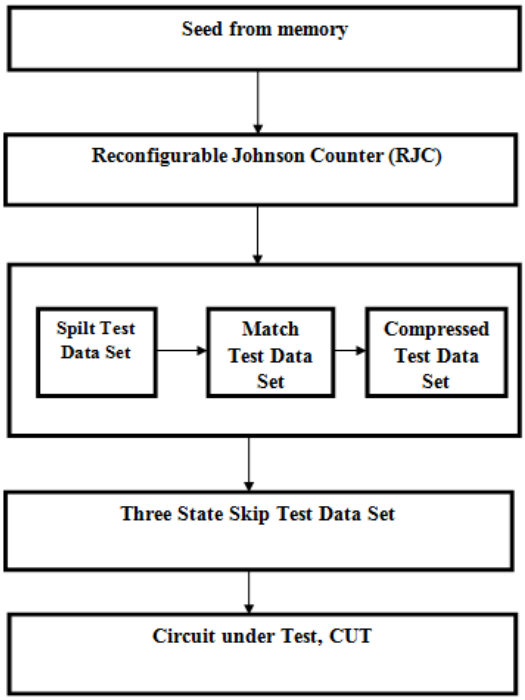

Fig. 1: General architecture of TSS scheme

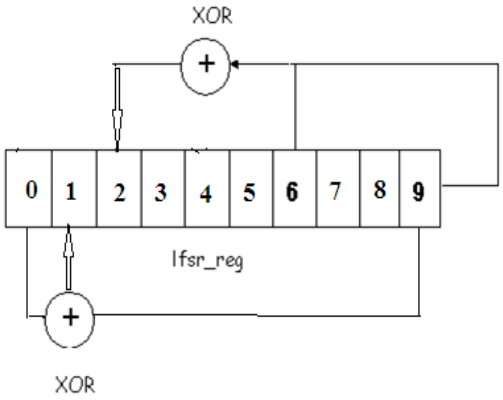

Fig. 2: Proposed TSS logic

Then the present test sequence are compared and matched with the next consecutive test sequence using TSS algorithm. It creates different state value based on the correlation of the various test sequences. Finally, those test sequences are sent to CUT.

Implementing three state skip LFSR architecture: Proposed TSS logic presents to reduce the test sequence when compared with the Two folded state skip LFSR. As the TFSS LFSR architecture corresponds to their characteristic polynomial, this TSS logic based on a set of instructions performs successive jumps between the states. The proposed architecture of the proposed TSS LFSR is shown in Fig. 2. In this TSS logic, minimum test

Table 1: TSS and TFSS test sequence

Test vectors	TSS-pattern	TFS-pattern
1000100011	1010 0100 01	1000 0100 01
1010010001	1011 0010 00	1101 0010 00
1011001000	0111 1001 00	0101 1001 00
0111100100	0001 1100 10	0011 1100 10

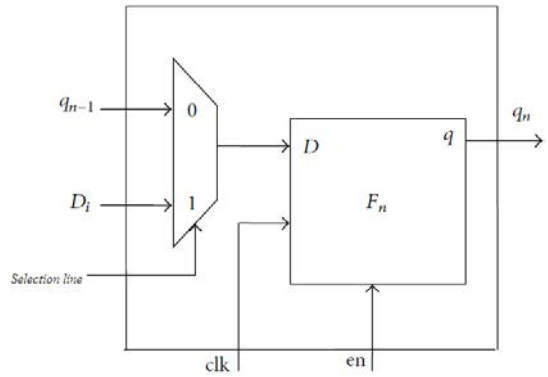

Fig. 3: Proposed RJC architecture

data storage is attained by selecting or skipping the test data in the useless parts of the test sequence. The switching between the modular form is executed by reversing the direction of all the data flow between the latches stated in the TSS logic tapping (XOR-ing 0th and 9th bit stored in 2nd bit position) and taping 9th and 6th the feedbacks into the third latch. The resultant state sequence is shown in Table 1.

Implementation of reconfigurable johnson counter: Figure 3 shows that the architecture of Reconfigurable Johnson Counter (RJC). The RJC consists of D-flip flops (D-FF) and Multiplexer combined to generate certain test patterns by selecting the mode of operation. The modified structure of RJC has five inputs namely clk, enable(en), selection line, D-FF and q_{n-1} then single output as q_n. Whenever the selection line which is equal to logic "0" then the proposed RJC counter starts to generate new test patterns using count operation to avoid the consecutive test sequences. If the selection line is set to logic "1" then the present test sequence (seeds) fed from memory. Figure 4 shows that the implementation of RJC using D-FFs XOR-ed with the feedback loop produces a new sequence of the test vector.

Test data split: The original test data set, T_D for a circuit with n test patterns which are generated by the ATPG, can be represented by an n-tuple set, $T_D = \{T_D^1, T_D^2, T_D^3 ..., T_D^n\}$ where the length of i^{th} test data, T_D^i which consists of 0s, 1s and Xs, match the length of the scan chain, l_{SC}. After acquiring the above test data, T_D, the next strategy is for each T_D^i to be split into the length of the l_{SR}. Hence, this makes the m×n split test data sets:

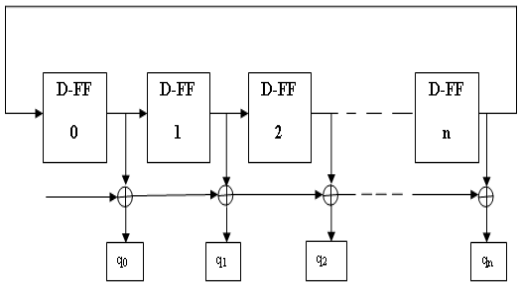

Fig. 4: Implementation of RJC

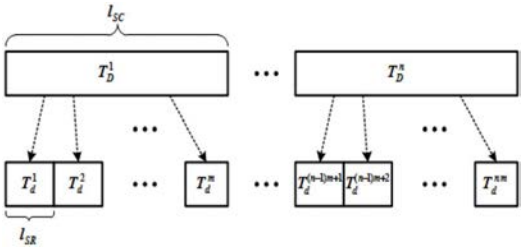

Fig. 5: Test data split scheme

$$T_D^i = \{T_d^{(i-1)m+1}, T_d^{(i-1)m+2}.., T_d^{im}\} \quad (1)$$

Where each T_d^i is a subset of T_D^i and the length of these subsets is l_{SR}. Hence, test data T_D is composed of the subsets of T_d^i with slices of m×n as shown in Fig. 5.

Here, the value of l_{SR} must be determined by a certain standard because this length is associated with the hardware area overhead and compression ratio. The amount of compressed test data can be predicted for determining a suitable l_{SR} by the following:

$$C_{(B)}(T_D) \cong |T_D| \times \left[1 - P_{(m)} - \left|\left(T_d^i, T_d^{i+1}\right)\right|\right] R_{pi} + (m \times n) \quad (2)$$

Where:

$C_B(T_D)$ = Number of compressed bits of the test data

T_D, $|T_D|$ = Size of the test data and is the probability of match between T_d^i and T_d^{i+1}; it can be written as follows:

$$\left[P_{(m)} - \left|\left(T_d^i, T_d^{i+1}\right)\right|\right] = 1/(n \times m - 1)$$
$$\sum_{(i=1)}^{(n \times m-1)} \left(T_d^i == T_d^{(i+1)}\right) \quad (3)$$

Finally, the key is that the two terms, $[P_{(m)}-|(T_d^i\ T_d^{(i+1)})]$ and m are dependent on l_{SR}. Therefore, l_{SR} is closely related to the compression ratio and hardware area overhead. The effort to obtain a full area for proper l_{SR} is important for acquiring improved results.

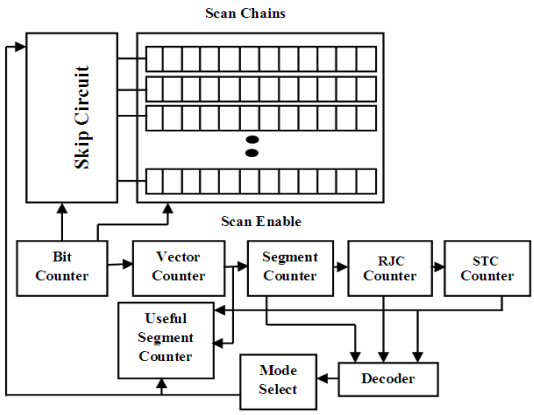

Fig. 6: Decompression architecture with proposed TSS logic

Matching and compression algorithm for test data: To improve the efficiency of the proposed TSS logic satisfies the matching and compression algorithm. In order to compress the split test data, the two steps should be performed: A forward X-filling for more matching test data set and a backward X-filling for compressed test data set. The unfilled split test data T_d^i are converted to filled split data, T_d^i where $T_d^i = \{T_d^{(i-1)m+1}, T_d^{(i-1)m+2}, ..., T_d^i m\}$; they are a subset of T_P. Finally, the split variable T_p^i and filling variable added to store the matching point. Then the matched test vectors are compressed using TSS algorithm. The steps involved in TSS algorithm are shown in below.

TSS-Algorithm:

- Initialize test set
- $T_p^i \leftarrow T_d^i$
- for I = 1-m-1 do
- for l = 1-l_{SR} do
- if T_p^i bit streams from l^{th}-l_{SR}^{th} are equal-T_d^{i+1} bit streams from 1^{st}-(l_{SR}-l+1)th do
- $N_{eq}^{i+1} \leftarrow l_{SR}$-l+1
- for j = 1-l_{SR}-l+1 do
- if T_p^{i+1} [j] is an unspecified bit do
- T_p^{i+1} [j]~T_{SR}^{i+1}[j+l-1]
- else do
- T_p^{i+1} [L_{SR}-l+2]~T_p^{i+1}[l_{SR}]~
- end if
- end for
- T_d^{i+1} [l_{SR}-l+2]~T_d^{i+1}[l_{SR}]
- break for
- end if
- end for
- end for

The proposed decompression architecture is shown in Fig. 6. When a new seed value is loaded in the decompression architecture, Useful Segment Counter is initialized with RJC Counter value to count the total number of useful segments generated for each seed.

Table 2: Power reduction of benchmark

	TFSS-LFSR		Proposed TSS scheme	
Bench markckt	Avg power (μW)	Peak power (μW)	Average power (μW)	Peak power (μW)
S5378	600	4200	582	2100
S9234	730	4520	680	2260
S13207	745	4735	602	2367.5
S15850	783	5904	594	2952
S38584	2466	19880	2102	9940

Figure 6 illustrates the proposed decompression architecture having chain environment with RJC and Skip Test Code (STC) Counter, useful segment counter and decoder logic. Whenever a new seed entered various counters are used to compare and skip the sequence then the final seed id fed to useful segments counter. Then, a new set of seeds are chosen for the more processing. To find out the excellence of the useful segment, Mode Select unit is used here. For this evaluation, all the values of Segment, RJC and STC counter are decoded. The decoded output is given to the Mode Select unit to drive the proposed test data Skip logic.

RESULTS AND DISCUSSION

The Modeling and implementation of the proposed TSS scheme is done in VHDL and simulation is carried out in Model Sim 6.5. Parameters like power, area are analyzed in Xilinx 14.2 ISE. In this study, samples of 256 test patterns are analyzed for correlation, randomness and number of transitions between consecutive patterns. The validation of the analyzed patterns is done by applying to the bench mark circuits of different complexity. Power analysis is done with the maximum, minimum and typical input test vectors for stuck-at faults and transition faults of combinational and sequential circuits. Results for each method are tabulated and compared with the previous methods. The obtained results proved that the reduced Dynamic power dissipation is by TSS scheme.

Table 2 shows the Comparison between the Existing Algorithms (TFSS) and proposed TSS algorithm for peak and average power analysis for ISCAS benchmarks in testing. From the analysis proves that TSS scheme reduces the power compared to TFSS. Figure 7 shows the comparative result of power consumption from the result shows that the proposed method has produced more optimized result than other methods.

Table 3 shows the area overhead results for TSS scheme compared to TFSS method with low test data volume. The experimental results clearly show that the proposed method can be implemented for large designs with low area hardware. Figure 8 shows the comparative result of power consumption, from the result shows that

Table 3: Area overhead of benchmark (%)

Circuit	TFSS-LFSR (%)	TSS scheme (%)
S5378	0.45	0.42
S9234	0.57	0.50
S13207	0.68	0.60
S15850	0.75	0.73
S38584	0.91	0.89

Table 4: Test data length improvements

Circuit	L = 200 Exis. Prop. TDL (%)	L = 500E xis. Prop. TDL (%)
S5378	30300 1790 92	69000 2906 95
S9234	32400 1784 94	76000 3055 96
S13207	31800 1756 93	56000 2701 94
S15850	32400 1740 95	79500 2791 96
S38584	25200 6639 74	46000 9054 80

Table 5: Fault coverage comparison of benchmark (%)

Circuit	TFSS-LFSR (%)	TSS (%)
S27	89.61	96.32
S298	81.35	93.66
S15850	80.93	91.21
S38584	81.08	96.45

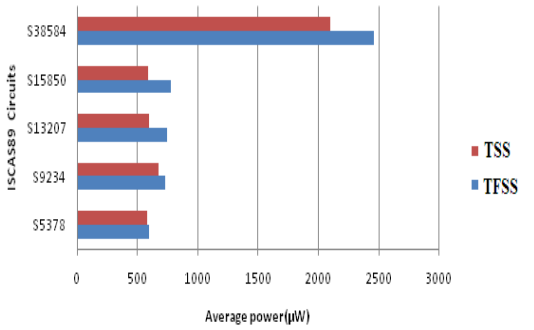

Fig. 7: Comparison of average power consumption for ISCAS 89 benchmark circuits

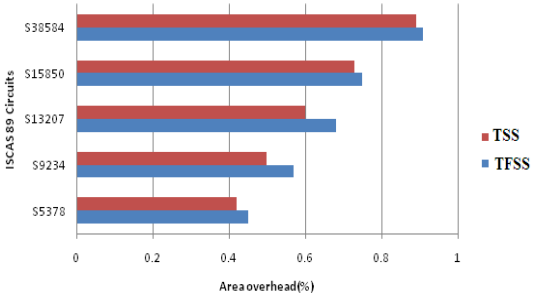

Fig. 8: Comparison of area overhead (%) for ISCAS 89 benchmark circuits

the proposed method has produced more optimized result than other methods. Table 4 illustrates the improvements in test data length reduction achieved by the proposed TSS method (using tetramax testing tool) for various values of L, S and k. Columns labeled "TDL" present the reduction percentage for each case. It can be seen that the reduction achieved by the proposed method is very high (60-96%).

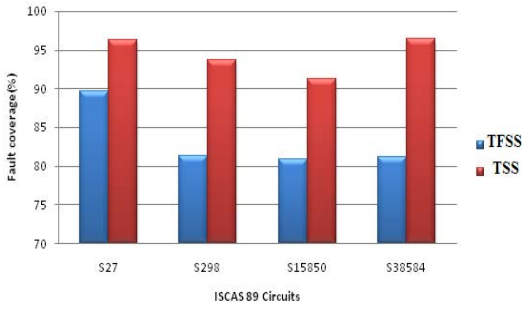

Fig. 9: Fault coverage comparison for ISCAS 89 benchmark circuits

Table 5 reported the fault coverage comparison (%) of different Benchmark circuits. Figure 9 shows the performance of fault coverage comparison for ISCAS 85 and 89 benchmark circuits. Figure 9 shows the comparative result of different parameter for Existing algorithms and proposed TSS algorithm, the result shows that the proposed method has produced more optimized result than other methods.

CONCLUSION

Three state skip-LFSR which drastically shortens the test sequence of LFSR-reseeding-based test set embedding methods was introduced. Three state skip logic incorporates a small linear circuit which estimates the next LFSR state, N cycles after the current state, shortening in this way rejects the useless parts of the test sequence. The overall system can adapt to standard fault coverage oriented ATPG with minimal computations, reduced area and power consumption. The need for optimizing the test data compression methods and test set embedding methods is offered with the proposed reduced test sequences. With the influence of this smart approach, testing in IP cores was mostly done with test set embedding methods. Fault coverage and test coverage for collapsed and un-collapsed faults were done and the test generation for these benchmark circuits was also carried out.

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