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Simplified Space Vector Pulse with Modulation Algorithm for Three Level Inverter with Neutral Point Potential Control

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Abstract: In this study, we present an algorithm for the Space Vector Pulse with Modulation (SVPWM) applied to three level diode clamping inverter. In this algorithm, the space vector diagram of the three level inverter is thought that is composed of six space vector diagrams of two level inverters. This idea allow us to generalize the two level SVPWM algorithm into the study of three level inverter. The redundant vectors of the space vector diagram of three level inverter are used to asserve the neutral point potential of the inverter.

Key words: Three level inverter, Space Vector Pulse Wide Modulation (SVPWM), neutral point potential control

INTRODUCTION

With increase of semi conductors technology, voltage source PWM inverters have been extending its application area widely. Standard two level voltage source inverter is composed of only one switching cell per phase. But in the field of high power driving systems, the level of direct current bus voltage constitutes an important limitation of the handled power. An other drawback is the very high $dv\ dt^{-1}$ generated by the two level voltage source inverter[1].

Three level inverters have more advantages than the standard two level inverters. AC-link voltage harmonics are lower due to the increase of output voltage levels. The blocking voltage of each switch is clamped to the half of DC-link voltage[2]. Performance of multilevel inverters depends on the PWM algorithm. The triangular-sinusoidal and the hysteresis PWM are dissuaded in the study of multilevel inverters because they can not deal with the major drawback of multilevel inverters which is the DC-link capacitor voltage balancing.

The space vector pulse with modulation has more advantages comparing to triangular-sinusoidal and hysteresis PWM. In space vector modulation we have more freedom to choice the sequences of the states of the inverter devices. This free choice can be used in order to minimize switching losses, to reduce output ripple or to obtain the input neutral point balancing.

Several studys apply the SVPWM to the three level inverter like koy[3-5]. These works use a typical SVPWM method, which approximate the output voltage by using the nearest three output vectors (the nodes of the triangle containing the reference vector in the space vector diagram of the inverter). When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location. Thus the computational complexity is greatly increasing with the increasing number of the reference vectors and it is a main limitation of the application of this typical SVPWM.

In this study we study a simplification of the space vector pulse with modulation for three level inverter. This simplification is made by noting that the space vector diagram of the three level inverter is equivalent to six space vector diagrams of a two level inverter. Thus we can generalize the SVPWM algorithm of two level inverter to the study of three level inverter. This simplification can reduce considerably the computational time and reduce the algorithm complexity. We use the redundancy of certain vectors of the space vector diagram of the inverter in order to ensure the stabilisation of the input DC voltages of the inverter.

SVPWM FOR TWO LEVEL INVERTER

The SVPWM strategy is proposed in by Van Der Broeck[6]. It consists of the generation of a specific sequence of states of the inverter. The reference voltage vector is defined as:

$$V^* = v_a^* \cdot e^{j0} + v_b^* \cdot e^{j2\pi/3} + v_c^* \cdot e^{j4\pi/3} \quad (1)$$

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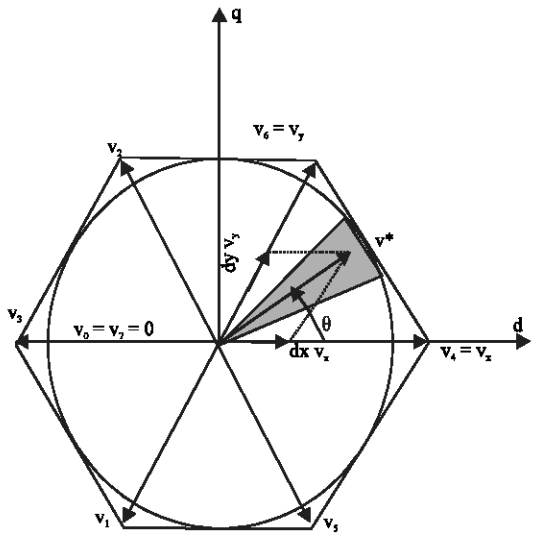

Fig. 1: Space vector diagram of two level inverter

Table 1: States of two level inverter

State	Fa	Fb	Fc	Voltage vector
0	0	0	0	V_0
1	0	0	1	V_1
2	0	1	0	V_2
3	0	1	1	V_3
4	1	0	0	V_4
5	1	0	1	V_5
6	1	1	0	V_6
7	1	1	1	V_7

where V_a* V_b* and V_c* are the reference stator voltages of phases a-c.

The vector V* can take eight positions in the complex plane according to values of the phases a-c switching signals $F_{a,b,c}$. Fig. 1 gives the complex plane of the voltage and Table 1 gives the correspondence between the switching signals and the voltage vector position. Vectors v_1-v_6 divide the d-q plane into six sectors of 60° long. In turn, each sector is divided into N equal switching intervals. Each switching interval correspond to T_s = T/N seconds, where T is the period of output voltage. In each interval, the voltage reference vector is generated by combining the two vectors v_x state X) and v_y (state Y), limiting the sector which include the switching interval, in addition to a zero sequence voltage v_z (state Z), which is v_0 or v_7:

$$V^* = d_x.v_x + d_y.v_y + d_z.v_z \quad (2)$$

The duty ratios d_x, d_y and d_z of the states X, Y and Z are calculated as:

$$\begin{aligned} d_x &= M.\sin(\pi/6-\beta) \\ d_x &= M.\sin(\beta) \\ d_z &= 1-d_x-d_y \end{aligned} \quad (3)$$

where, β is the centre angle of the given switching interval measured with respect to the beginning of the sector.

Because of the free choice of Z between v_0 and v_7, the sequence of state in each switching interval can be made in different manners. Sequences $YXZ_2/XYZ_1/YXZ_2$. where Z_1 and Z_2 are complementary v_0 and v_7, allows transition from one state to another by switching of one inverter leg only.

sTHREE LEVEL INVERTER SESCRIPTION

Figure 2 shows diagram of a three level diode clamping inverter. Each phase of the inverter consists of four switching devices and two clamping diodes. The DC supply consists of two capacities in series. Table 2 shows the switching states of each phase of the inverter.

Since three kinds of switching states exists in each phase, the five level inverter has $3^3 = 27$ switching states. Figure 3 shows the space vector representation of the output. The voltage vectors are identified as PON, PNN, etc. For example, in the study of PON, the output terminals U,V and W have the potentials E, 0 and -E respectively. There are 27 vectors in this space vector diagram, which are divided into 4 groups according to its amplitude: large vectors (e.g., PNN), medium vectors (e.g., PON), small

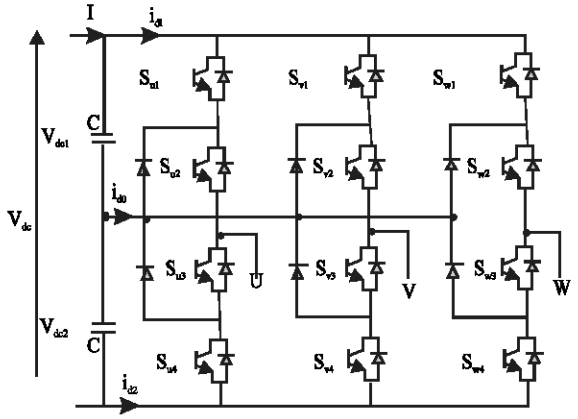

Fig. 2: Configuration of three level inverter

Table 2: States of three level inverter

Switching symbols	Switching states Sx1	Sx2	Sx3	Sx4	Output voltage
P	On	On	Off	Off	E
O	Off	On	On	Off	0
N	Off	Off	On	On	0

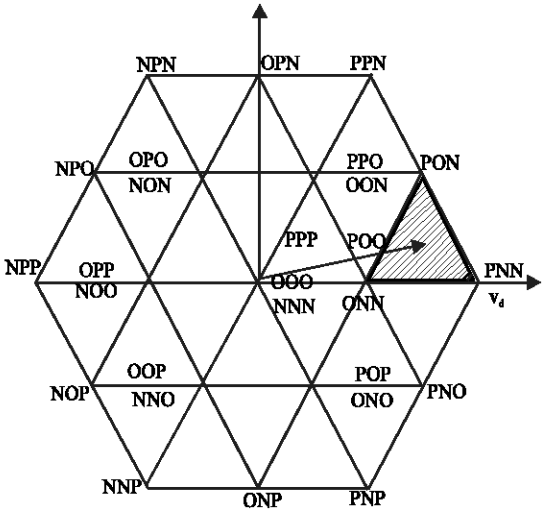

Fig. 3: Space vector diagram of three level inverter

vectors (e.g., POO) and zero vectors (e.g., NNN). Small and zero vectors are redundant, while large and medium vectors are not.

SIMPLIFIED SVPWM FOR THREE LEVEL INVERTER

The space vector diagram of a three level inverter can be thought that is composed of six small hexagons that are the space vector diagrams of the two level inverters[7]. Each hexagons, constituting the diagram of a two level inverter, centres on the six apexes of the medium hexagon as shown in Fig. 4 . To simplify the diagram of a two level inverter, two steps have to be taken. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the six hexagons. Secondly, we substrate the amount of the centre voltage of the selected hexagon from the original reference voltage.

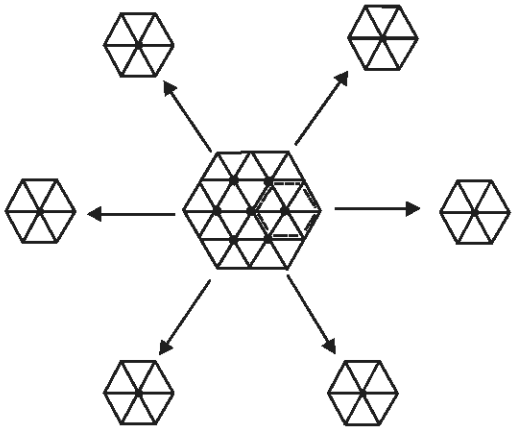

Fig. 4: Decomposition of space vector diagram of three level inverter

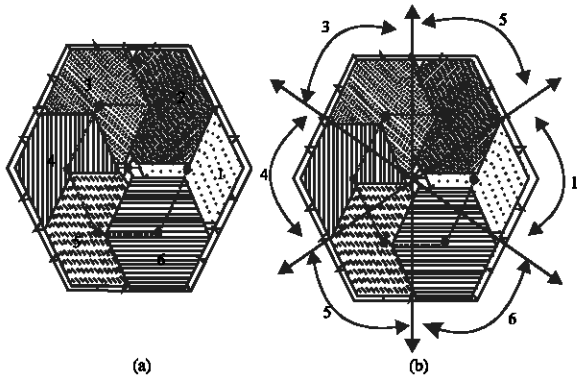

Fig. 5: Selection of hexagon's number

Correction of reference voltage vector: By the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that comprise the three level space vector diagram. There exist some regions that are overlapped by adjacent small hexagons (Fig. 5a). These regions will be divided in equality between the two hexagons as shown in Fig. 5b. In this study the hexagon number s is selected as following:

$$\begin{aligned} \overset{3}{V}{}^{*} &= \overset{3}{v}{}_{q}^{*} + i\overset{3}{v}{}_{q}^{*} \\ &= \overset{3}{v} \cdot e^{j\theta} \end{aligned} \tag{4}$$

$$s = \begin{cases} 1 & \text{if } \dfrac{-\pi}{6} < \theta < \dfrac{\pi}{6} \\ 2 & \text{if } \dfrac{\pi}{6} < \theta < \dfrac{\pi}{2} \\ 3 & \text{if } \dfrac{\pi}{2} < \theta < \dfrac{5\pi}{6} \\ 4 & \text{if } \dfrac{5\pi}{6} < \theta < \dfrac{7\pi}{6} \\ 5 & \text{if } \dfrac{7\pi}{6} < \theta < \dfrac{3\pi}{2} \\ 6 & \text{if } \dfrac{3\pi}{6} < \theta < \dfrac{11\pi}{6} \end{cases} \tag{5}$$

The index (^{3}) above the voltage vector indicates the three level space vector. Once the value of s is determined, the origin of the reference voltage vector is changed to the center voltage vector of the selected hexagon. This is done by subtracting the center vector of the selected hexagon from the original reference vector. Figure 6 shows the original reference voltage vector V^{3*} and the corrected reference voltage vector V^{3*} seen from the location of (PPO)-(OON) vectors. Table 3 gives the components of the corrected reference voltage V^{3*} for the six hexagons.

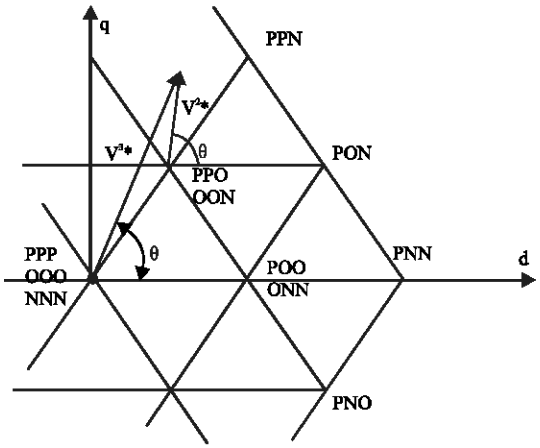

Fig. 6: Simplification of three level space vector diagram into two level space vector diagram

Table 3: Correction of reference voltage vector

s	V_d^{2*}	V_q^{2*}
1	$V_d^{3*} - 2.E.\cos(0°)$	$V_d^{3*} - 2.E.\sin(0°)$
2	$V_d^{3*} - 2.E.\cos(\pi/3)$	$V_d^{3*} - 2.E.\sin(\pi/3)$
3	$V_d^{3*} - 2.E.\cos(2\pi/3)$	$V_d^{3*} - 2.E.\sin(2\pi/3)$
4	$V_d^{3*} - 2.E.\cos(\pi)$	$V_d^{3*} - 2.E.\sin(\pi)$
5	$V_d^{3*} - 2.E.\cos(4\pi/3)$	$V_d^{3*} - 2.E.\sin(4\pi/3)$
	$V_d^{3*} - 2.E.\cos(5\pi/3)$	$V_d^{3*} - 2.E.\sin(5\pi/3)$

Switching intervals: Once the final corrected reference voltage V^{2*} and the corresponding hexagon are determined, we can apply the conventional two level space vector PWM to the inverter. The reference voltage vector V^{2*} is generated by combining states X, Y and Z. The states X and Y represent limits of the section in which the vector V^{2*} falls, while the state Z represents the center of the selected hexagon.

Because of the redundant voltage vectors of each state, we can choose X, Y and Z in several manners. This choice is generally determined by three factors: Firstly, we choose X, Y and Z in such a manner that the transition from one state to another involves switching of one device only, in order to decrease losses in the inverter. Secondly, we choose X, Y and Z in order to reduce the harmonics of the output voltage. Thirdly, we can choose the states X, Y and Z in order to control the neutral point potential of the DC-supply. Indeed, some of the redundant vectors can cause the charging of the DC-link capacitors, while some other vectors cane cause the discharging of these capacitors.

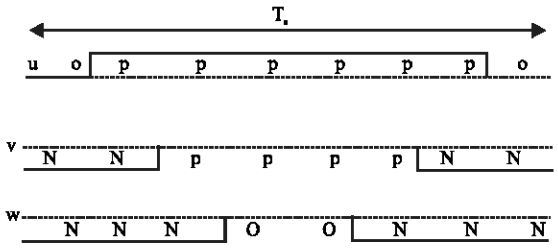

Fig. 7: Waveforms of output voltages for the hashed region in Fig. 3 in the study of sequence ZXYZYXZ

SEQUENCE OF VOLTAGE VECTORS

In order to show the influence of the choice of the states sequence on the harmonics of the output voltage we simulate the space vector algorithm for several state sequences.

Firstly, we consider the sequence ZXYZYXZ. This sequence means that in each triangle of the reference voltage vector diagram (Fig. 3), the reference voltage vector is composed by using the nodes of the triangle in turn and in reverse turn. For example, if the output voltage is in the hashed triangle of Fig. 3, the sequence of the output voltage is: (ONN)-(PNN)-(PON)-(POO)-(PON)-(PNN)-(ONN). The waveforms of phase output for the corresponding switching interval time Ts are shown in Fig. 7.

Secondly, we simulate an other sequence: ZXYZXYZ which means that in each triangle, the reference voltage vector is made by the nodes of the triangle twice in turn. For example, if the reference voltage vector is in the hashed triangle of Fig. 3, the sequence is: (ONN)-(PNN)-(PON)-(POO)-(PNN)-(PON)-(ONN).

Thirdly, we simulate the sequence ZOZXYZXYZZO that, other than the three node-vector of the triangle containing the reference vector, add the vector PPP (state ZO), which is the center of the space vector diagram, in order to synthesize the reference vector[8]: (PPP)-(ONN)-(PNN)-(PON)-(POO)-(PNN)-(PON)-(ONN)-(PPP). Starting vector and ending vector are PPP in every switching interval. So the problem of the abrupt change in output vector when passing from a triangle to another is avoided and we achieve a smooth switching of output vector: The switching states change only one step every time.

RESULTS

We simulate the association of the three level inverter with an induction motor. Table 4 gives the simulation parameters of the inverter and the motor. The

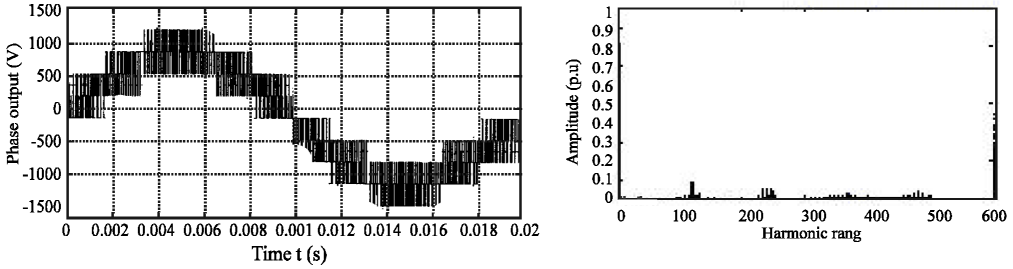

Fig. 8: Output phase voltage and its harmonics' spectrum for sequence ZXYZYX

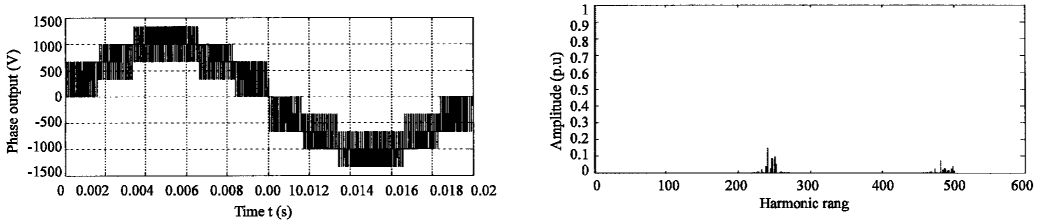

Fig. 9: Output phase voltage and its harmonics' spectrum for sequence ZXYZXYZ

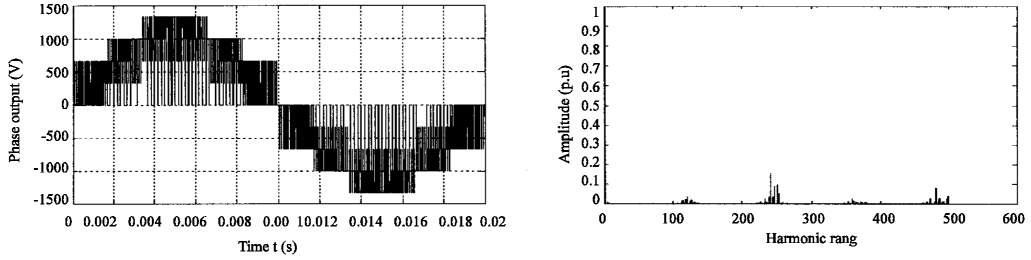

Fig. 10: Output phase voltage and its harmonics' spectrum for sequence ZOZXYZXYZZO

Table 4: Correction of reference voltage vector

SVPWM	Modulation index m = 0.8
	DC supply voltage parameters V_{dc} = 800 V
	Number of switching intervals N = 120
Induction	R_s = 3.085 Ω; R_r = 4.85 Ω ;
motor	l_s = 0.274 H; l_r = 0.274 H;
parameters	l_m = 0.258 H; p = 2; f = 50 Hz

simulation is made using Matlab-Simulink. The simulated output voltage and its harmonics spectrum for the two proposed sequences are given in Fig. 8-10. We show that the harmonics of the output voltage are centered around multiples of 50.N frequencies, where N is the number of switching intervals (here N = 120). By comparing the results given by the two sequences, we show that the second sequence (ZXYZXYZ) gives best performances, because the amplitudes of the lowest harmonics are most reduced in this study. The sequence ZOZXYZXYZZO gives less quality of harmonics' spectrum, but this is acceptable because the main goal of this sequence is to avoid abrupt changing of switching states.

DC VOLTAGE CONTROL

Problem of DC voltage variation: In the previous, it is assumed that the neutral point potential of the inverter is zero, i.e. the capacitors maintain their voltages at its set values. Indeed this assumption is not correct: If we will not taking some precautions, the neutral point potential will changing depending on the load current of the inverter.

A most accurate model of the input DC voltage of the inverter is given by following Eq.

$$
\begin{aligned}
&C\frac{dV_{dc1}}{dt} = I - i_{d1}\\
&C\frac{dV_{dc2}}{dt} = I - i_{d2}\\
&i_{d0} = -i_{d1} - i_{d2}\\
&i_{d1} = F_{11}.F_{12}.i_a + F_{21}.F_{22}.i_b + F_{31}.F_{32}.i_c\\
&i_{d2} = F_{13}.F_{14}.i_a + F_{23}.F_{24}.i_b + F_{33}.F_{34}.i_c
\end{aligned}
\qquad (6)
$$

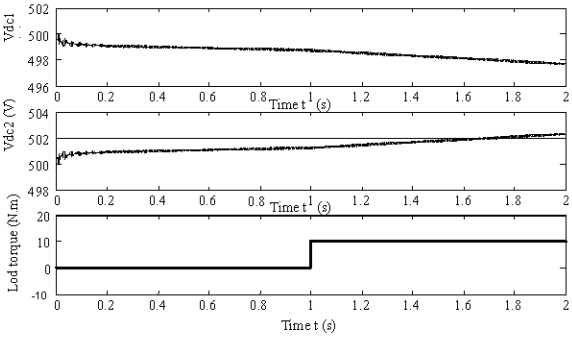

Fig. 11: Input DC voltages using positives redundant vectors only

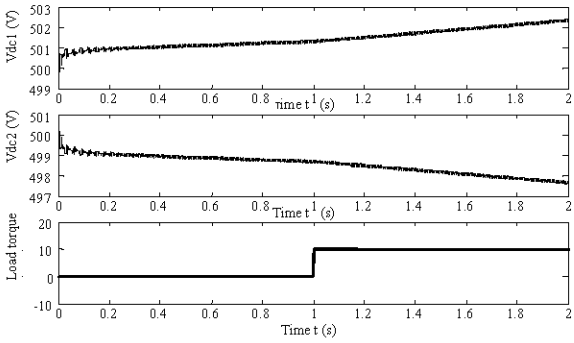

Fig. 12: Input DC voltages using negatives redundant vectors only

where V_{dc1} and V_{dc2} are capacitors voltages, i_{d0}, i_{d1} and i_{d2} are input currents of the inverter and F_{ij} (I = 1, j = 1, 4) 3 are commutation functions of switching devices (Fig. 2).

WU,[9] prove that DC input voltages will be influenced only by short and middle vectors of the space vector diagram. Those small vectors that connect phases to neutral point or negative point potential of input are called negative voltages (ONN, OON, NON, NOO, NNO and ONO), while small vectors that connect phases to neutral point or positive point potential of input are called positive vectors (POO, PPO, OPO, OPP, OOP and POP). Medium vectors also affect dc voltages. However, as they are not redundant vectors, this influence will not be controlled, being therefore considered a perturbation for the DC voltage stabilization.

To show the phenomenon of DC voltage variation, we simulate the association of DC voltage input- three level inverter and induction motor, using only one type of small redundant vectors: positives vectors (Fig. 11) or negative vectors (Fig. 12). In both two studies, we show that from the beginning, the two DC voltages V_{dc1} and V_{dc2} change from their equal initial values (500 V). This variation became very important if we apply a load torque (at time 1 second), because of the neutral point current induced by this load torque.

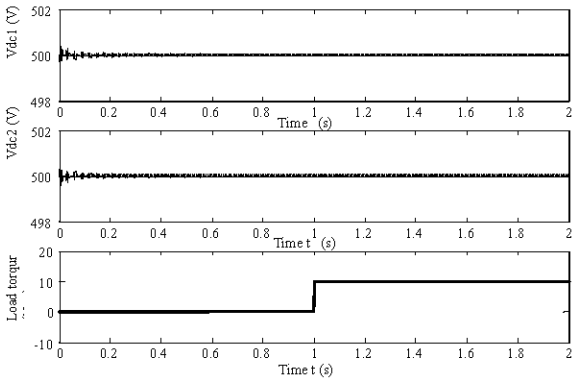

Fig. 13: Input DC voltages using control algorithm

DC voltage control method: There are two methods that Stabilize the DC input voltages. The first method is changing the switching sequence. The second is rearranging the time distribution of the voltage vectors in the switching sequence. Here, we use the first method, i.e. changing between positive and negative small redundant vectors, depending on the values of V_{dc1} and V_{dc2}. We make a continuous sensation of the difference between V_{dc1} and V_{dc2} . If V_{dc1}- V_{dc2}>0 we use positive small redundant vectors and if V_{dc1}-V_{dc2}<0 we use negative small vectors to generate The output voltage.

The simulation (Fig. 13) shows that the two DC voltages take constant values even if we apply a load torque at time 1s seconds. This results prove the efficiency of the proposed control method.

CONCLUSION

In this study, we show that we can simplify the SVPWM algorithm applied to the three level diode clamping inverter. To make this simplification, the SVPWM for three level inverter is reduced to that for two level inverter by using a coordinates change. The flexibility of the SVPWM method, which is the free choice of switching sequences and redundant vectors, allows us to reduce the harmonics of the output voltage by choosing the adequate sequence of states in each switching interval. We can also use this flexibility to ensure the balancing of the input DC voltages under any load conditions.

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