Asian Journal of Information Technology 5 (1) : 1-4, 2006

Digital and Analogue Storage Capability of Al/SIO$_2$/SI Structures

Wagah. F. Mohamad and L.S. Ali
Department of Electrical Engineering, College of Engineering,
Al-Isra University, Amman- Jordan

Abstract: Various kinds of charge storage cells are discussed as a result of examining many samples with different structures. C-V, I-V and R-V measurements of the structures confirm the storage capability of MIOS devices. The examined structures reveal three kinds of memory actions. First one is the charge storage capability which can be concluded from (C-V) curve shifting as the device exposed to certain stress for a certain time. Second is the electronic switching that is demonstrated by the fact that switching between ON and OFF states and back to original state can only be obtained by inverting the polarity of the applied bias voltage. Third kind of memory action is that the device can be switched into a variety of stable intermediate resistance states. The new resistance state is determined by the height of the programming pulse applied to the device. This memory action is noticed from R-V characteristic and known as a nonvolatile analogue memory behavior.

Key words: MIOS structures, MOS storage capability, Al/Sio$_2$/Si structures

INTRODUCTION

Essentially the memory devices are structures whose resistance and capacitance vary with magnitude and polarity of applied voltages[1]. The storage devices may be volatile or nonvolatile. They can be used as an analogue or digital memories. The MOS structure is an important type of the memory devices. Recently the shunt capacitance and shunt conductance of such structures have been studied and investigated thoroughly[2,3]. The retention and endurance of charges in the non-volatile memories depend on the oxide layer of the device. The oxide layer is the most important part in the MOS structure. This layer limits the type of the storage device.

It is known that the leakage current is responsible for enhanced charge loss in flash EEPROM memory. The leakage current is a tunneling process via neutral traps and it is induced by Fowler-Nordheim (FN) stress in MOS capacitors increases drastically when the oxide thickness decreases[2,3]. The MOS device is essential structure in flash EEPROM memory. It is more important to study the factors and parameters which influence switching and retention of memorization in MIOS structures.

MIOS DEVICE FABRICATION

The MIOS devices used in the present investigation were fabricated as follows:

After the wet chemical treatment of silicon wafers have been carried out, thermal oxides were grown thermally at 800°C in dry oxygen for time intervals of 15, 25 and 35 mins that yield silicon dioxide of thicknesses 7.75, 15.5 and 21.7 nm respectively. The oxide thickness t_{ox} was calculated from C-V measurement realized at 100 KHz. It should be mentioned that this method gives a rough estimation of the oxide thickness, but for this work there is no need for a precise measurement of oxide thickness.

The wet chemical treatment was repeated for cleaning only the back sides of all silicon wafers after thermal silicon dioxide $(SiO_2)_{th}$ growth. Then aluminum was thermally vacuum evaporated on the back side of all wafers as a back contact with thickness of 200 nm. Post-metallization annealing was carried out under vacuum for 60 min at 400°C, for making a good ohmic contact between silicon and aluminum as a back contact. Then thermal vacuum evaporated $(SiO)_d$ film of 100 nm thickness was deposited with a rate of 0.2 nm/sec on a part of the thermal grown silicon dioxide $(SiO_2)_{th}$ using a suitable mask to form $(SiO)_d$ 100 nm second insulator layer.

For other samples the second insulator layer was fabricated by thermal vacuum evaporated $(SiO_2)_d$ films of 100 nm thickness with deposition rate of 0.2 nm/sec on the thermal grown silicon dioxide $(SiO_2)_{th}$ to form $(SiO_2)_d$ 100 nm.

Corresponding Author: Wagah. F. Mohamad, Department of Electrical Engineering, College of Engineering, Al-Isra University, Amman-Jordan

For each kind of the MIOS devices, two types of gate contacts were fabricated. For some devices a strip of NiCr of 40 nm was deposited with a rate of 0.2 nm/sec on the second insulator layer using a suitable metallic mask with an aperture of 2 mm width and 20 mm length. In the last step, for all devices, aluminum gate contacts of 200 nm thick were thermally vacuum deposited through the metallic mask with (1 and 2 mm) diameter holes.

MIOS CHARGE STORAGE CAPABILITY

For the MIOS ($Al/(SiO_2)_d$100nm/$(SiO_2)_{th}$7.75 nm/p-Si) structure the high frequency (1 MHz) capacitance voltage (C-V) curves were measured before and after stress voltage to evaluate the effect of the stress on the capacitors as shown in (Fig. 1 and 2). From the high frequency C-V curves, the characteristics of the flat-band voltage shifts were obtained. The distribution of the generated interface-states densities was calculated. Before stressing, oxide charges are found to be 1.63×10^{11} charge / cm^2.

After the stress of – 10 V for 1000 sec, the C-V curve indicates the presence of the positive charge in the dioxide. The change in oxide charges are calculated after the stress and found to be equal to $\Delta V_{FB} \times C_{acc}$, i.e., ($2.6 \times 10^{11}$ charge/cm^2).That occurred because of tunneling of holes from p-type silicon substrate into the gate structure[4]. Comparing the two C-V characteristics for strip gate and dot gate samples, it is clear that the shift window in the dot gate sample approaches 2.5 V while in the strip gate sample is about 2 V.This is attributed to the more recombination of electron injected from metal gate with stored positive charges and the more tunneling back of holes near Si/SiO_2 interface into Si substrate in the strip gate sample after removing a stress voltage because of larger area and larger defects. Hence, the density of remained store charges will be less[5].

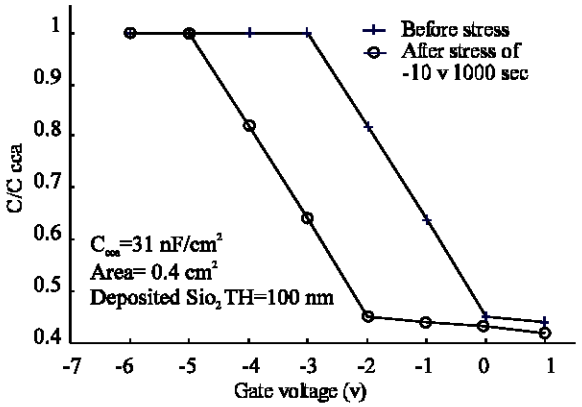

Fig. 1: MIOS C-V characteristics for thermal Sio_2 TH=7.75 nm with strip gate

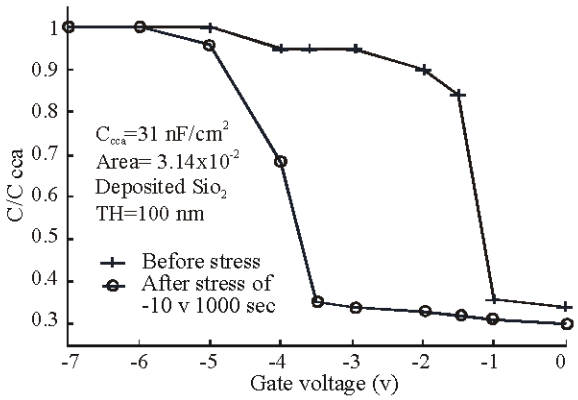

Fig. 2: MIOS C-V characteristics for thermal Sio_2 TH=7.75 nm with dot gate

MIOS DIGITAL PROGRAMMABLE RESISTOR MEMORY

Switching action of the two kinds of devices has been studied after exposing them to a stress voltage of 10 V for 1000 sec. The experimental I-V curves for each device in "OFF" and "ON" states are illustrated in (Fig. 3 and 4). It is clear from both figures that these devices exhibit memory switching[6]. Both ON-state and OFF-state characteristics extrapolate through the I-V origin. ON-state is thus retained once the bias is removed, giving a non-volatile, memory switching. By applying a negative bias the device can be switched from conducting ON-state back to the OFF-state. From the two characteristics shown, the behavior of each device differs from the other.The switching voltage from OFF-state (line AB) to ON-state (line CAD) for the device of SiO deposited insulator is between (5-6) V, while that for SiO_2 deposited insulator is between (7-8) V. In the reverse direction the switching voltage from ON-state (line CAD) to OFF-state (line EA) for the device of SiO deposited insulator is between – 3V and – 4V, while that for SiO_2 deposited insulator is between – 6V and – 7 V.

The two devices are of the same thermal tunnel silicon dioxide of 7.75 nm thickness. Difference in switching voltages is attributed to the second deposited insulator difference, because both deposited insulators (SiO and SiO_2) have the same thickness (100 nm).Forming effect in SiO deposited layer happens at a voltage less than that of SiO_2 deposited layer, i.e. the insulation reliability of SiO is less than that of SiO_2[7]. Formation of a filament may be associated with a diffusion of the top metal into the insulator layer, resulting in a dispersion of metallic atoms in the insulating (SiO and SiO_2) matrix[8].

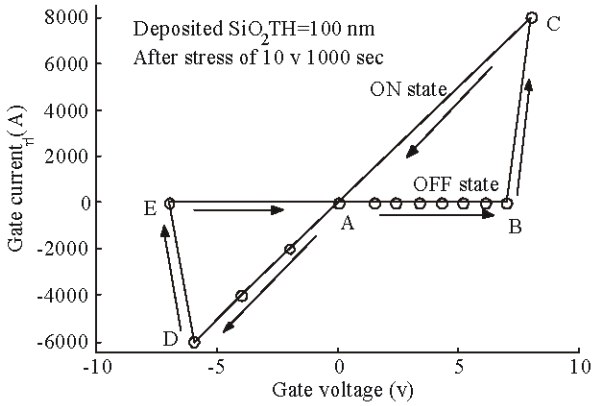

Fig. 3: MIOS I-V characteristics for thermal Sio_2 TH=7.75 nm with dot gate

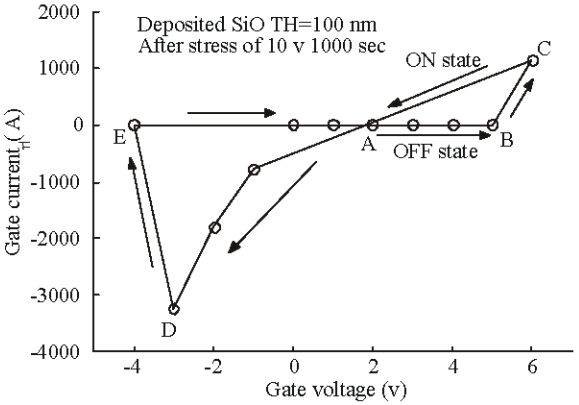

Fig. 4: MIOS I-V characteristics for thermal Sio_2 TH=7.75 nm with dot gate

MIOS ANALOGUE PROGRAMMABLE RESISTOR MEMORY

Non-volatile memory switching has been observed in Al/$(SiO_2)_d$ 100 nm/$(SiO_2)_{th}$ 21.7 nm/(p-Si) (MIOS) structure. Evidence for filamentary conduction is found for devices that are in their low impedance state. The switching phenomenon requires the existence of two impedance states which are stable at zero applied bias. The device tested showed memory switching and their initial state was one of high resistance. Fig.(5) shows analogue switching characteristic of Al/$(SiO_2)_d$ 100 nm/$(SiO_2)_{th}$ 21.7 nm/(n-Si) (MIOS) device. After the device was exposed to stress voltage of 40 V for 1000 sec., the device displayed a non-volatile, analogue memory behavior. The resistance state is determined by the height of the programming pulse applied to the device. The range of programming voltages that can be applied is referred to as the programming window. The operation of the device involves the following processes[1]:

1. Forming: This is only one time process in which a stress of 40 V for 1000 sec is applied across the device electrodes. This creates a vertical deep conductingchannel of submicron width, which can be programmed to a value in the range 500 Ω to 600 KΩ.
2. Writing: To decrease the device resistance, positive "write" pulses are applied.
3. Erasing: To increase the device resistance, negative "erase" pulses are applied.
4. The device resistance can be "read" using a voltage of less than 0.2 V without causing reprogramming.

The programming pulses (write or erase), which range between 1 V and 3 V, are typically 500 nsec width. In Fig. 5. The device resistance is seen to increase from 500 Ω toward 600 KΩ depending on the height of the erase negative pulse. The magnitude of write positive pulse is used to set final resistance of the device. Programming window is 2 V.

It is thought[9] that the current in a formed device is carried by a filament, which is less than 1 μm in diameter. Formation of a filament may be associated with a diffusion of the top metal into the amorphous SiO_2 layers, resulting in a dispersion of metallic atoms in the insulating SiO_2 matrix[10]. At Si-SiO_2 interface, when the device is in the high resistance state, it is characterized by a large device voltage and low device current. In this state the semiconductor under the tunnel oxide is deep depleted since any minority charge at Si-SiO_2 interface is effectively drained away by the tunnel-oxide. At switching point the

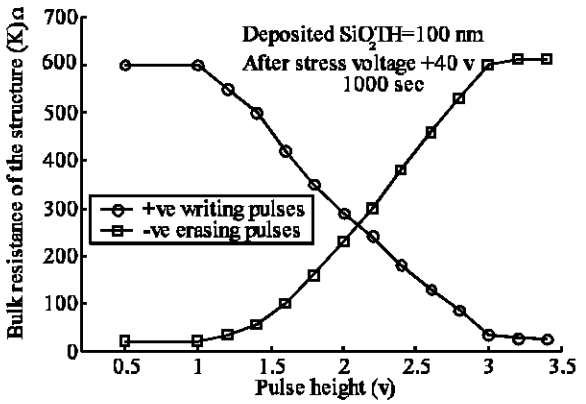

Fig. 5: MIOS bulk resistance versus applied puls height for thermal Sio_2 TH=21.7 nm with dot gate

device becomes unstable due to the initiation of a regenerative feedback mechanism[3], which collapses the width of the deep-depletion region to its strong-inversion value.

CONCLUSIONS

The examined devices manifest three kinds of memorization phenomena. The first one is the charge storage capability which can be noticed through C-V curve displacement when stressing the device. The second is the digital memory switching which is demonstrated by the fact that the switching between ON and OFF states and back can only be obtained by inverting the polarity of applied bias voltage. The third kind of memorization noticed in this work is that a device can be switched into a variety of stable intermediate resistance states. The new resistance states could be determined by the height of the programming applied pulses. This phenomenon is known as the analogue memorization.

REFERENCES

1. Murray, A.F. and L.W. Buchan, 1998. A users guide to non-volatile on-chip analogue memory, Electronics and Communication Engineering J., pp: 53-63,
2. Swart, P.L. and C.K. Campbell, 1973. Effect of losses and parasitic on a voltage-controlled tunable distributed RC notch filter, IEEE J. Solid-State Circuits, SC-8, pp: 35-36.
3. Simmons, J.G., L. Faraone, U.K. Mishra and F.L. Hsueh, 1981. Determination of the switching criterion for metal/tunnel oxide/n/ p+ silicon switching devices, IEEE Electron Device Letters, Vol. EDL-2, pp: 109-112.
4. Meinertzhgen, A., C. Petit, M. Jourdain and F. Mondon, 2000. Anode hole injection and stress induced leakage current decay in metal-oxide-semiconductor capacitors, Solid-State Electronics , pp: 623-630.
5. Huang, T.Y., and W.W. grannemann, 1982. Non-volatile memory properties of metal / $SrTiO_3$ / SiO_2 / Si structures, Thin Solid Films, pp: 159-165.
6. Shannon, J.M. and S.P. Lau, 1999. Memory switching in amorphous silicon-rich silicon carbide, Electronics Letters, pp: 1976-1977.
7. Wolf H.F., 1971. Semiconductors Copy right 1971, by John Wiley and Sons, Inc.
8. Dearnaley, G., D.V. Morgan and A.M. Stoneham, 1970. A model for filament growth and switching in amorphous oxide films, J. Non-Crystalline Solids, pp: 593-612.
9. Kroger, H. and H.A. Richard Wagener, 1980. Memory switching in Polycrystalline silicon films, Thin Solid Films, pp: 171-176.
10. Organ, D.V., A.E. Guile and Y. Bektore, 1980. Switching times and arc cathode, pp: L 35-L 38.