Asian Journal of Information Technology 5 (10): 1058-1063, 2006

On the Computer Aided Analysis and Implementation of Data Parsing Function in 56kbps Voiceband Modem

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Abstract: Due to widespread availability of twisted copper pair, 56kbps voiceband modems working over these wire lines are becoming popular day by day. Present study provides the embedded solution to one of the functional block namely Bit Parser of these modems. Its functioning resembles with the serial to parallel converter or demultiplexer. Algorithm to implement this functional block, along with simulation as well as practical results, has been presented here. Bit parser function has been implemented on Texas Instrument's based TMS320C50PQ57 DSP chip and corresponding implementation parameters have been presented in this study.

Key words: Digital signal processor, 56kbps voiceband modem, bit parser

INTRODUCTION

The world is undergoing major social and economic changes through new information processing techniques of computers and communication. The convergence of computer and telecommunication has converted this world into a digital global village. As the domains of computer and telecommunication systems are fusing with consequent blurring of their boundaries, new services are being established. These services are mainly computer based with the digital computer as a general-purpose electronic device placed at the focal point of the network for processing and forwarding information. These diverse disciplines are interwoven to produce the fabric of Information Technology (IT).

Rapid developments in the field of IT have been affecting life in all aspects i.e. education, management, research and industry. IT has revolutionized the world and shrunk it into a small Personal Computer (PC). Any type of information is now available with a single click of mouse. Information in any form (speech, text or picture) can be exchanged at any time anywhere within the world. Information Communication Technology (ICT) based applications like e-banking, e-learning, e-commerce and many other e-applications are getting wide-spread popularity due to the advancements in data communication systems.

Computers multiply their usefulness when they are able to exchange information with one another directly. The ability to link large number of computers across great distances vastly increases the access to information resources. The problem lies in finding an adequate medium over which the valuable data can be exchanged. Ideally, the Medium must be available globally, allow adequate data transfer rates and must be cost effective. At first, the logical solution may seem to be to a simple with the use of existing telephone lines for this purpose. However, there are some problems in transmiting digital information over this medium. Telephone lines used in the Public Switched Telephone Network (PSTN) or conventional phone system are designed to carry analog signals. Analog signals vary continuously along with their length and can be depicted as waves. Specifically, conventional phone lines are designed to carry the human voice. Computers are digital devices, as they communicate internally and with each other in a binary format i.e. signal having two discrete states and nothing in between, usually depicted as l's and 0's, so there is a problem in using conventional telephone lines to transmit computer information. Hence when two computers have to communicate over a conventional phone line, an intermediary device must translate the digital signal to an analog signal and another intermediary device has to translate the analog signal back into digital format for the receiving computer. This device is known as Modem and its name comes from terms Modulation and Demodulation. As the name suggests it perform modulation and demodulation on data or signal, which is to be transmitted. It accepts serial binary pulses from a device, modulates some properties (amplitude, frequency or phase) of an analog signal in order to send the signal in an analog medium and performs the opposite process, enabling the analog information to arrive as digital pulses at the computer or device on the other side of connection.

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In addition to digital/analog signal conversion, modems also control other aspects of establishing, maintaining and terminating data communications between host computers such as dialing, negotiating protocol with the remote modem and error detection/correction. In the beginning modems were used mainly to communicate between data terminals and a host computer but later the use of modems was extended to communicate between end computers. As computer technology becomes widely available to the masses, modems are playing important role in increasing the flow of information.

V.90 is the official designator for the ITU's recommendation for 56k-modem. It is the latest technology, which offers faster Internet connection speed without using expensive digital lines like T1 or ISDN[1]. Prior to this standard the modem communication across the PSTN was limited by Shannon's theorem and Quantization noise, to rates below 35kbps. Old modem technology V.34 assumes both ends to be analog and hence faces two analog-to-digital conversions in the transmission path, where quantization error occurs twice that limit data rate to 35kbps[2]. V.90 technology assumes one end (ISPs side or Servers side) to be pure digital (usually all ISPs are now connected to the network by digital lines) and other end (client or user side) to be analog, so only one analog-to-digital conversion is present. ADC and DAC are the two devices, which limit the data rates over telephone channel. Digital bit stream from analog waveform can be obtained by using a device known as ADC, which generates quantization noise and it is the major issue that limits the maximum data rate. This noise lowers the amount of information throughput. With the use of digital lines at other ends (ISPs side) there is no quantization noise and less noise directly corresponds to higher throughput. Due to the absence of one ADC V.90 technology is able to accelerate data downstream from the Internet to computers at the data rates up to 54kbps. So V.90 modem is a pair of analog (Client) and digital (Server) modem. Block diagram of basic V.90 system is shown in Fig. 1[3-7].

This study deals with the simulation and implementation of Bit Parser of V.90 digital modem transmitter as shown in Fig. 2. Bit Parser partitions the block of binary data for one mapping frame into groups of bits for processing by encoder of the transmitter. In other words it can be said that it acts like a serial to parallel converter or like a demultiplexer. It takes D input data bits from the scrambler (i.e.d_0 to d_{D-1}) and group them into S differential encoder input bits (s_0 to s_{S-1}) and K Modulus encoder input bits (b_0 to b_{K-1}) as shown in Fig. 3.

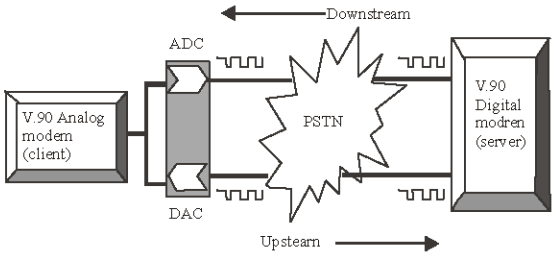

Fig. 1: Block diagram of basic V.90 system

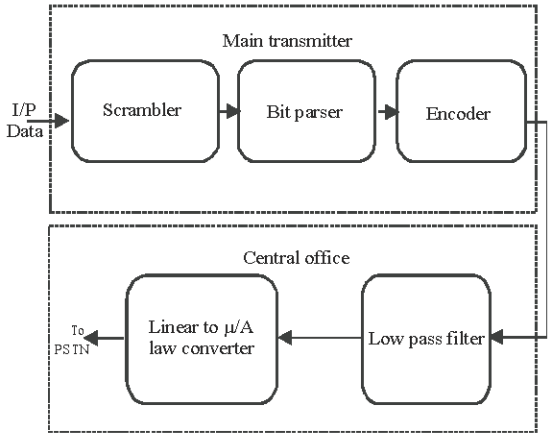

Fig. 2: Transmitter of V.90 digital modem (Server side)

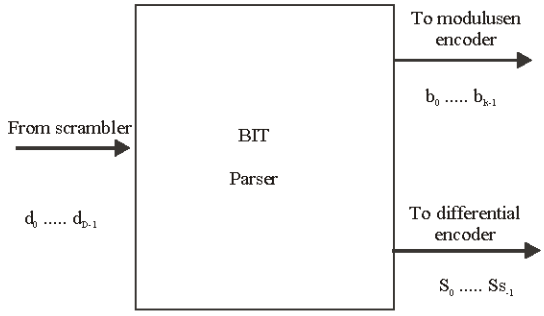

Fig. 3: Block diagram of bit parser

$$D_S = [(K+S) * 8000]/6 \quad (1)$$

Data Signaling Rate (D_S) of the modem is defined by the parameters S (the number of differential encoder input data bits per data frame) and K (the number of modulus encoder input data bits per data frame) as per Eq. 1[1] and selected during the startup phase. Data-signaling rate of the modem is selected by these parameters. Appendix (A) shows the various data signaling rates supported by 56kbps modem for different values of K and S.

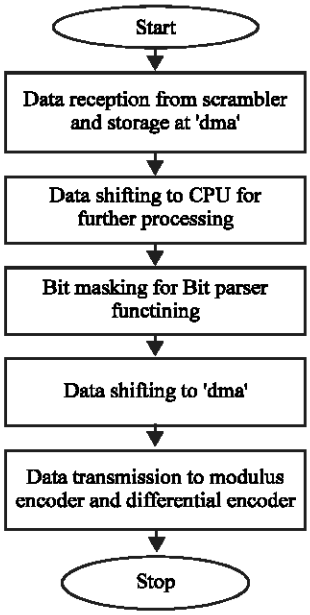

Fig. 4: General algorithm to perform bit parser function of V.90 digital modem

Specifications of bit parser: V.90 modem supports various data rates as specified in the ITU V.90 recommendation. The operating data rate as well as number of input bits D to the bit parser block is decided by the parameters K and S. Size of input data bits D used by the parser from output string of the scrambler for a particular data rate is equal to the sum of K and S bits[8].

A general algorithm for implementation of bit parser function of V.90 digital modem is given in Fig. 4. In the very first step, output of scrambler is received and stored at three different data memory locations, as the maximum value of D can be 42, which requires only three 16-bit data memory locations. In the next step, inputs stored at different data memory addresses (dma) are loaded into the accumulator one by one to perform bit masking function using AND instruction followed by a constant multiplier that mask off desired number of bits to be sent to Differential encoder (S) and modulus encoder (K). Finally masked bits are loaded into the appropriate 'dma' and further transmitted to next functional block of the transmitter.

Algorithm for implementation of bit parser: As a case study it has been assumed that modem is working at a rate of 48 kbps for which K = 33 and S = 3 so total number of bits that will enter in to the bit parser will be equal to 36. This rate was chosen because at this V.90 modem generally operated due to FCC power constraint[3]. 48 bits stream from scrambler is loaded into three different 'dma' In1, In2 and In3 and then first 16 bits out of 48 bits are loaded into the high and next 16 bits in low accumulator using appropriate instructions. As all first 32 bits have to be used by Modulus Encoder, they have been stored at 'dma' K1 and K2, respectively. 33rd bit for modulus encoder has been achieved by loading next 16 bits from third 'dma' In3 to accumulator and masking it by a constant 1. Next three sign bits can be obtained by masking the data loaded at high accumulator from 'dma' In3 with a constant 7. Another options for achieving data rate of 48 kbps requires K = 30 and S = 6[1,8]. This is the maximum rate at which previous modems i.e. V.34 standard modems were able to communicate and in fall back mode V.90 modem generally agree to operate at rate. For this rate K = 19 and S = 6 i.e., total bits D that will enter in to the bit parser will be 25 so instead of three 'dma' only two 'dma' are required. Again the program structure is same; the difference is only in constants used for masking. Similarly bit-parsing action for different data rates can be obtained by slightly modifying the program discussed earlier.

Simulation of bit parser: Source codes written in assembly (*.asm) were first converted in to the format (*.out) that Simulator of the Code Composer Studio (CSS) generally support using assembler and linker programs (mak.bat) and then were loaded in to simulator of CCS[9,10]. Here program was debugged step by step and final results have been obtained. Status of the simulator of CCS after the execution of assembly program corresponding to data rate of 48 kbps (with K = 33 and S = 3 and K=30 and S = 6) and 33.33 kbps (K = 19 and S = 6) is shown in Fig. 5 to 7, respectively.

Simulator of CCS shown in these figures contain three main windows; Dis-Assembly, Memory (data memory) and CPU and Peripheral Register window. Dis-Assembly Window shows the source codes (Instructions as well as op-codes) that have been loaded in the program memory of the DSP (in present study starting program memory address (pma) is C000 H). Memory window displays the content of data memory of the DSP. In the study of data rate of 48 kbps (with K = 33 and S = 3), output of scrambler is loaded into the 'dma' 8000H and 8001H (H means address is in hexadecimal) and output of bit parser has been stored at 'dma' 8002 H to 8005H (first 16 K-bits at 8002 H, next 16 K-bits at 8003H, last single K-bit at 8004 H and three S-bits at 8005 H). CPU and peripheral register window shows the status of all the registers and peripherals available on DSP after

Fig. 5: Simulation of bit parser function of V.90 digital modem transmitter at data transmission rate of 48 kbps with K =33 and S=3

Fig. 6: Simulation results of Bit Parser functioning of V.90 Digital Transmitter at data rate of 48 kbps with K = 30 and S=6

execution of the program. Fig. 8 shows the display of input data taken for simulation purpose and corresponding output produced by the bit parser. Results obtained so far have been found in accordance with the theoretical results. Similar study has been carried out for data rate 33.33 kbps with different data inputs and similar results have been obtained.

Implementation of bit parsing function on TMS320C50PQ57 DSP: Same source code and input data that were used during simulation have been used for practical implementation of bit parser function on DSP module. Source codes were loaded into the DSP module for two different data rates as mentioned earlier. Practical results so obtained from DSP module are in accordance with the simulated results, which confirms the successful implementation of bit parser function of transmitter of V.90 digital modem on TMS320C50PQ57 DSP[11,12]. Table 1 summarizes the data memory and program used during the present implementation along with the corresponding program execution times.

Parametric comparison for three different implementations is shown in Fig. 8 from which it can be concluded that for different values of K and S, different

Fig. 7: Simulation results of bit parser functioning of V.90 digital modem transmitter for data transmission rate of 33 1/3 kbps with K =19 and S=6

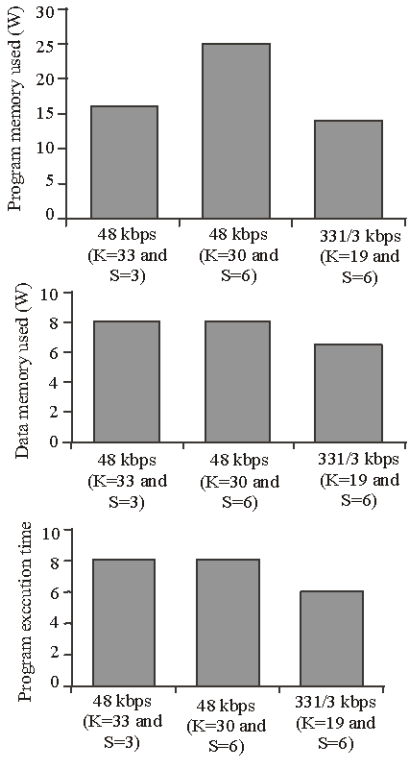

Fig. 8: Parametric comparison for different data rates with different values of K and S

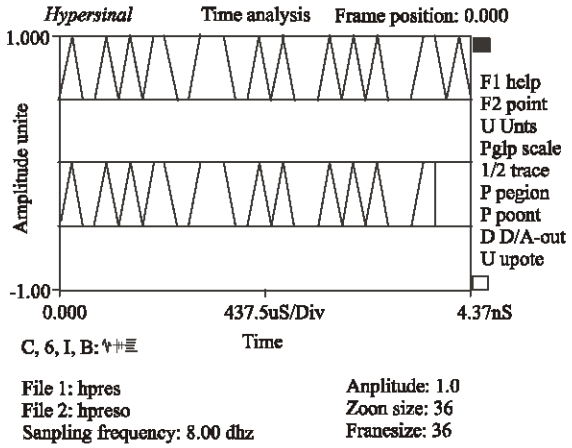

Fig. 9: Time domain display of D and K bits of bit parser for K=33 and S_r=3

Table 1: List of various parameters of bit parser of V.90 digital modem transmitter calculated against different data rate

Rates (kbps)	Program Memory Used (W)	Data memory Used (W)	Program execution (ms)
48 (K=33 and S=3)	16	8	0.2807
48 (K=30 and S=6)	25	8	0.4386
33.33 (K=19 and S=6)	14	6	0.2456

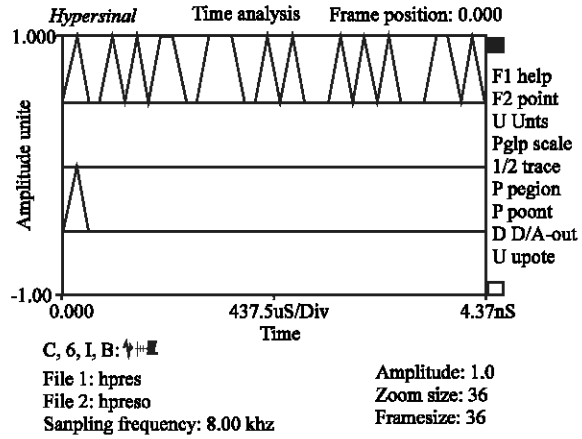

Fig. 10: Time domain display of D and S bits of bit parser for K=33 and S_r=3

memory spaces are required and program execution time also depends on these values. Similarly bit parser for another combination of K and S can be implemented and will have different implementation parameters. Fig. 9 displays the input given to the bit parser and corresponding K output for the study K = 33 and Sr = 3 and display of corresponding S output for the same input is given in Fig. 10. From these figures, which have been obtained with the help of Signa logic DSP Software, accurate working of bit parser function of V.90 digital modem can be confirmed for above-mentioned combination and similar results has been obtained for other combinations[13].

Appendix (A): Data signaling rate defined by the parameters K and S

K, bits entering modulus encoder	S, sign bits used for user data		Data signalling rate, kbit/s	
	From	To	From	To
15	6	6	28	28
16	5	6	28	29 1/3
17	4	6	28	30 2/3
18	3	6	28	32
19	3	6	29 1/3	33 1/3
20	3	6	30 2/3	34 2/3
21	3	6	32	36
22	3	6	33 1/3	37 1/3
23	3	6	34 2/3	38 2/3
24	3	6	36	40
25	3	6	37 1/3	41 1/3
26	3	6	38 2/3	42 2/3
27	3	6	40	44
28	3	6	41 1/3	45 1/3
29	3	6	42 2/3	46 2/3
30	3	6	44	48
31	3	6	45 1/3	49 1/3
32	3	6	46 2/3	50 2/3
33	3	6	48	52
34	3	6	49 1/3	53 1/3
35	3	6	50 2/3	54 2/3
36	3	6	52	56
37	3	5	53 1/3	56
38	3	4	54 2/3	56
39	3	3	56	56

CONCLUSION

During the present study an algorithm to implement bit parser functioning in the transmitter of 56kbps voice-band modem was developed and corresponding source code were written. Simulation was performed to debug the source codes and after debugging, with the help of reference data, theoretical (simulated) results were obtained. Same source codes were loaded in the DSP chip and practical results were obtained for different data rates. Practical results were found be in accordance with the theoretical results which confirms the successful implementation of bit parser on DSP chip. Implementation parameters like Program memory and data memory used along with program execution times were calculated and were found to be different for data rates.

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