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Contribution to Definition of a Structured Design Methodology of Mixed Circuit

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Abstract: This research concerns a set of proposals in order to structuring the design of MOS analog VLSI. They are derived from structured logic design methods, which have shown their great efficiency. We propose, by using NMOS inverter as linear amplifier, a simple method to go from functional to structural description. So it was possible to confirm that the designed circuit will work exactly as it was predicted by functional simulation results. This method has been, successfully and efficiently applied to the design of a PLL.

Key words: Structure design, mixed, integrated circuit,functional simulation,structure simulation

INTRODUCTION

The Metal Oxide semiconductor Field Effect Transistor, MOSFET, introduced in 1960 promised the potential of a simple device, that could be integrated on a large scale in digital integrated electronics. However, bipolar technologies have been preferred over MOSFET technologies for analog applications because of better device matching that result in lower differential offset voltages, higher transconductance, g_m, better frequency response. But the rapid increase in chip complexity which occurred over the past few years has created the need to implement complete analog/digital subsystems on the same integrated circuit using the same technologies. For this reason, implementation of analog function in MOSFET technology has become increasingly important.

The intent of this study is to find a unified approach for design analog and digital circuit. The choice, is fixed on a load-depletion inverter cell in NMOS technology. The goal of this approach is to simplify and to accelerate the design of analog circuit, which is often the most time consuming part in the design of a mixed system. Following this approach, the design, is done in a hierarchical way, starting from the functional description. To illustrate the approach proposed, we chose to analyze a PLL (Phase Locked Loop) circuit (Gadner, 1966). Two simulations functional and structural are examined to investigate the performance of the PLL, in particular, locked conditions. A comparison between these simulations is considered to put into evidence the efficiency of this approach.

SITUATION OF PROBLEM

Advances in the linear circuit domain are not so well investigated due to the nature of linear circuit, which differ markedly from digital circuit in that, there are no universal building blocks equalling to the gate in digital circuit. Therefore, the change from level functional to structural one is relatively difficult because there is not a basic common structure for all analog blocks. To overcome the difficulty of designing mixed circuit Analog/Digital a basic cell sufficiently simple and common for 2 applications should be found. Our choice to carry on the inverter cell in NMOS technology configured for the treatment of analog signals (Gray and Meyer, 1984; Haskard and May, 1985). Thus, we can progress in the same way for both parts. The programming of simple parameters transistors allow the obtention of desired circuit as shows the chosen PLL example.

BASIC CELL

With reference to Fig. 1a, the basic cell consists of an enhancement and depletion transistor connected in inverter, mode depletion load. The region of interest for analog amplification is that in which, both transistor are saturated to achieve high transconductance and low conductance. The Fig.1b shows the transfer function V_{out} (V_{in}), where both transistors operating in this region.

According to the Shishman and Hodges (Drennan and Andrew, 2003) model, level 1 for an MOS transistor operating in the saturation region, the drain-source current is given by the equation:

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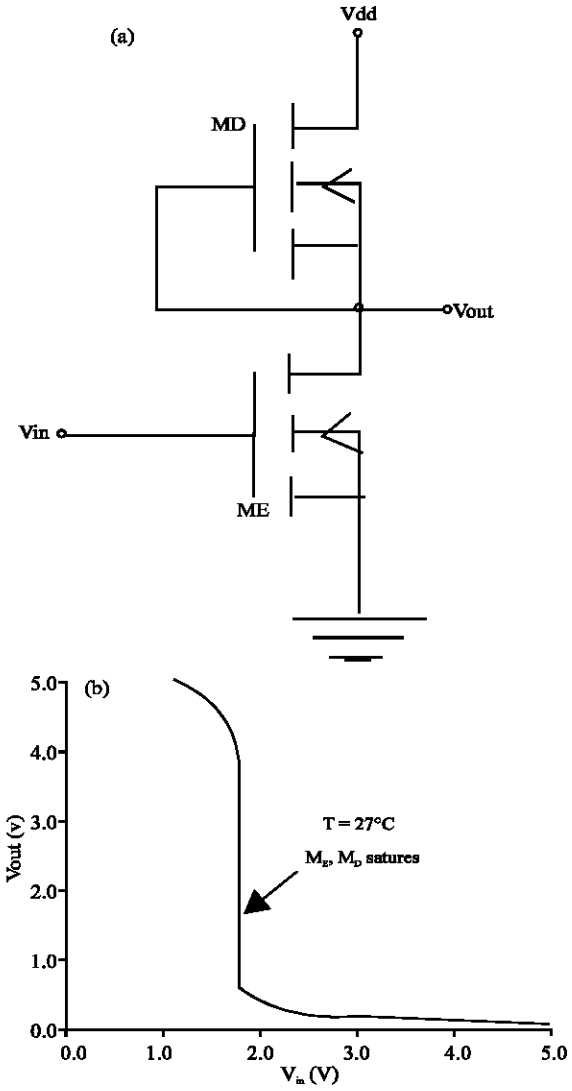

Fig. 1: (a) Basic cell, (b) Transfer function

$$I_{ds} = K\frac{W}{L}(V_{gs} - V_{th})^2(1 + ?V_{ds}) \quad (1)$$

Where,

K_p : Intrinsic transconductance (in A/V^2)
W : The width of transistor (im)
L : The length of transistor (im)
V_{gs} : The gate-source voltage (V)
V_{to} : The threshold level voltage (V)
λ : The channel length modulation parameter

The relationship between the threshold voltage and the body bias V_{bs} is given by:

$$V_{th} = V_{to} + \gamma(\sqrt{V_{bs} + 2\varphi} - \sqrt{2\varphi}) \quad (2)$$

Where the process parameters are:

V_{to} : The threshold voltage for $V_{bs} = 0V$
V_{bs} : The substract-source voltage
γ : The body effect factor
φ : The Fermi level

If both transistors are identical and if body effect and channel-length modulation, are neglected, the small signal-voltage gain is simply the ratio of the transconductance of the enhancement transistor M_E to the transconductance of the depletion transistor M_D, i.e, the square root of the ratio of the W/L ratios:

$$A_V = -\frac{g_{mE}}{g_{mD}} = \sqrt{\frac{(\frac{W}{L})_E}{(\frac{W}{L})_D}} \quad (3)$$

It can be noticed that the voltage gain only depends of the ratio W/L of both transistors M_E and M_D.

APPLICATION OF THE PLL MODEL

PLL is a typical mixed circuit whose principal function is to adjust, the phase produced signal of the voltage controlled oscillator to the phase of the incoming signal. The PLL is modelled, by its three basic functions as shown in Fig. 2: Phase Detector (PD), Low-Pass Filter (LPF) and Voltage-Controlled-Oscillator (VCO):

- The phase detector is the digital part, composed by an XOR circuit. It supplies the error voltage $V_d(t)$ proportional to the phase difference of the input signal and the output VCO signal. Its gain K_d is the variation of the error voltage to the variation of the phase.
- The low-pass filter, defined by it time constant, ô, generates the average error voltage $V_f(t)$ to the VCO control input.
- The VCO is the analog part. It supplies an output signal $V_{vco}(t)$ whose frequency is directly proportional to the control voltage V_f (t). Its gain K_V is the variation of the frequency to the variation of the control voltage.

An important aspect of the PLL performance is the capture range. It is that we will valid using 2 simulations functional and structural.

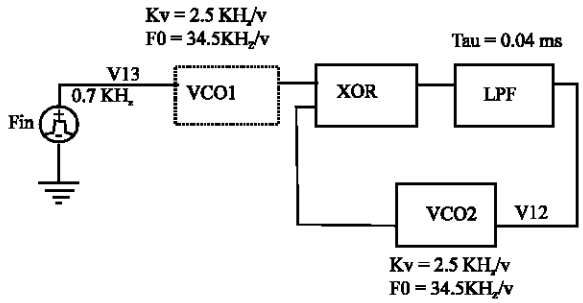

Fig. 2: Block diagram of functional model PLL

APPLICATION OF FUNCTIONAL MODEL

In order to characterise PLL performances, TESS program (Derennan and Andrew, 2003) is used to simulate the functional model. Each block of the PLL (Fig. 2) comes from the TESS library, via an arbitrary choice of specific VCO parameters indicated below:

Central frequency : F_0 = 34.5 kHz
Minimal frequency: F_{min} = 24 kHz
Maximal frequency: F_{max} = 48 kHz
Output voltage : V_{out} = 10V
VCO gain : K_v = 2.5 kHz/V
Voltage corresponding to F_0: V_0 = 5V.

The first characterisation consists of model simulating via an incident signal of the same frequency as the VCO central frequency. Figure 3 shows the dynamic of the PLL capture. It can be, seen that the output (V_{12}) of the loop filter goes through a peak whose value is 8V, then decreases to 5V, a value that well corresponds to the central frequency. The nonlinear characteristic of the loop filter is responsible for the appearance of the peak of control Voltage (V_{12}) prior to PLL locking on the central frequency occurring after 0.4 ms.

The second characterisation consists of the application of a step frequency at PLL entry. The test model as shown in Fig. 3, uses a second VCO_1 connected the incident PLL input, having the same parameters as VCO_2 in the PLL. Then, it suffices to apply a step voltage varying between 7V and 3V to the input (V_{13}) of external VCO_1. Figure 4 gives the response at a step frequency, e.g., 0.7 kHz around the central frequency.

It can always, be noticed that the output (V_{12}) of the loop filter goes through a peak, which is attenuated to reach the square signal (V_{13}) of the PLL input; this shows the new PLL locking with the step frequency. We can remark on each waveform, the situation where the VCO frequency F_V has become closer to the frequency input F_{in}. Thus, we determine that the capture range of the PLL, is situated between 27 kHz and 40 kHz.

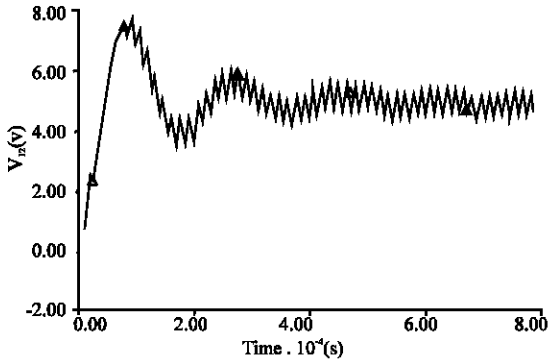

Fig. 3: PLL model response for F_{in}=F_0=34.5 kHz, without VCO1

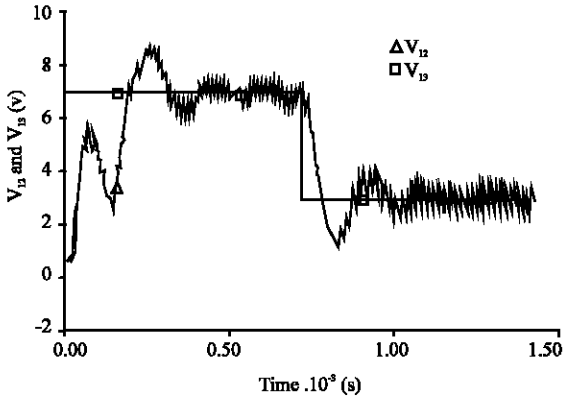

Fig. 4: Response PLL at a step frequency with VCO1 connected

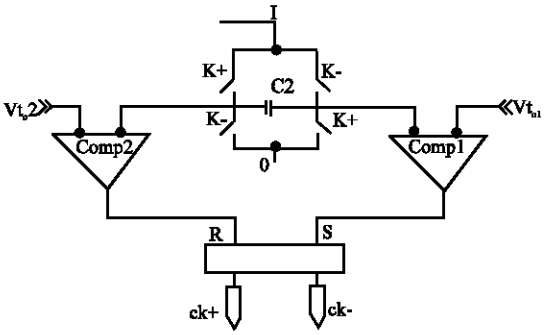

Fig. 5: Differential structure of the VCO circuit

APPLICATION OF STRUCTURAL MODEL

For a more detailed analysis of the PLL, this study describes, how we decomposed it into sub-modules, simple enough, which can be implemented, into basic inverter. We will now discuss the hierarchical design of important analogue block, which is the VCO.

A fully differential architecture is employed in Fig.5. The VCO circuit consists of a current mirror I, two

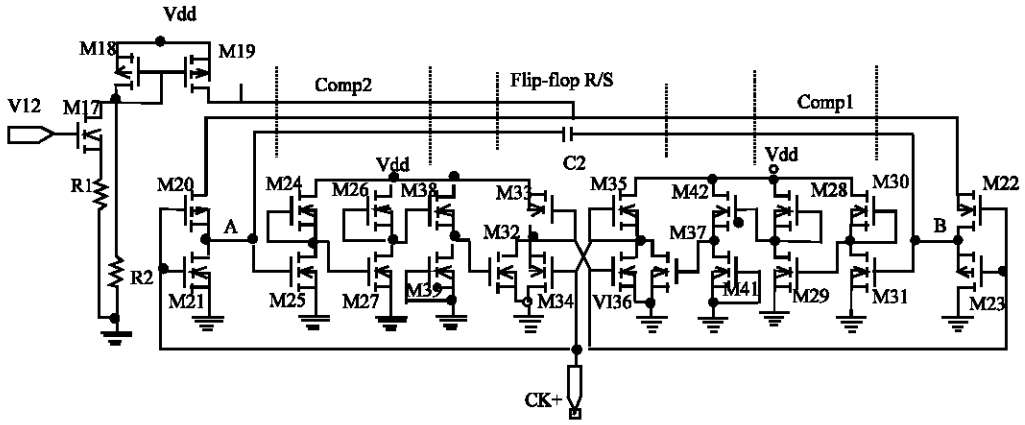

Fig. 6a: VCO Integrated structure

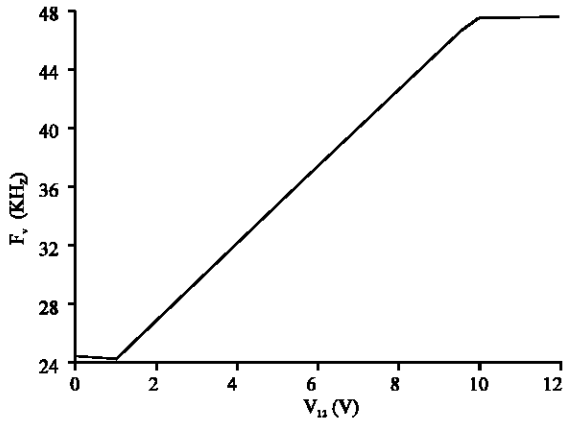

Fig. 6b: Voltage-to-frequency transfer characteristic VCO for R_1=R_2=10kΩ

voltages reference Vto1 and Vto2. Each of these drives a voltage comparator $comp_1$ and $comp_2$ and S/R flip-flop block; ck^+ and ck^- are switching signals derived from the S/R flip-flop that steer the polarity of the charging current through the capacitor C_2 via the differential pair switching k-and k+. A more detailed structure of the VCO is shown in Fig. 6a.

The VCO circuit functions as follows. The transistor M_{17} and the external resistor R_1 form a source follower. The current through R_1 is linearly dependent on the VCO input voltage V_{12}. This current flows through the transistor M_{18}, which, together with the transistor M_{19} forms a current mirror. External resistor R_2 adds an additional constant current through the transistor M_{18}, this current offsets the VCO operating frequency. The S/R flip-flop composed of transistors (M_{32} to M_{37}) turns on, either les transistors (M_{20}, M_{23}) or (M_{21}, M_{22}) which operate as switching. One side of the external capacitor C_2 is, therefore hold at ground, while the other side, is charged by the current I supplie by the transistor M_{19}. As soon as C_2 charges to the point (V_{to}= 0.9V) at which the voltage comparator (M_{24} to M_{27}) or (M_{28} to M_{31}) is reached, the flip-flop changes state. The charged side of the capacitor is now, pulled to ground. The other side goes negative and discharging rapidly. Subsequently, a new half cycle starts. The timing is determined by the charging of capacitor. It swings from a threshold $+V_{to}$ to $-V_{to}$ during a half cycle. Here V_{to} represented the threshold voltage of the differential pair switching transistors. Using the relation $I = C_2.dV/dt$, the VCO is modelled to deliver the following output frequency:

$$F_V = \frac{1}{T} = \frac{I}{4C_2V_{to}} \quad (4)$$

The values of frequency F_{max} and F_{min} specified above allowed us to calculate the resistors R_1 and R_2 (10 kΩ) for a 10nF capacitor C_2. The values of the VCO frequency are plotted as a function of the control voltage V_{12} (Fig. 6b).

The important observation here is the high linearity of the VCO characteristic from F_{min} to F_{max} frequencies; this occurs over all the values range (1V-10V) of the input control voltage V_{12}. We also remark that the range frequency is between (24 kHz - 48 kHz), the gain (K_v=2.6 kHz V^{-1}) deduced from Fig.6b and that, the central frequency is equal to 34.5 kHz for a voltage V_{12}= 5V. These results are in agreement with the specifications chosen in functional simulation.

RESULTS AND DISCUSSION

The complete architecture of the PLL circuit is shown in Fig. 7. It is realised of an arrangement of repetitive basic cell inverters, each one containing two MOS transistors. The phase detector, which constitutes the digital part, is a XOR circuit composed of four NAND gates. Its

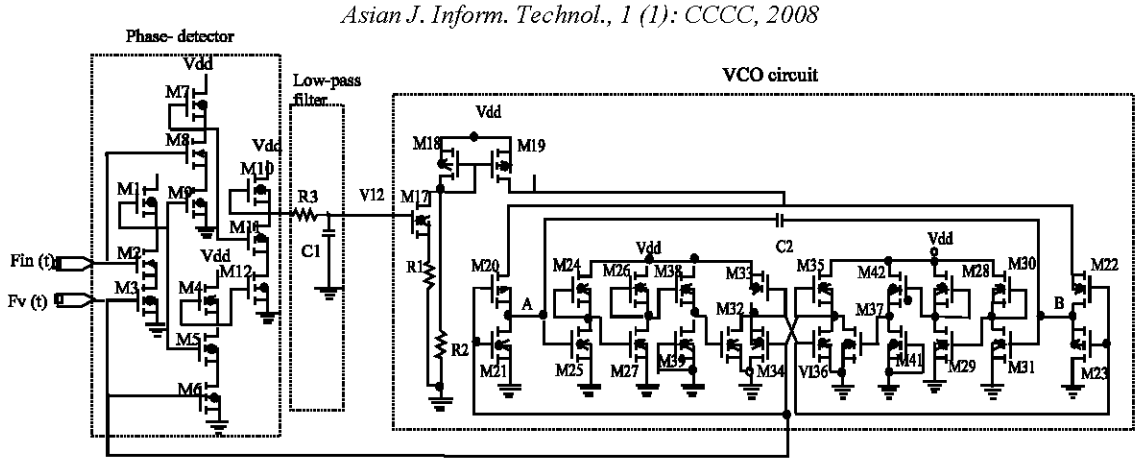

Fig. 7: The completed structural schema of the PLL circuit

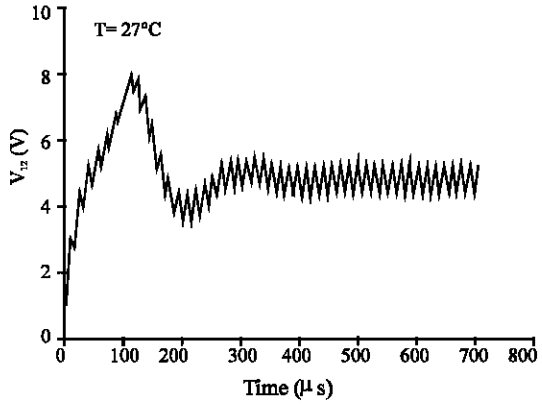

Fig. 8a: Response of the structural model PLL for F_{in}=F_0 =34.5 KHz, without VCO1

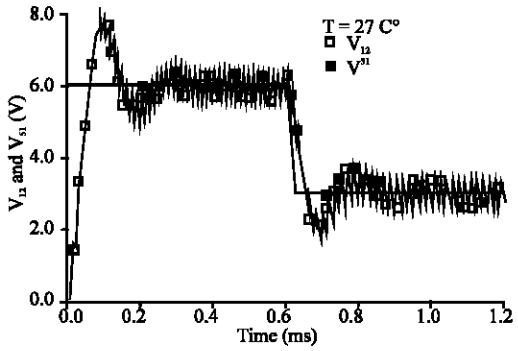

Fig. 8b: Response of the structural model PLL at a step of frequency with VCO1 connected

integrated structure is shown in Fig. 7. For the analog part, the voltage comparator is, implemented using two cascade stages to achieve high voltage gain to maximise speed commutation. The third stage is a simple level-shifter circuit to compensate the delay time through the flip-flop and to maintain the voltage across the capacitor constant equal at V_{to} (0.9V). The flip-flop is, constructed using two inverters driving each other, it provides a valid square output to drive the two differentially pair switching. Finally, the loop filter is realised through external parts, because of the radical configuration changes from one application to another. The time constant τ = 0.04 ms permit us to calculate the R_1 = 20kΩ for a capacitor C_1=2nF. Our PLL circuit is designed for operating at a single 10V supply.

Table 1: Process parameters and devices geometries

Transistors	V_{to} (V)	W (µm)	L (µm)	
M1,4,7,10	-2.5	6	60	PD
M2,3,5,6,8 M9,11,12,	0.9	80	5	
M18,19,20,23	-0.9	6	60	
M17,21,22,	0.9	80	05	VCO
M24,26,28,30 M33,36,39,41,	-2.5	6	60	
M25,27,29,31,32 M34,36,37,38,42,	0.9	80	5	

Table1: Process parameters and devices geometries

For the carried out simulation we assume that the enhancement and depletion transistor have the same intrinsic transconductance (K = 2E-3) and they are biased with (V_{gs}-V_{to} = 0.2V). Using, these NMOS process parameters the different geometries of device are calculated and listed in Table 1.

The completed schema of the PLL, can be simulated at structural level, using MOS1 in PSPICE program. The response of the PLL model, for the same input frequency F_{in} = F_0 is shown in Fig. 8a. For, the step of frequency we use an external VCO1. Its integrated structure is identical to that of the internal VCO2. The response of the PLL is shown in Fig. 8b, after applied an input signal V_{51} varying between 6 and 3V. We can remark on each waveform, the situation where the VCO frequency has become closer to the frequency input. They are in

excellent agreement with those obtained by TESS program and the capture range is equally between (27 and 40 kHz).

CONCLUSION

The design philosophy outlined is relatively simple it allows the simple incorporation of digital and analog circuits on the same chip and to employ the same standard NMOS process. The verification done, on the PLL circuit, using functional and structural simulation, with a minimum of specification parameters, shows very good agreement, considering the simplicity of our approach and the complexity of the transient behaviour of the PLL. Moreover, the comparison of the present results put into evidence the validity of this methodology, so the concept can be extended to produce a larger circuits.

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