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An FPGA Based Implementation of CA-CFAR Processor

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Abstract: In this study, a constant false alarm rate processor is investigated and a special focusing is devoted to the Cell-Average Constant False Alarm Rate (CA-CFAR) processor. This processor is analyzed and its performance is estimated. An FPGA-based CA-CFAR processor has been implemented using Xilinx integrated circuit chip XC9600. The implemented processor using this technique has been tested with signals imbedded with different types of clutter and noise-alike signals. The implementation process and the processor response reflect how this digital tool is excellent due to its high reliability and flexibility.

Key words: CFAR, FPGA design, signal processing

INTRODUCTION

The received signals in (or out) any detection device are usually buried in thermal noise and clutter, which refers to any undesired signal echo that is reflected back to the receiver by buildings, clouds, the sea, etc. Since the clutter-plus-noise power is not known at any given location, a fixed-threshold detection scheme cannot be applied, if the false alarm rate is to be controlled. An attractive class of schemes that can be used to overcome the problem of clutter are the Constant False Alarm Rate (CFAR) processing schemes which adaptively set the threshold based on local information of total noise power. The threshold in a CFAR detector is set on a cell basis using estimated noise power by processing a group of reference cells surrounding the cell under investigation. The Cell Average Constant False Alarm Rate (CA-CFAR) processor adaptively sets the threshold by estimating the mean level in a window of (M) range cell. The CA-CFAR processor is the optimum CFAR processor (maximizes detection probability) in a homogeneous background when the reference cells contain Independent and Identically Distributed (IID) observations governed by an exponential distribution (Barkat, 2005). As the reference window is widened, the detection probability approaches that of the optimum detector which is based on a fixed threshold. The Cell Averaging (CA) technique is outlined schematically in Fig. 1 (Skolnik, 2001; Weiss, 1982).

PERFORMANCE EVALUATION

From the equations of P_d, P_{fa}, CFAR losses and ADT in reference (Gandhi and Kassam, 1988; Nadav, 1988) Table 1, present numerical evaluation values of α and

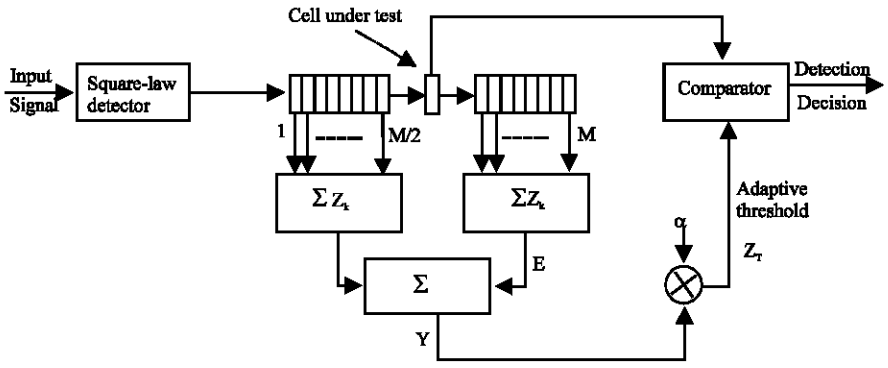

Fig. 1: Cell-Average CFAR (CA-CFAR) technique

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Table 1: Constant scale factor T and Average Detection Threshold ADT of CA-CFAR processor and ADT of optimum fixed threshold processor

	Optimum	M = 8		M = 16		M = 24		M = 32	
P_{fa}	ADT	α	ADT	α	ADT	α	ADT	α	ADT
10^{-4}	9.21	2.162	17.3	0.778	12.45	0.468	11.23	0.334	10.673
10^{-6}	13.8	4.623	37	1.371	21.94	0.778	18.68	0.54	17.278
10^{-8}	18.42	9	72	2.162	34.6	1.154	27.71	0.778	24.905

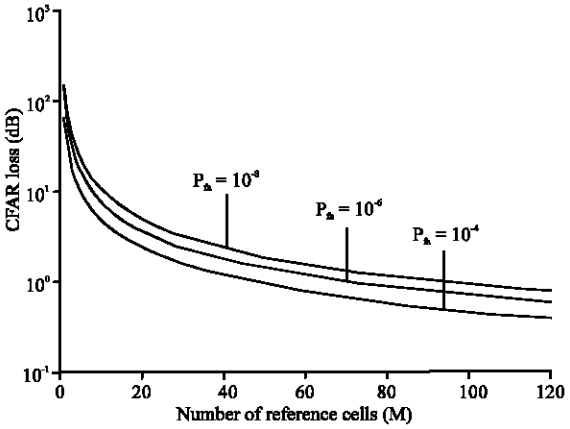

Fig. 2: Theoretical CFAR loss as a function of number of reference cells (M)

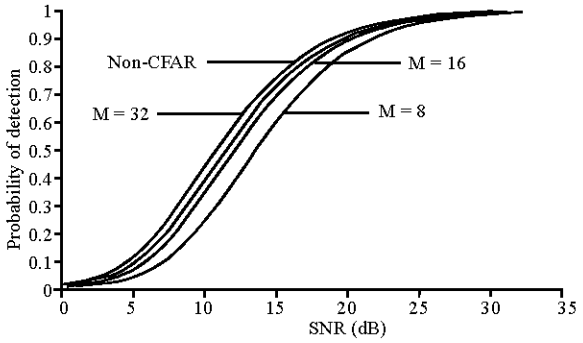

Fig. 3: Performance curves for CA-CFAR with window size (M) as a parameter for $P_{fa} = 10^{-6}$

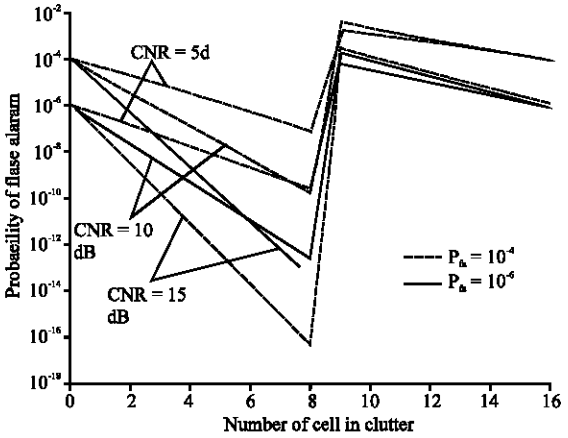

Fig. 4: False alaram rate performance of the CA-CFAR processors in clutter power transition

average detection threshold *ADT* corresponding to certain values of *M* for different values of probability of false alarm, P_{fa}. It's clear from this table the relation between *ADT*, α, P_{fa} and *M*, where, when *M* increase α decrease and *ADT* also decrease for different values of P_{fa}. A compromise must be adopted to choose the value of *M*, not to be along to lessen the detection loss. Figure 2 and 3 demonstrate the performance curves of the CA-CFAR processor.

DESIGN OF CA-CFAR

Based on the previous results the following parameters can be chosen for suitable operation for the system was shown in Fig. 1. These parameters are foundto be $M = 16$, $P_{fa} = 10^{-6}$ and $\alpha = 1.371$ and the decision will be as;

- If { Y > αy }then target is present and the threshold value (αy) is loaded in the cell under test before shifting the contents of all cells
- If{ Y < αy }then target is not present and the contents of all cells are shifted by one resolving

RESULTS AND DISCUSSION

The probability of detection P_d increases linearly as *SNR* increases. On the other hand as the number of the cells coming from heavy clutter, *R*, increases, P_d decreases. The loss for $P_d = 0.5$ and *INR* = 5 dB is increases by about 4 dB at extraneous target $R = 10$ to 7.25 dB at $R = 24$, while this loss is about 12.5 dB and 15.5 dB for the same values of *R*, but interference-to-noise ratio *INR* = 15 dB. This loss can be considered large, since 13 dB is needed to detect the target with $P_d = 0.5$ and $P_{fa} = 10^{-6}$, while P_d at this value approaches to zero for *INR* = 15 dB, so, the performance of these processors degrades rapidly in nonideal conditions.

The P_{fa} exhibits a sharp discontinuity at $R=M/2$. The dip in P_{fa} from cells 1 to 8 is caused by the right-hand edge of the thresholding set being the heavy clutter region. This raises the threshold even through the test cell is in the thermal noise region. On the other hand, the

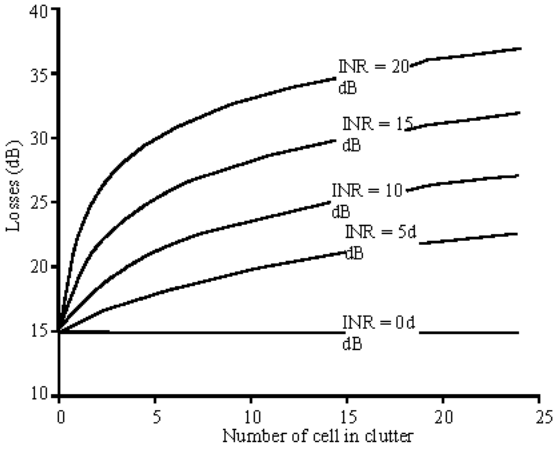

Fig. 5: CA-CFAR loss in the presence of interfering targets (M = 16, P_d = 0.5, P_{fa} = 10^{-6})

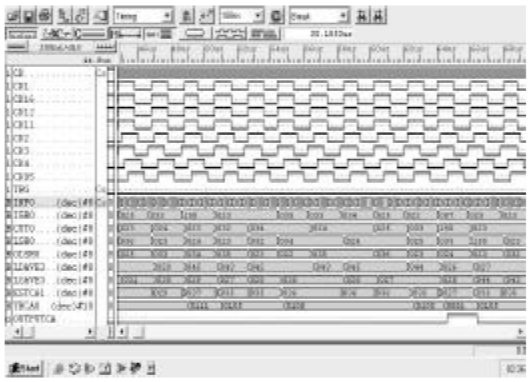

Fig. 6a: The simulation results of the (CA-CFAR) processor for single target

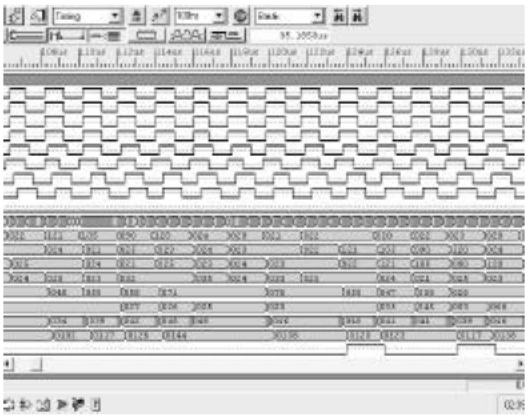

Fig. 6b: The simulation results of the (CA-CFAR) processor for multipul target

cell under test being in a heavy clutter region causes the sharp spike in P_{fa} from cell 9 to 16, but the left-hand edge of the thresholding is caused by a light clutter region. This lowers the threshold and allows a large increase in P_{fa}. Referring again to Fig. 4 it should be clear that the degradation in the CA-CFAR performance at clutter edges increases as the *CNR* increases. The detection probability as a function of the interference-to-noise ratio at M = 16, P_{fa} = 10^{-6}, *SNR* = 20 and 40 dB and for different values of interfering targets (R). It can be seen that as *INR* increases the P_d decreases, while for smallest number of interfering targets, the P_d increases and the processor performance becomes better than the multiple targets case. The detection probabilities for *SNR* = 40 dB are higher than the case of *SNR* = 20 dB.

Figure 5 shows the CA-CFAR loss in the presence of interfering targets as a function of number of cells lying in clutter. The displayed results show that, as R and *INR* increase, the CA-CFAR loss increases.

PROCESSOR IMPLEMENTATION USING FPGA

The CA-CFAR processor implemented using FPGA/Xilinx integrated chip (Xc9600). The final implementation scheme is consist of the following sub-circuits:

- Storage circuit.
- Sixteen 8-bit shift registers.
- An 8- bit data register (CUT).
- Two accumulator circuits.
- Eight 8- bit adders.
- A multiplier circuit.
- An 8-bit comparator.

Implementation results: A computer simulation program is built to evaluate the performance of the CA-CFAR processor under different values of samples input data using FPGA. Rayleigh distributed clutter is used for testing CA-CFAR under the clear, clutter edge and multiple target environments in different cells. The simulation results are shown in Fig. 6a,b,c for M = 16, α = 1.5 and P_{fa} = 10^{-6}.

The simulation parameters of the time signal used are; time period of T=350 ìsec and pulse width of τ =2µsec. In Fig. 6a, the target at cells location (3) with value of (150) appears in the second time period. Then the response of the processor which makes the decision after 8- reference cells is equal to one because the CUT value is larger than adaptive threshold value.

From Fig. 6b the clutter edge at cells location (2, 3, 4, 5) with values of (121, 105, 95, 120) appear (the first

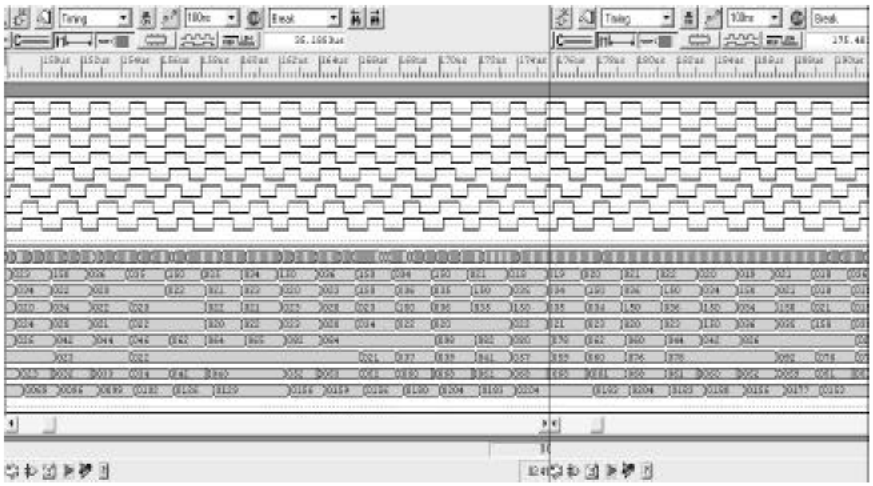

Fig. 6c: The simulation results of the (CA-CFAR) processor for clutter target

and forth) in second time period. In this case the decision is equal to one because the adaptive threshold value from the leading and lagging windows is smaller than CUT value.

While from Fig. 6c the multiple target seen in the cells (2, 5, 8, 10, 12) with the value of (150) dose not appear in the second period. The response of the processor is equal to zero because the CUT value is smaller than adaptive threshold value.

CONCLUSION

CFAR will not estimate the clutter mean level exactly a s it only uses a finite data sample. In all cases, the shorter length (M) gives higher loss. The threshold multiplier amplitude (α) values increase as the number of cells (M) decreases. The interference reduces the detection performance for all CA-CFAR, the CA-CFAR loss increases as the number of interfering targets and the interference-to-noise ratio increase. The CA-CFAR processor operates under clear environment only with small loss but it is not efficient in non-homogenous (clutter edge). The larger values of threshold multiplier amplitude (α), the larger loss can occur.

FPGA technology presents an excellent tool for modern digital circuits design. This technology has provided simple implementation and high reliability. It is so flexible that its library can be extended to include new circuits by using the available options.

REFERENCES

Barkat, M., 2005. Signal Detection and Estimation, Artech House.

Gandhi, P.P. and S.A. Kassam, 1988. Analysis of CFAR Processor in Non-Homogeneous Background. IEEE. Trans. AES., 24: 427- 445.

Nadav, L., 1988. Radar Principles, John Wiley and Sons.

Skolnik, M.I., 2001. Introduction to Radar System, McGraw-Hill Book Company.

Weiss, M., 1982. Analysis of Some Modified Cell-Averaging CFAR Processors in Multiple-Target Situations, IEEE. Trans. AES., 18: 102-113.