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Memory Design Considerations for DDR-3 SDRAM

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Abstract: The emerging DDR3 SDRAM (Double Data Rate 3 Synchronous Dynamic Random Access Memory) standard will extend the performance range of DDR memories considerably, while maintaining some amount of backward compatibility with the existing DDR2 memory standard. The design of DDR-3 was done using Verilog HDL. The new features in DDR3 build on the DDR2 SDRAM add logical improvements to increase system bandwidth (up to 1.6GB s^{-1}) and increases performance at low power. Furthermore, the supply voltage for the memory is reduced from 1.8 V for DDR2 to just 1.5 V for DDR3 targeting a workday equivalent of battery time. DDR3 has additional features which include a master reset pin, an 8-bit pre-fetch and ZQ calibration in order to improve performance and reliability. This study will provide the reader with a detailed understanding of the key design considerations for DDR3 SDRAM system.

Key words: DDR-3, flyby topology, leveling, ODT, ZQ calibration, memory design

INTRODUCTION

Memory speed is a crucial component of system performance. Currently, the most common form of memory used Is Synchronous Dynamic Random Access Memory (SDRAM). DDR SDRAM is an evolutionary extension of "single-data-rate" SDRAM and provides the benefits of higher speed, reduced power and higher density components. In order to achieve the 1.6GB s^{-1} bandwidth target, DDR3 uses a prefetch of 8 words versus DDR2's 4 word prefetch. Thus, for every read or write operation, a total of 8 words are accessed in the core of the DRAM to keep up with the data rate at the pins. Data is clocked into or out of the device on both the rising and falling edges of the clock. With data being transferred 8 bytes at a time DDR RAM gives a transfer rate of (memory bus clock rate)×2 (for dual rate)×8 (number of bytes transferred). Thus with a bus frequency of 100 MHz, DDR 3-SDRAM gives a max transfer rate of 1600 MB/s (2006).

An asynchronous RESET pin guarantees the state machine inside the chip can be reset to a known state after power-up. DDR3 memory modules adopted a "fly by topology" for the addresses, command and clock signals. DDR3 includes a ZQ pin that is connected to an external precision resistor that is used to precisely adjust the "on" impedance of the output drivers and the On Die Termination (ODT) impedances. DDR3 SDRAMs have two self refresh modes that scale the refresh rate according to temperature. The dramatic growth in consumer electronics has generated an increasing need for economical off-chip data storage (Graham, 2006). From EDO RAM to SDRAM to DDR-2, there is no looking back for legacy memory technologies as the DDR3 will arrive well before the masses could experience the current DDR2. In this study, the important features in the DDR-3 SDRAM design will be discussed.

FUNCTIONAL DESCRIPTION

Basic functionality: The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location.

Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 selects the row. The address bits registered coincident with the

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Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued and select BC4 or BL8 mode 'on the fly' if enabled in the mode register (Table 1) (DDR_3 SDRAM, 2006).

Table 1: Abbreviation definitions

Abbreviation	Function
CKE	Clock Enable
CK,CK#	Differential clock inputs
CS#	Chip select
DM	Input data mask
BA0-BA2	Bank address inputs
A0-A15	Address inputs
A10 / AP	Auto precharge
A12 / BC#	Burst chop
DQ	Data input
DQS	Data strobe

Simplified state diagram: A new reset pin is used to clear all state information in the DDR3 memory device without the need to individually reset each control register or power down the device. This saves time and power when bringing the device to a known state. Various functions, features and modes are programmable in four Mode Registers as user defined variables and must be programmed via a Mode Register Set (MRS) command. 'Idle state' is defined as all banks are closed, no data bursts are in progress, CKE is high and all timings from previous operations are satisfied as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied. The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks.

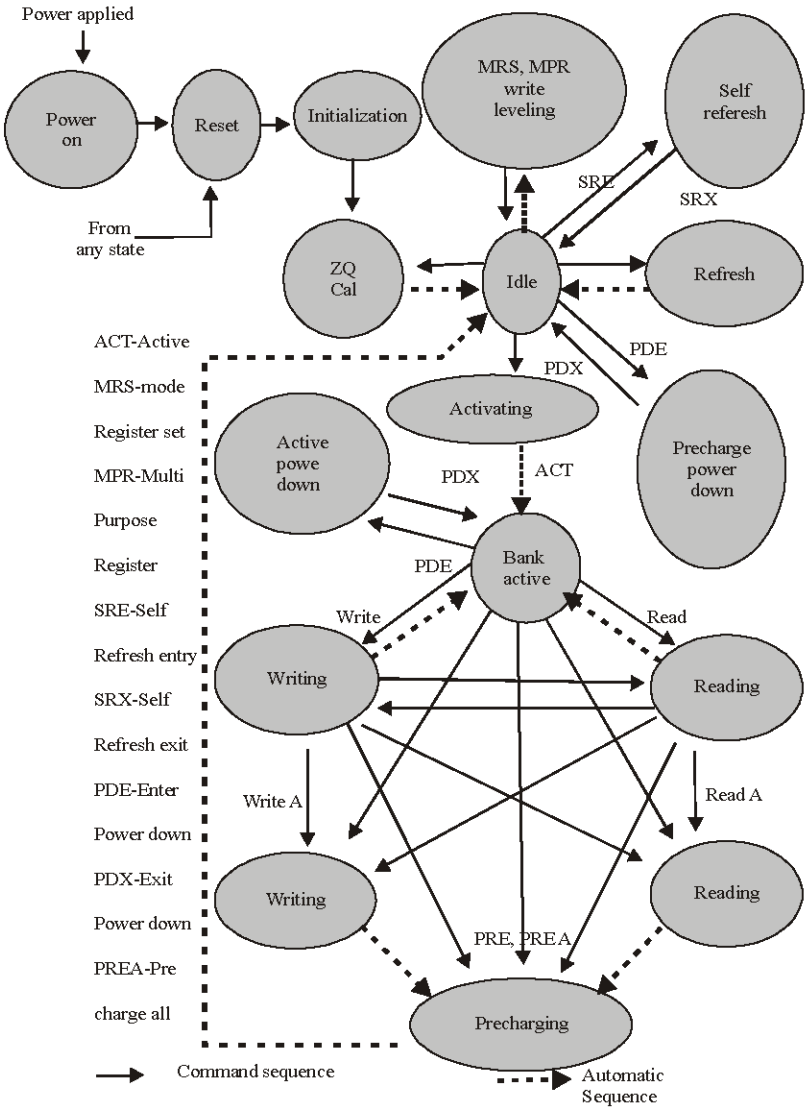

Fig. 1: Simplified state diagram

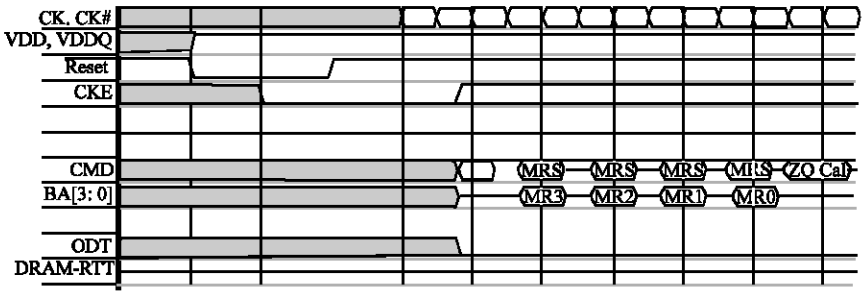

Fig. 2: Reset and initialization sequence

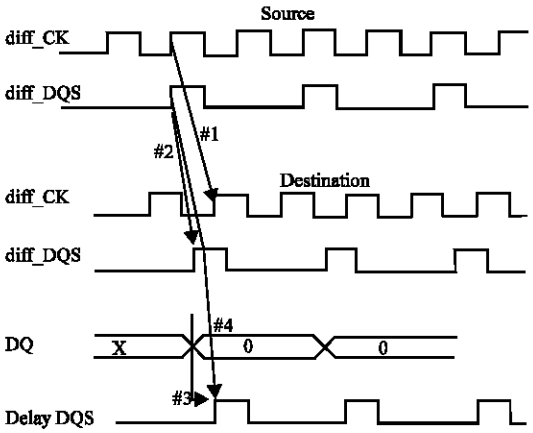

Fig. 3: Timing diagram for write leveling

a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank (DDR$_3$ and SDRAM, 2006).

This simplified state diagram is intended to provide an overview of the possible state transitions and the commands to control them (Fig. 1 and 2).

Write leveling: DDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. During write leveling, the memory controller needs to compensate for the additional flight time skew delay introduced by the fly-by topology with respect to strobe and clock. The source CK and DQS signals are delayed in getting to the destination as illustrated by arrow #1 and arrow #2, respectively. The memory controller repeatedly delays DQS, a step at a time, until a transition from a zero to a one is detected on the destination CK signal (Fig. 3). This will re-align DQS and CL so that the destination data on the DQ bus can be captured reliably (Raj, 2007).

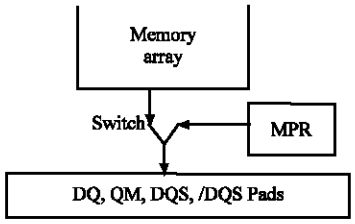

Fig. 4: Read leveling using MPR

Read leveling: During read leveling, the memory controller adjusts for the delays introduced by the fly-by memory topology that impact the read cycle. This is done via the addition of a special Multi-Purpose Register (MPR) in the DDR3 memory device. The MPR can be loaded with redefined data values via a special command from the memory controller. These data values can be used for system timing calibration by the memory controller. As shown in Fig. 4, the MPR can be selected, by setting a bit in another memory register (EMRS3, bit A2), to switch the source of data for memory read to come from the MPR, not the normal memory array. The MPR data is substituted for the DQ, DM, DQS and /DQS pads on the memory device. This feature allows the memory controller to calibrate the timing of the read path to adjust for any additional delays introduced by the DDR3 fly-by architecture. The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence (Raj, 2007).

Read/write operation: The Read/write command is used to initiate a burst read/write access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank and the address inputs select the starting column location. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. During a Read or Write command (Fig. 5 and 6), DDR3 will support BC4

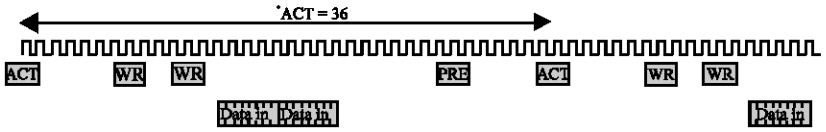

Fig. 5: Write operation

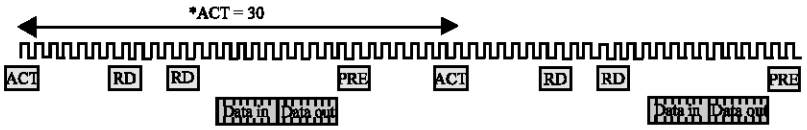

Fig. 6: Read operation

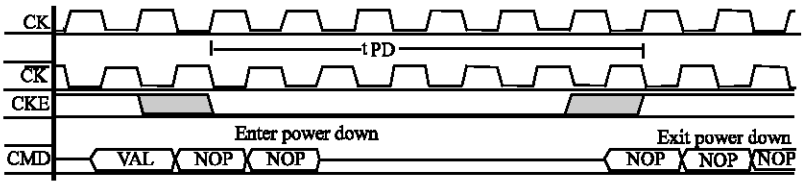

Fig. 7: Active power-down entry and exit timing diagram

and Burst Length BL8 on the fly using address A12. A row is opened with an ACT command and then a set of two BL = 8 Reads is completed from columns in that row. After the Reads are complete, the row is closed with a PRE command and the sequence is restarted (DDR_3 SDRAM, 2006).

POWER DOWN MODES

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operation are in progress (Fig. 7).

CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress. During power-down, if all banks are closed after any in progress commands are completed, the device will be in precharge power-down mode; if any bank is open after in progress commands are completed, the device will be in active power-down mode.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE and Reset#. Multiple NOP or Deselect commands are needed during the CKE switch off in order to protect DRAM internal delay on CKE line to block the input signals. All existing Power Down "entry to exit" timing diagrams using tCKE will be updated to tPD (power down time). The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). CKE high must be maintained until tCKE has been satisfied (DDR_3 SDRAM, 2006).

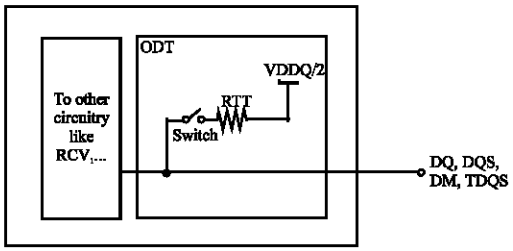

Fig. 8 : Functional representation of ODT

On-die termination: ODT (On-Die Termination) is a feature that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS# and DM. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance as shown in Fig. 8.

In order to preserve signal strength on the active bank, it is best to add a switch to turn off ODT simultaneously with enabling chip select. There is no possibility for the reflections to reenter the bus and contaminate the real signals. Dynamic ODT function that permits the termination impedance of the DDR3 SDRAM to be varied between two preset values on-the-fly without issuing a mode register set command (DDR_3 SDRAM, 2006).

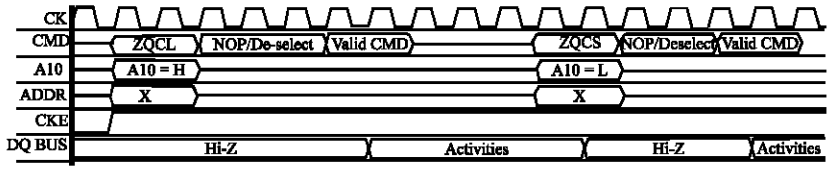

Fig. 9: ZQ calibration timing

ZQ calibration: The new ZQ calibration feature allows the memory device to take a longer time for calibration at start-up and a smaller time during periodic calibration activities (Fig. 9). ZQ Calibration command is used to calibrate DRAM Ron and ODT values. DDR3 SDRAM needs longer time to calibrate Ron and ODT at initialization and relatively smaller time to perform periodic calibrations (DDR_3 SDRAM, 2006).

Self refresh: DDR3 SDRAMs have two self refresh modes that scale the refresh rate according to temperature. If in case temperature of the DDR3 SDRAM is below 85° Celsius, the chip can use a 7.8us refresh interval. However, if the DDR3 SDRAM is between 85° C and 95° C, the chip must use a nominal 3.9us refresh interval which is also the only rate available with DDR2 SDRAMs that operate up to 95°C. Since the DDR3 SDRAM will likely cool off in self refresh mode, the ability to slow down the refresh rate and conserve almost one half the power, is a huge bonus to standby power sensitive applications (Graham, 2006).

RESULTS AND DISCUSSION

DDR3 delivers extremely high bandwidth with data rates up to 1.6GB s^{-1}, twice the bandwidth of DDR2. 8 banks (DDR3) have 4 more open banks for back to back access compared to 4 banks (DDR2) (Fig. 10).

Component per pin: 800-1,600 MT/s

Bus bandwidth: 6,400-12,800 MT/s

The supply voltage is reduced from 1.8V to1.5V. i.e., ~30% reduction in power due to supply voltage alone. For example, the graph shows that an 800MHz DDR3 consumes approximately 30% less power than an equivalent DDR2 module when both perform the same task (Fig. 11).

DDR3 modules offers better signal control than DDR2 resulting from DQ shielding, self ODT and a fly-by command/address/control bus. DDR3 is the memory solution of choice for next generation in high-performance CPU systems. DDR3 SDRAM can transfer data at a maximum of 25.6 GB s^{-1} on a desktop PC. Table 2 shows a feature by feature comparison of DDR2 and DDR3 memory devices.

Table 2: DDR2 and DDR3 feature comparison

Parameters	DDR2	DDR3
Data rate	400-800Mbps	800-1600Mbps
Voltage	1.8 V	1.5 V
Reset	No	Yes
Termination	On die	On die (enhanced)
Driver calibration	Off-chip	On-chip with ZQ pin
Leveling	No	Yes

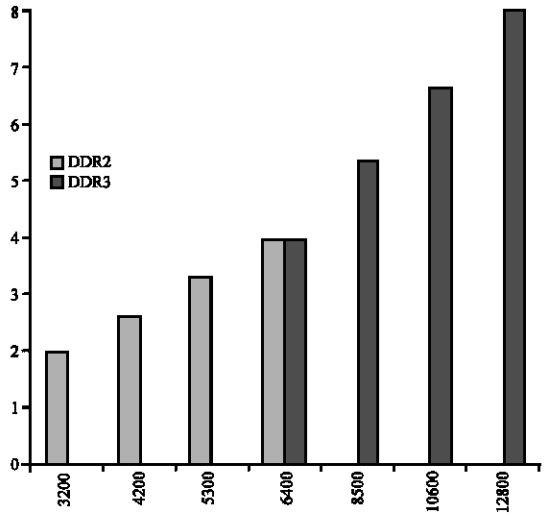

Fig. 10: Comparison of bandwidth

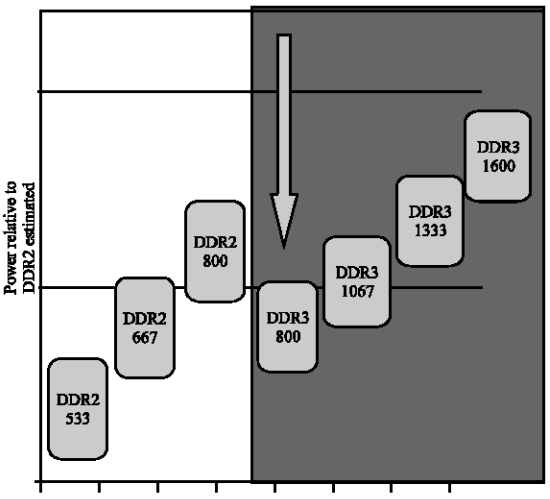

Fig. 11: Power consumption

CONCLUSION

DDR3s main thrust is to increase bandwidth results in substantial performance improvement over previous DDR2 memory systems. DDR3's increased performance coupled with lower power requirements benefits desktop PCs, notebooks and servers. For main memory, DDR3 is expected to become the memory of choice to accompany the dual-and multi-core processors. Thus, the new features in DDR3 build add logical improvements to increase system bandwidth (up to 1.6GB s^{-1}) and increase in performance at low power.

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