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Reconfigurable Multiprocessor System Reliability Estimation

Oleg Viktorov
Department Software Engineering, Al-Zaytoonah University,
P.O. Box 1764, Amman, Jordan

Abstract: Reconfigurable multiprocessor systems offer an approach for improvement of system reliability. On the one hand the faults do not cause the whole system down because of the redundancy of such systems and suitable reconfiguration actions. From the other hand, higher system performance means more processors and other modules, which may result in more faults and a higher risk that system fails. Since classical reliability evaluation technique is not applicable to reconfigurable multiprocessor systems, another approach to reliability evaluation is presented. The result shows that the systems with multibus interconnection are the most reliable among all reconfigurable multiprocessor systems with bus oriented interconnection unit.

Key words: Reconfigurable multiprocessor systems, redundancy, single bus interconnection, multiple bus interconnection, multiport memory unit, cross-bar interconnection unit

INTRODUCTION

One of the most widely used way to increase system performance is a parallelism that is usually achieved by means of multiprocessing. However, this hardware overhead can be used also to increase system reliability. Conventional multiprocessor system consists of n processors P_1, P_2, . . . , P_n, m memory units M_1, M_2, . . . , M_m and interconnection unit. When a fault occurs system recovery should be done through reconfiguration of interconnection unit that consists of k switching elements S_1, S_2, . . . , S_k .. More then 10 interconnection unit structures are known (Selvaraj and Jozwiak, 2005; Ku and Hayes, 1997; Mahapatra and Dutt, 2001; Singh and Youn, 1991), but the investigations of system structures presented here is restricted to the following systems with bus oriented interconnection units:

- Common bus reconfigurable multiprocessor systems;
- Multibus reconfigurable multiprocessor systems;
- Multiport reconfigurable multiprocessor systems;
- Cross-bar reconfigurable multiprocessor systems.

Well-known formulas can be used for conventional multiprocessor system probability estimation (Kales, 1998). It seems that reconfigurable multiprocessor system reliability can be improved because their natural redundancy is used to increase reliability (Yu and Koren, 1994). So reconfigurable multiprocessor system reliability estimation is a new task and it needs some new approaches that have been presented in this study.

REALIABILITY ESTIMATION APPROACH

A reconfigurable multiprocessor system has maximum configuration, if all n processors, m memory units, b interconnection buses and k switches are in full working order.

A reconfigurable multiprocessor system has minimum configuration, if a system has v nonfaulty units and single unit failure causes system down.

This reconfigurable multiprocessor systems reliability estimation approach uses D-the number of system configurations, in witch system is out of order.

$$D = (n-v+1)(n-v+1)/2$$

Common bus reconfigurable multiprocessor systems reliability can be defines by the following formula:

$$R(t) = 1-\prod_{p=1}^{D} Q_p(t),$$

Where $Q_P(t)$-of the failure probability of the system in configuration p.

RESULTS

Common bus reconfigurable multiprocessor systems и its graphical representation are shown in Fig.1 a and b. Common bus reconfigurable multiprocessor system reliability is:

$$Rcb(t) = 1-\prod_{i=a}^{n}\prod_{j=b}^{m}\prod_{l=d}^{n}(1-R_P^i(t)R_m^j(t)R_B(t)R_S^l(t)), \quad (1)$$

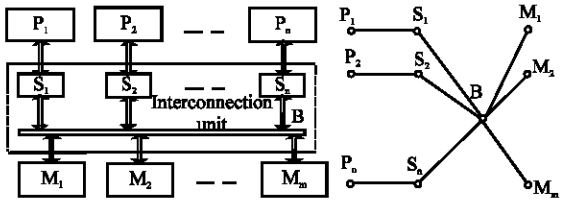

Fig. 1: Reconfigurable multiprocessor system with commen bus

Where

- $R_p^i(t)$ is the probability that i-th processor performs the given function;
- $R_i^i(t)$ is the probability that j-th memory unit performs the given function;
- $R_B(t)$ is the probability that common bus provides the proper connection;
- $R_S^l(t)$ is the probability that l-th switching element performs the given function.

Multibus reconfigurable multiprocessor systems and its graphical representation are shown in Fig. 2a and b.

Multibus reconfigurable multiprocessor system reliability is:

$$R_{MB}(t) = 1-\prod_{i=a}^{n}\prod_{j=b}^{m}\prod_{k=c}^{m}\prod_{l=d}^{m}, \quad (1-R_P^i(t)R_m^j(t)R_B^k(t)R_S^l(t)) \tag{2}$$

Where

- $R_P^i(t)$ is the probability that i-th processor performs the given function;
- $R_i^i(t)$ is the probability that j-th memory unit performs the given function;
- $R_B^k(t)$ is the probability that k-th common bus provides the proper connection;
- $R_S^l(t)$ is the probability that l-th switching element performs the given function.

Multiport reconfigurable multiprocessor systems and its graphical representation are shown in Fig.3 a and b.

Multiport reconfigurable multiprocessor system reliability is:

$$R_{MPM}(t) = 1-\prod_{l=c}^{n}\prod_{k=d}^{n}\prod_{k=c}^{m}\prod_{l=d}^{m} \quad (1-R_P^i(t)R_m^j(t)R_B^k(t)R_M(t)) \tag{3}$$

Where

- $R_p^i(t)$ is the probability that i-th processor performs the given function;
- $R_B(t)$ is the probability that k-th common bus provides the proper connection;

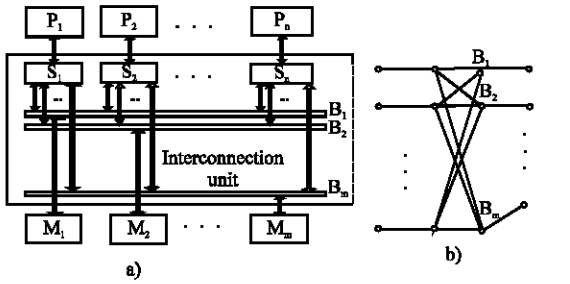

Fig. 2: Reconfigurable multiprocessor system with multiple buses

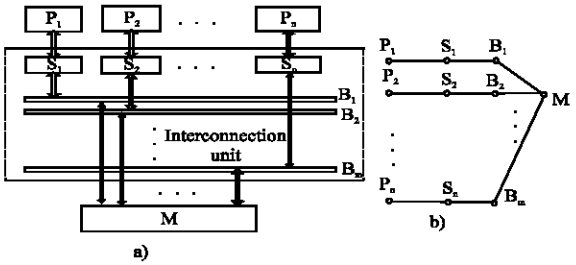

Fig. 3: Reconfigurable multiprocessor system with multiple memory

- $R_S^l(t)$ is the probability that l-th switching element performs the given function.
- $R_M(t)$ is the probability that multiport memory unit M performs the given function;

Cross-bar reconfigurable multiprocessor systems and its graphical representation are shown in Fig. 4 a and b.

Multibus reconfigurable multiprocessor system reliability is:

$$R_{cbs}(t) = 1-\prod_{l=c}^{n}\prod_{j=b}^{m}\prod_{k=c}^{m}\prod_{l=d}^{ixj} \quad (1-R_v R_P^i(t)R_m^j(t)R_B^k(t)R_S^l(t)) \tag{4}$$

Where

- $R_P^i(t)$ is the probability that i-th processor performs the given function;
- $R_i^i(t)$ is the probability that j-th memory unit performs the given function;
- $R_B^k(t)$ is the probability that k-th common bus provides the proper connection;
- $R_S^l(t)$ is the probability that l-th switching element performs the given function.

R_v is the probability that a multiprocessor system with v non faulty units performs assigned functions:

$$Rv = \sum_U \sum_W G/C_{i\,x\,j}^{\max(i,j)}$$

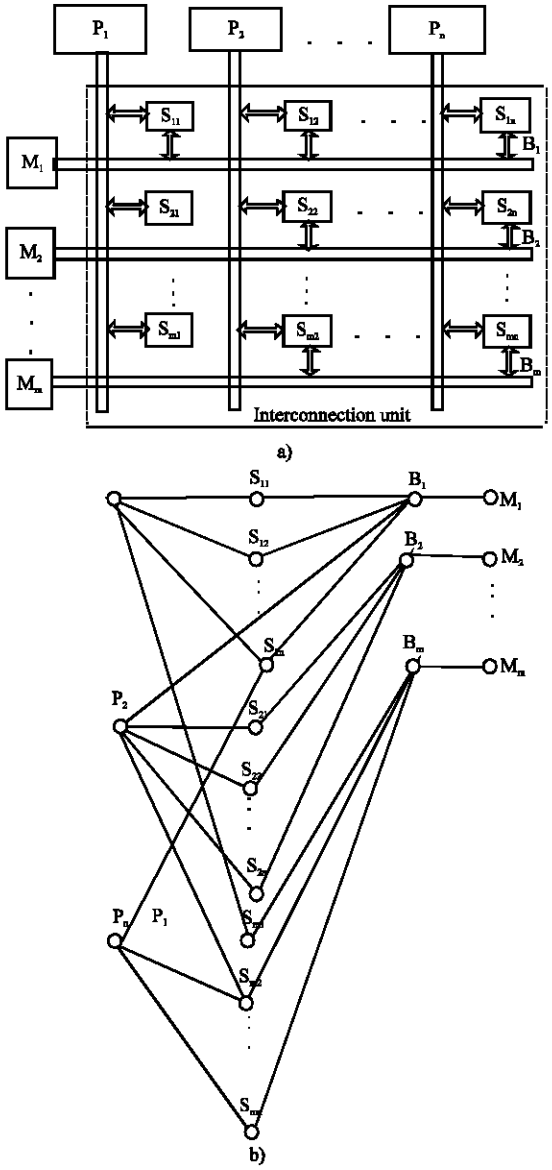

Fig. 4: Reconfigurable cross-bar switch multiprocessor system

U is the set of partitions of max(i,j) on k addends;
W is the set of matrices, which have no empty rows;
G-the number of column arrangements for each matrices from the set W;
$C_{i\,x\,j}^{\max(i,j)}$-the number of max(i,j)-subsets of i x j element set.

CONCLUSION

Analysis of the expressions (1)-(4) and graphical representations (Fig. 1b-4b) shows that multibus reconfigurable multiprocessor system has the highest system reliability, because maximum and minimum configurations of common bus reconfigurable multiprocessor systems (multiport reconfigurable multiprocessor systems) are the same (Fig 1b-3b). The complexity of cross-bar reconfigurable multiprocessor systems grows gradually ($0(N^2)$) with number of processors and memory units, that definitely badly affects the system reliability.

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