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Design and Implementation of Reduced Area Reed Solomon Encoder using Quantum Dot Cellular Automata

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Abstract: Reed Solomon (RS) codes are one of the most extensively used error correcting codes in contemporary digital communication broadcast systems. The area and complexity are the major issues in digital circuit design. This study proposes an implementation of Reed Solomon encoder circuit with reduced area using nanotechnology based Quantum dot Cellular Automata. Here, researchers uses a reduced cell EX-OR gate to perform all computation of Reed Solomon encoder circuit. The Reed Solomon encoder circuit has been synthesized using QCA designer tool. The available conventional Reed Solomon encoder circuit occupies larger area but because of the nano scale technology the area and complexity of the proposed Reed Solomon encoder circuit is reduced considerably. The proposed design needs only about 86% of the hardware compared to previous design with same clocking performance.

Key words: Reed Solomon encoder, Ex-OR gate, majority gate, QCA designer, scale

INTRODUCTION

Error control codes are widely used in present digital communication systems to protect the transmitted data from channel errors (Wang, 2001). Normally the error control codes are classified into convolutional codes and block codes (Berlekamp *et al*., 1987). Reed Solomon (RS) codes are linear block codes and belong to the class of non-binary Bose Chaudhuri Hocquenheim (BCH) codes. Reed Solomon (RS) codes achieve the largest possible code minimum distance for any linear code with the same encoder input and output block lengths. For non binary cyclic codes the distance between two codeword is defined as the number of symbols in which the sequence differs. Reed Solomon coding scheme was introduced by Reed and Solomon (1960) Wicker and Bhargava (1999). Reed Solomon code can correct all random and burst errors and this coding scheme has being exploited in many applications such as satellite communication, compact disc players, broadband, wireless communications, digital television, wireless sensor networks, etc. (Ong *et al*., 2011).

Nano technology based Quantum dot Cellular Automata (QCA) cell produce a new way to digital systems (Lent *et al*., 1993; Kohavi, 2007; Baker *et al*., 2004; Amlani *et al*., 1999). QCA is a computational methodology as an alternate to Field Effect Transistor (FET) (Lieberman *et al*., 2002; Bhattacharjee, 2008) devices. It is developed at the ATIPS Laboratory at the University of Calgary, QCA designer currently supports three different simulation engines and many of the CAD features required for complex circuit design (Walus *et al*., 2004a-c). In order to represent binary information logic 1 and logic 0 the cell polarization P = +1 and P = -1 is used, respectively (Walus *et al*., 2003; Wei *et al*., 2003). QCA cell polarization is shown in Fig. 1.

QCA inverters that use 45° and 90° cells orientations have been developed (Lakshmi and Athisha, 2010). The QCA majority gate produces an output that reflects the majority of the inputs. The QCA majority gate has four terminal cells out of which three are representing input terminal cells and the remaining one represents the output cell. Let us assuming the three inputs are X, Y and Z, the logic function of the majority gate is:

$$M(X, Y, Z) = XY + YZ + ZX \quad (1)$$

To construct well efficient QCA design, the digital circuits are implemented with the help of majority

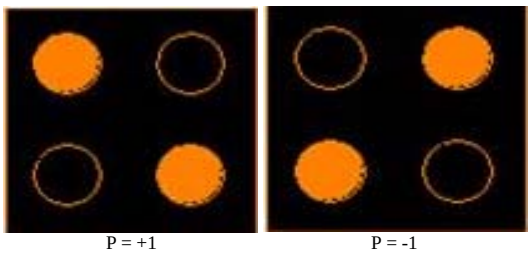

Fig. 1: QCA cell polarization

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gate-based design techniques are needed. The another type of majority gate consist of six terminals out of which five are representing input terminal cells and the remaining one represents the output cell (Navi *et al*., 2010).

FINITE FIELDS

In order to understand the encoding principles of Reed Solomon codes, it is necessary to venture into the area of finite fields commonly known as Galois Fields (GF). For any prime number p there exists a finite field denoted GF(p) containing p elements. To obtain the finite set of elements of $GF(2^m)$ from F, a condition must be implemented on F so that it may contain only 2^m elements and is closed under multiplication. The elements of finite fields are given by:

$$GF(2^m) = \left\{0, \alpha^0, \alpha^1, ..., \alpha^{2m-2}\right\} \quad (2)$$

The Galois Fields (GF) addition and multiplication is the important elements of encoder circuit. These addition and multiplication of the finite field elements is implemented with the help of binary Exclusive OR gate. The necessary Exclusive OR operations to compute the check sum corresponding to each message symbol is compared with the binary case which used the same generator polynomial. The realization of Exclusive OR gate is done making use of Majority Gates (MGs) and following the equations as follows:

$$A \oplus B = AB' + A'B \quad (3)$$

The Exclusive OR is designed with 3 majority gates and 2 invertors. The corresponding QCA implementation is shown in Fig. 2. It is implemented with 64 QCA cells with an area of 65756 nm^2.

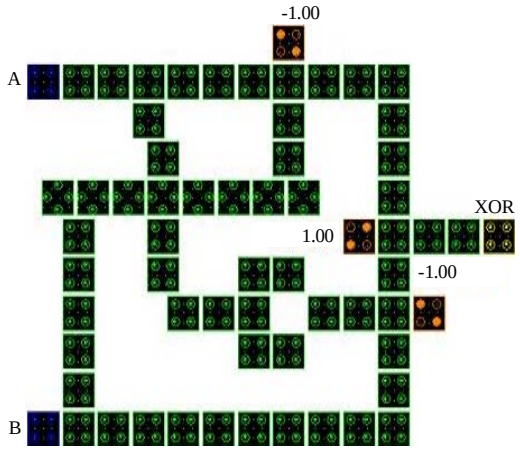

Fig. 2: QCA implementation of Exclusive OR gate

REED SOLOMON ENCODER STRUCTURE

The most conservative RS(n, k) code is written as follows:

$$(n,k) = (2m-1, 2^m - 1 - 2t) \quad (4)$$

Where:

n-k = 2t = The number of parity symbols
t = The symbol error correcting capability of the code

The generating polynomial for an RS code can be written as:

$$G(X) = g_0 + g_1X + ... + X2t \quad (5)$$

The degree of the generator polynomial is equal to the number of additional parity symbols. Since, RS codes are cyclic codes, encoding is systematic form is corresponding to the binary encoding procedure. The shifting of a message polynomial m(X) into the right most k stages of a codeword register and then appending a parity polynomial p(X) by placing it in the leftmost n-k stages. The resulting codeword polynomial can be written as:

$$U(X) = p(X) + X^{n-k}m(X) \quad (6)$$

The linear feedback shift register encoder for (7, 3) Reed Solomon code is shown in Fig. 3. Here, RS non zero code words are made up of 7 symbols and each symbol is made up of 3 bits. This RS encoder circuit required the number of stages in the shift register is n-k. In case of binary encoder, it uses the values of only 1 or 0 but in RS encoder each coefficient is specified by 3 bits, it can uses one of eight values. Here, the total number of clock cycles is equal to n and the values of output register are the codeword polynomial. The codeword polynomial contains the parity symbol and also the message symbols in the form of polynomial.

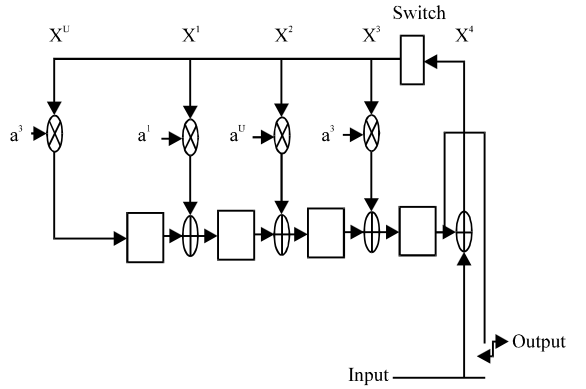

Fig. 3: Linera feedback shift register encoder for a (7, 3) RS code

QCA implementation: QCA computation proceeds by orientation of cells based on polarization of neighboring cells. The QCA inverter is built by neighboring QCA cells on the diagonal which causes Coulomb forces to place the two electrons in opposing wells of the cell compared to the source.

The Reed Solomon encoder circuit is designed with 24 majority gates and 16 inverters and 4 storage elements. The corresponding QCA implementation is shown in Fig. 4. In the implementation the total number of cells required is 1084 cells. This is much lesser than the previous conventional Reed Solomon encoder circuits. Similarly, all the computation of the encoder circuit is done with the help of Exclusive OR gate.

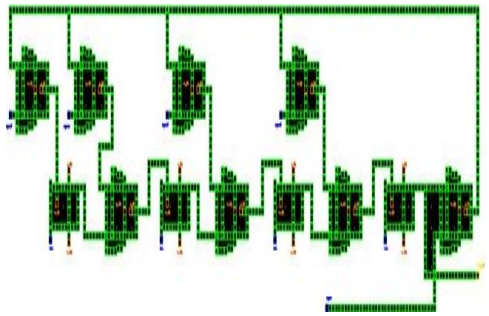

Fig. 4: QCA implementation of Reed Solomon encoder

SIMULATION RESULTS

The proposed Reed Solomon encoder circuit are designed and simulated by using QCA designer tool Ver.2.0.3 for (7, 3) code. The design and simulation procedure is as follows. First, researchers generate the layout of the Exclusive OR gate. Then, researchers design a Reed Solomon encoder using the Exclusive OR gate. The simulated waveforms of Exclusive OR gate and Reed Solomon encoder circuit are shown in Fig. 5 and 6. To maintain reliability with size measurements in previous publication (Lakshmi and Athisha, 2010), researchers assume that the QCA cells are prepared by 2 nm quantum dots. The cells are divided by 0 nm. Thus, the area of the proposed Reed Solomon Encoder is 3131.52×758 nm.

Table 1 lists the area, speed and clocking of the proposed Reed Solomon encoder along with those of the existing one (Lakshmi and Athisha, 2010). It is seen from Table 1 that the projected design requires only

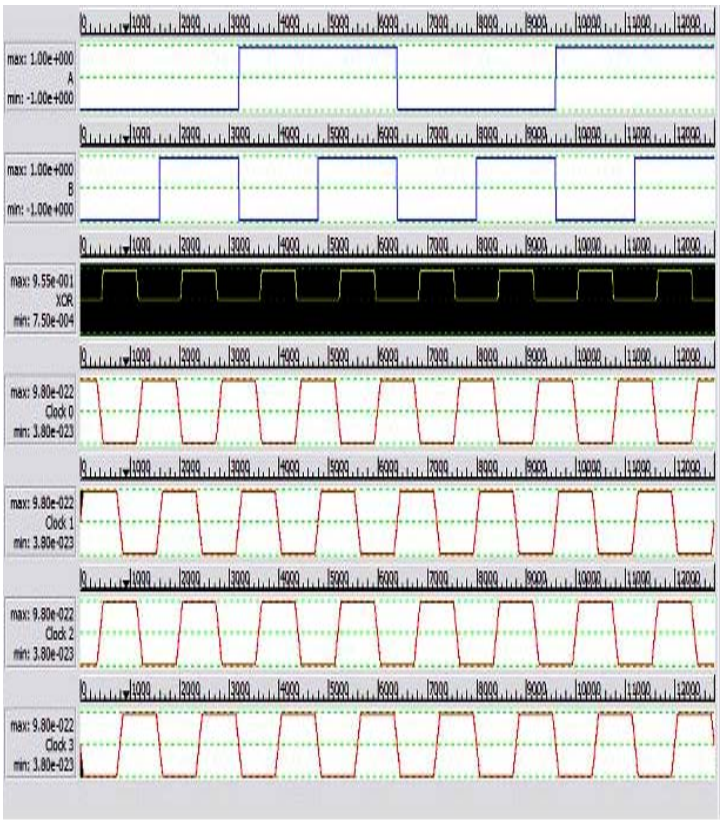

Fig. 5: Simulation result of Exclusive OR gate

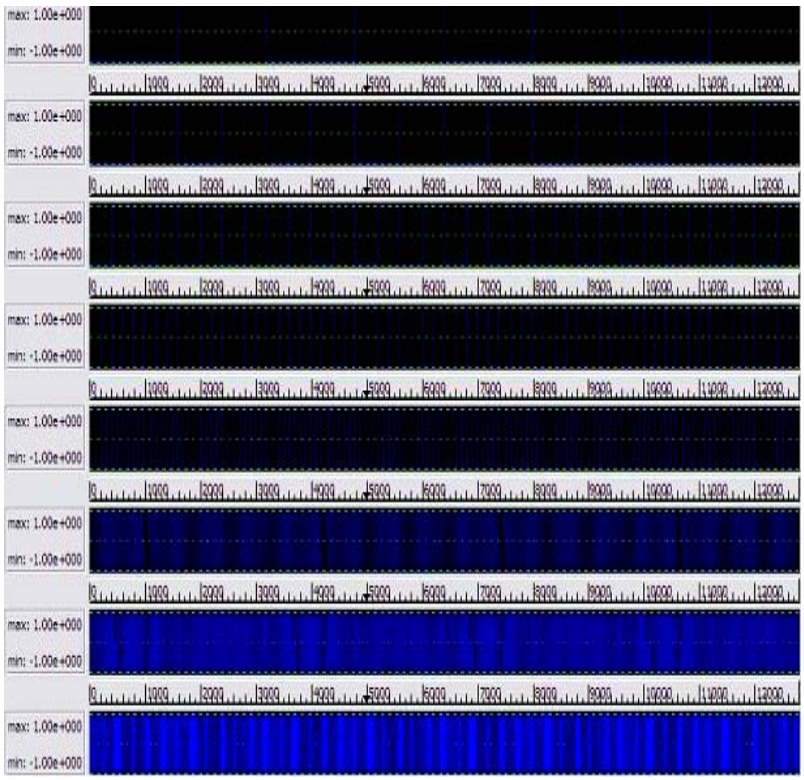

Fig. 6: Simulation result of Reed Solomon encoder

Table 1: Simulation result of QCA Reed Solomon encoder

QCA layout	Area (mm)	Speed	Clocking
Proposed EX-OR	234.04×224.37	Same	Same
Previous EX-OR	290×2260	Same	Same
Proposed Reed Solomon encoder	3131.52×758	Same	Same

about 86% of the hardware compared to the accessible one with the same speed and clocking performance.

CONCLUSION

The proposed design of Exclusive OR gate and Reed Solomon encoder circuit is presented in this study. These combinational logic gate and Reed Solomon encoder circuit have been considered and tested using QCA designer software. The role of the Exclusive OR gate has been confirmed according to the function table. The proposed layouts of Reed Solomon circuit are extensively lesser than the circuits using CMOS equipment and it reduces the area as well as complication required for the circuit than the preceding QCA circuits. The considered QCA based Reed Solomon encoder circuit can be used to hold each shift register with three bits. In future, this can be extended to hold each shift register with eight bits.

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