Asian Journal of Information Technology 15 (7): 1183-1192, 2016
ISSN: 1682-3915

MATLAB Based Simulation and Design of Multilevel PV Inverter for a Three Phase Grid Connected System

N. Balasubramaniam and Devishree Jayabal
Department of Electrical and Electronics Engineering,
Coimbatore Institute of Technology, Coimbatore, India

Abstract: This study proposed a novel design of Multilevel PV Inverter for Grid Connected System which is named as Center-tapped primary winding transformer based five level inverter (C-T^2 Inverter). The design of C-T^2 Inverter is aimed to reduce the number of components is directly proportional to reduction in the power losses, size and cost. The proposed three phase inverter is driving only by the Single dc supply that is each phase is parallel connected to the same dc input source. Finally, the grid synchronization is made by using Space Vector Pulse Width Modulation (SVPWM) which enhances the power quality indices like Power Factor (PF) and Total Harmonic Distortion (THD).

Keywords: Multilevel Inverter, grid synchronization, Space Vector Pulse Width Modulation (SVPWM), Center Tapped Primary Winding Transformer (C-T^2), phase

INTRODUCTION

Owing to the depletion of fossil fuels and the environmental issues has resulted, renewable energy, in particularly solar energy has gained popularity. The demand for Solar-electric-energy has risen in a consistent manner at the rate of 20-5% per annum in the last 20 year (Carrasco *et al*., 2006) and further the growth is mainly in the grid-connected applications. Due to this enormous growth in the market for grid-connected Photovoltaic (PV) systems, there are evolving interests in the grid-connected PV configurations.

During the recent years, power electronics engineers have greatly focused on multilevel inverters in the form of a novel type of power converter. Several multilevel inverters have a structure of switches and capacitor voltage sources. By means of a right control over the switching devices, these can be able to generate stepped output voltages along with low harmonic distortions. These multilevel inverters find extensive employment in manufacturing factories and have secured public faith as one among the new powerconverter fields since they are capable of overcoming the drawbacks of conventional Pulse Width-Modulation (PWM) inverters (Lai and Peng, 1996; Tolbert *et al*., 1999; Rodriguez *et al*., 2002).

Multilevel Inverters (MLI) can be segregated into three significant topologies: diode-clamped (Chen and He, 2006; Cheng *et al*., 2006; Bendre *et al*., 2006), flying capacitors (Krug *et al*., 2007) and cascaded H-bridge cells along with separate dc sources (Marchesoni *et al*., 1988; Watson *et al*., 2007; Lezana *et al*., 2007; Rech and Pinheiro, 2007). By theory, they can generate high-voltage output with voltage levels that is infinite. Typically, low voltage switching elements are series connected, powered by continuous switching signals for synthesizing step waveform having a high voltage. Between them, the diode-clamped MLI requires complicated PWM controls as more number of capacitors and diodes are needed for the generation of output levels and adjustment of the balance of every dc-link voltage of the capacitor (Nabae *et al*., 1981; Meynard and Foch, 1992). During the application of the flying capacitor MLI, the circuit can have comparatively less number of elements but the volume of the system is made as more capacitors are needed. In the cascaded H-bridge-type MLI, every low-voltage H-bridge module contains one independent dc-link voltage source. Its remarkable benefits are the easy controlling, flexibility during application and reliability. Nonetheless, the cascaded H-bridge type MLI has a drawback that the independent dc-link voltage requires to be given by each of the H-bridge separately (Rodriguez *et al*., 2007; Kang *et al*., 2005), in order to minimize the number of independent dc sources substituting reactors (Soto *et al*., 2003) or capacitors (Chiasson *et al*., 2007) in MLI's.

In a cascaded MLI with isolated dc source for the three phase grid connected system presented (Topology 1) is illustrated in Fig. 1. Every dc/ac inverter (H-Bridge) module consists of its own PV panel (isolated) and the PV modules along with their corresponding H-Bridge are still series connected for creating a high ac voltage level. It yields the merits of individual module Maximum Power Point (MPP) Tracking (MPPT); furthermore this cascaded inverter would keep

Corresponding Author: N. Balasubramaniam, Department of Electrical and Electronics Engineering, Coimbatore Institute of Technology, Coimbatore, India

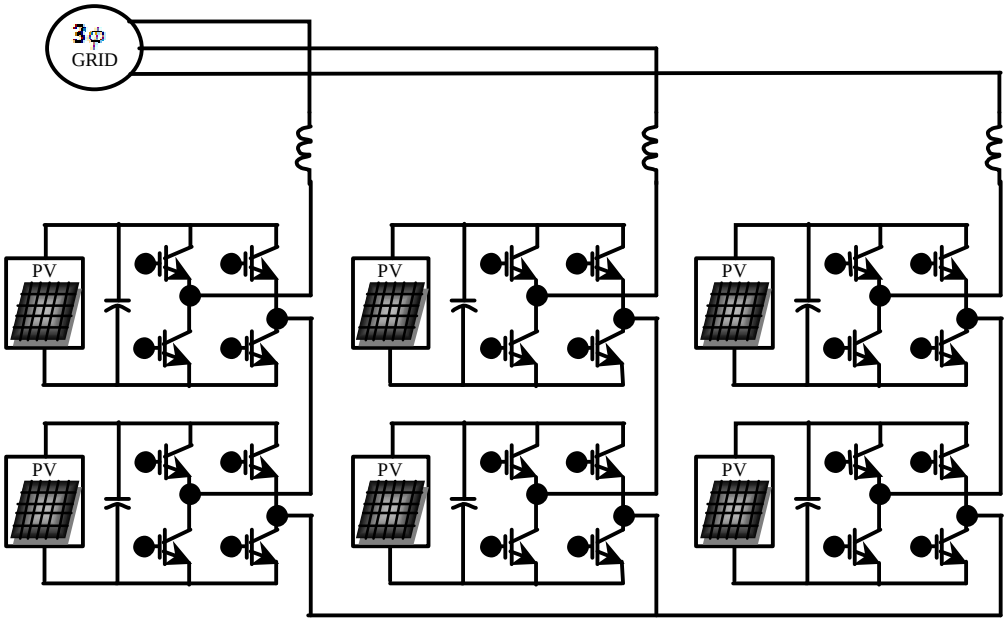

Fig. 1: Conventional 3ϕ cascaded five level inverter with isolated dc supply

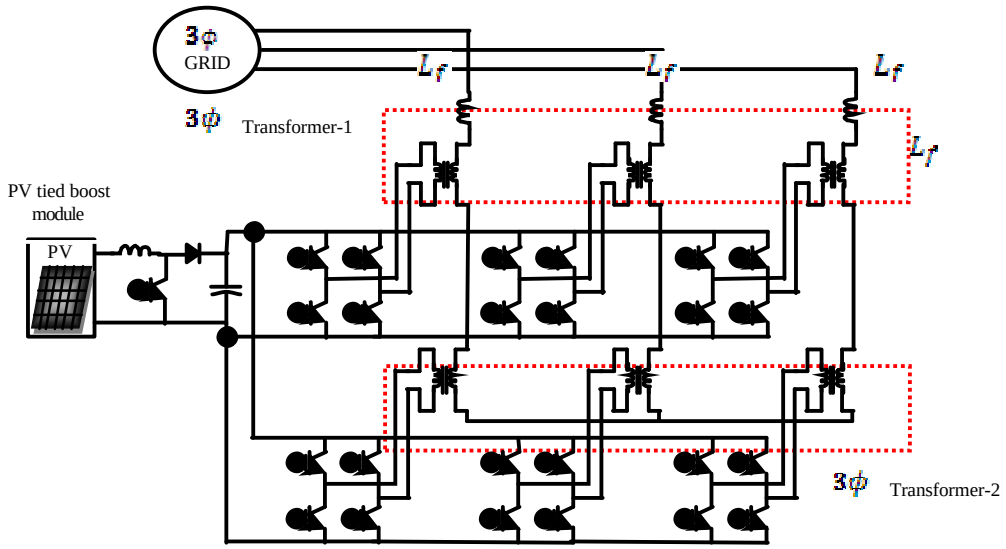

Fig. 2: Conventional 3ϕ cascaded five level inverter with common dc supply using 3ϕ transformer

up with the advantages of "one converter per panel," like better usage per PV module, ability to mix various sources and redundancy of the system. Additionally, this dc/ac cascaded inverter eliminates the necessity for the per-string dc bus and the central dc/ac inverter which also helps in the improvement of the overall performance. As the circuit configuration shown in Topology 1 has fewadvantages, nonetheless, it has a demerit that the independent dc-link voltage is needed to be given separately by H-bridge. Moreover PV mismatch is a critical issue observed in the PV system. Because of the (partial shading) unequally received irradiance, diverse temperatures and aging of the PV panels, the MPP of every PV module might be different. If every PV module is impacted by partial shading, the overall PV system efficiency will be reduced. The isolated converters (PV tied H-Bridge inverter) faces setbacks like taking up huge space, expensive and ineffective owing to its large power utility devices.

There is presented a cascaded MLI having a common dc source using three phase transformer for a three phase grid connected system (Topology 2) which is illustrated in Fig. 2. In this topology, a cascaded H-bridge MLI which utilizes one single dc input power source and two

isolated three-phase low-frequency transformers is used. The H-bridge modules are connected in parallel to the same dc input source and all secondary of the transformers areconnected. In this configuration, the output voltage is a total of the terminal voltages of each of the H-bridge module. The amplitude of the output voltage is decided by the input voltage and the turns ratio of the transformer. Every primary terminal of the transformer is been connected to an H-bridge module such as $+V_{dc}$+V_{dc}/2, zero, -V_{dc}/2, -V_{dc} are synthesized. Each secondary of the transformer is then series connected for piling up the output level. The Topology 2 has few advantages; nonetheless, it has a drawback that more number of three phase transformer results in high power losses, huge space and expensive, thus leading to reduction in power efficiency.

This study discusses about the methods for alleviating the above mentioned traditional issues related to topology and also for further improving the efficiency of the system and therefore a resourceful and cost-economic inverter with the number of current conduction devices reduced (three phase transformers and switching devices) has to be developed.

MATERIALS AND METHODS

The overall schematic diagram of novel center-tapped primary winding transformer (C-T^2) based five level inverter (C-T^2 Inverter) with common dc supply is shown in Fig. 3. It consists of PV tied boost converter in the front end, the 3ϕ C-T^2 Inverter, 3ϕ centre tap transformer; LC filter after which a three phase grid follows. This 3ϕ C-T^2 Inverter configuration further comprises of C-T^2 Inverter-A, C-T^2 Inverter-B and C-T^2 Inverter-C. Every phase C-T^2 Inverter has four switches S_{1-4} in addition with two power diodes D_1 and D_2. Moreover, the input inductor: L_b, diode; D_b, switch; S_b and voltage balancing capacitors; C_{b1} and C_{b2}; boost converter are employed for extracting the maximum power from PV panel making use of MPPT algorithm. Here, the single dc supply is utilized for powering the three phase five level inverter. At last, the harmonics produced by the inverter are filtered by means of the three phase LC filter.The output power obtained from the three phase five level inverter is then fed into the three phase grid as shown in Fig. 3.

The proposed topology has made the following major contributions: single dc supply (PV tied boost converter) which is used for driving the three phase five level inverter substituting the independent dc supply finds its application in topology 1. Because of the single-stage power conversion present between PV and load ports, there is huge improvement in the efficiency of the converter. The design of the three phase five level inverter having the number of components reduced is introduced for reduction in the current conduction losses. The number of three phase transformer used in the proposed inverter is limited for the purpose of size compaction. At last the grid synchronization is controlled tightly making use of Space Vector Pulse Width Modulation (SVPWM) and enhances the power quality indices like Total Harmonic Distortion (THD) and Power Factor (PF).

Working principle: For the sake of simplification of the analysis, a system that is proposed for the inclusion of two dc sources and C-T^2 Inverter-A (single phase system) is chosen for examination. Proper switching control of the C-T^2 Inverter-A can help in generating half and a whole level of dc supply voltage. The proposed inverteroperation can be grouped into four switching states ($+V_{dc}/2$, $+V_{dc}$, $-V_{dc}/2$ as shown in Fig. 4.

The suitable control of switch S_1 and S_2 employed for generating $+V_{dc}/2$, $+V_{dc}$ dc supply voltage is illustrated in Fig. 4a and b. In a similar manner, the desired control of switch S_3 and S_4 utilized for the generation of $-V_{dc}$, $-V_{dc}/2$ dc supply voltage is indicated in Fig. 4c and d. The C-T^2 inverter has to be switched properly taking the direction of load current and the Output Voltage Levels (OVL) into consideration in accordance with the switch on off conditions as exhibited in Table 1.

Control scheme: The entire scheme of control of the system proposed is illustrated in Fig. 5. The output current of the proposed system can be regulated based on the d-q model. The d-q based scheme works in a rotating reference frame; hence, the currents measured have to be multiplied by sin ωt and cos ωt signals. This synchronized reference signals are received from Phase Locked Loop (PLL).

As indicated in Fig. 5, the measurement of three-phase grid currents and voltages are done and then converted in order to attain the d and q-axis components, i.e., from three-phase a-c frame to two-phase rotation coordinate d-q frame. The park transformation (abc to dq0) is formulated by the equations that follow:

$$I_d = \frac{2}{3}\times\left[I_a \sin(\omega t) + I_b \sin(\omega t - \frac{2\pi}{3}) + I_c \sin(\omega t + \frac{2\pi}{3})\right]$$

Table 1: Switching table

S1	S2	S3	S4	OVL
1	0	0	0	$+V_{dc}/2$
1	1	0	0	$+V_{dc}$
0	0	0	0	0
0	0	1	1	$-V_{dc}$
0	0	1	0	$-V_{dc}/2$

$$I_q = \frac{2}{3}\times\left[I_a\cos(\omega t) + I_b\cos(\omega t - \frac{2\pi}{3}) + I_c\cos(\omega t + \frac{2\pi}{3})\right] \qquad I_0 = \frac{1}{3[I_a + I_b + I_c]}$$

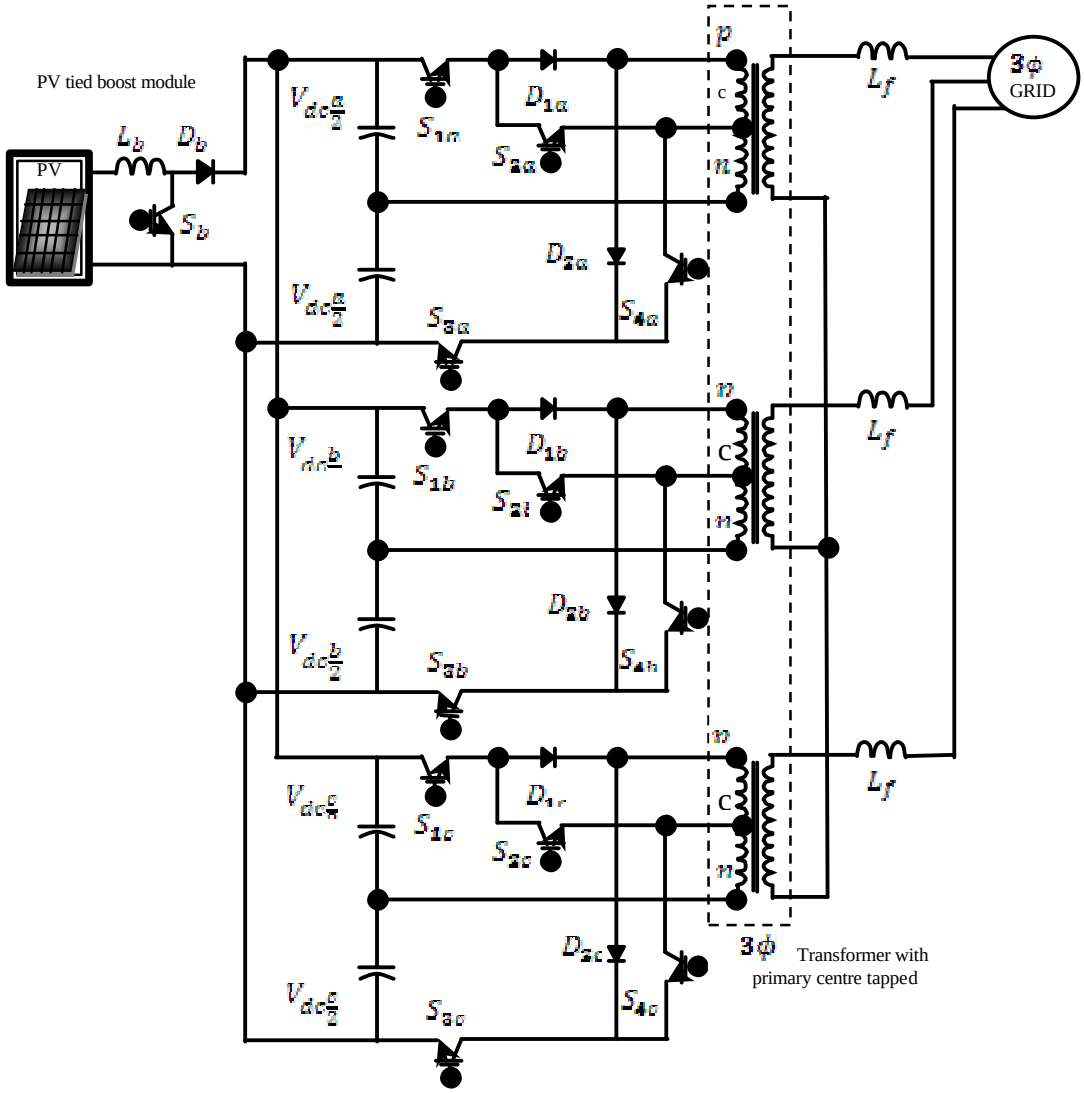

Fig. 3: Proposed C-T^2 inverter with common dc supply

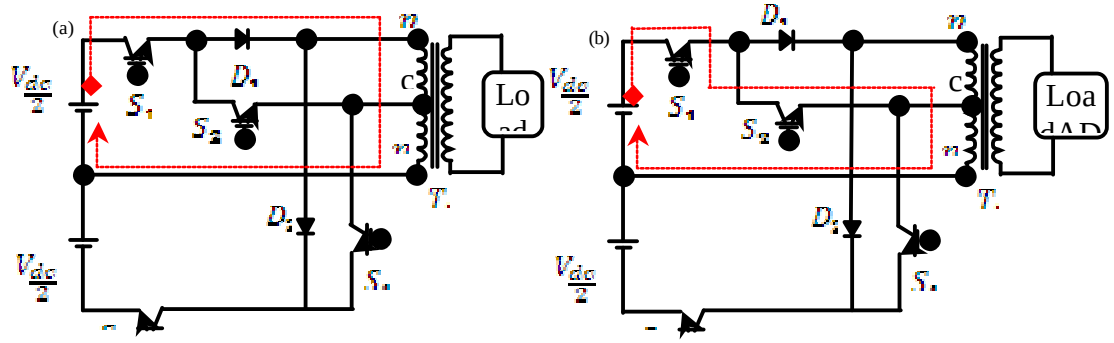

Fig. 4: Continue

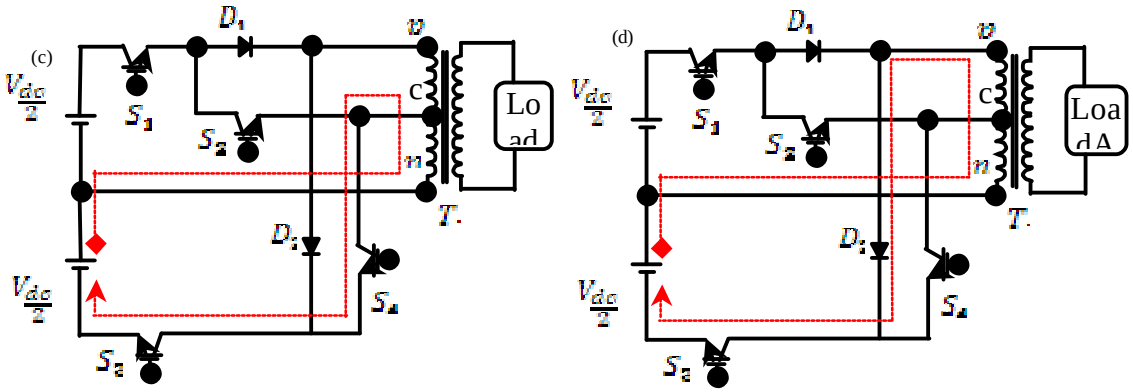

Fig. 4: Working principle of proposed C-T² inverter-A (single phase): a) OVL = $+V_{dc/2}$; b) OVL = $+V_{dc}$; c) OVL = $-V_{dc/2}$; d) OVL = $-V_{dc}$

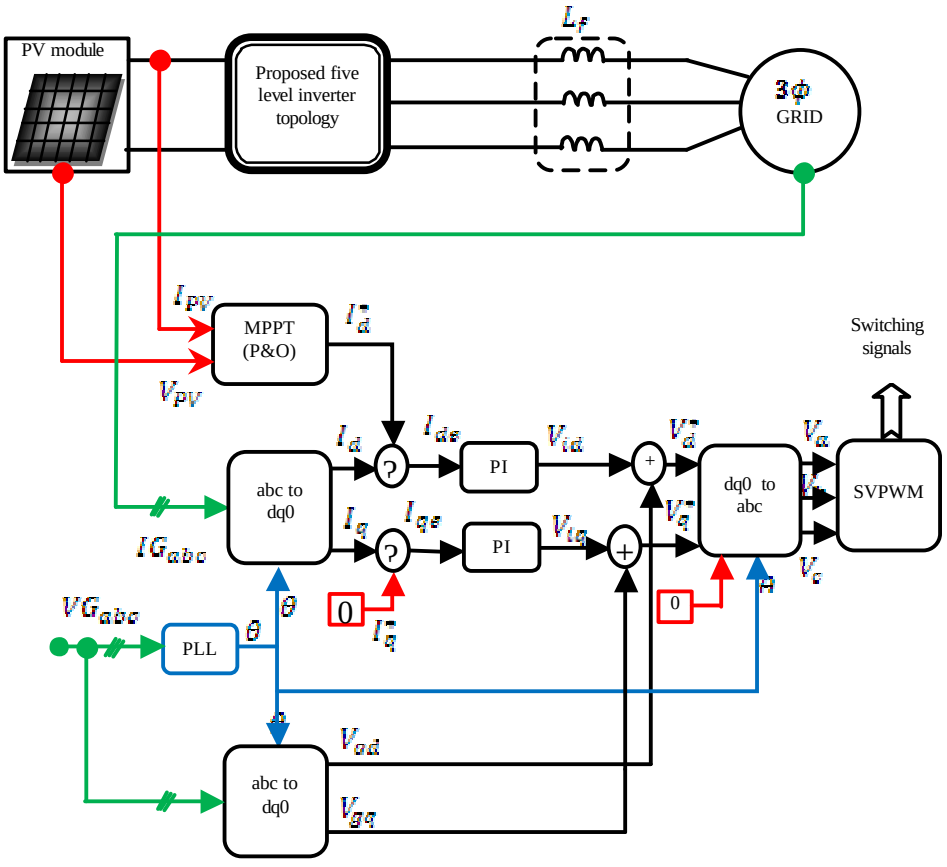

Fig. 5: Control scheme of proposed topology

Where I_a and I_a are the respective three phase Grid currents. The d and q-axis current component closed-loop controls generate the three-phase suitable voltage signals V_a, V_a and V_a (relevant to the modulation index M) that will pressure the original active current I_d and reactive current I_q to be able to track the appropriate reference currents I_d^* and I_q^*, correspondingly. The current references I_d^* and I_q^* are obtained from the PV array output. According to the IEEE recommended practice for utility interface of PV system, many of the PV inverters that are developed for utility-interconnected service work very close to unity power factor.

To achieve a unity power factor, the command I_q^* is fixed to zero.The current error generator then does the comparison of this reference active current (I_d^*) with the original active current (I_d) for generating an error current (I_{de}) that is expressed as:

$$I_{de}(k) = I_d^*(k) - I_d(k)$$

and simillarity for reactive current:

$$I_{qe}(k) = I_q^*(k) - I_q(k)$$

Where 'k' denotes the kth sampling instance. This error current I_{de} is given as input to a Proportional Integral (PI) controller to produce a controlled output voltage V_{id} which is given as:

$$V_{id}(k) = V_{id}(k-1) + K_p\{I_{de}(k) - I_{de}(k-1)\} + K_i I_{de}(k)$$

In the same way V_{iq}, this is given as:

$$V_{iq}(k) = V_{iq}(k-1) + K_p\{I_{qe}(k) - I_{qe}(k-1)\} + K_i I_{qe}(k)$$

Where K_p and K_i are the respective proportional and integral gains of the PI controller. Furthermore, the grid voltage vector is employed in a feed-forward loop for compensating the grid harmonics. The outputs obtained from traditional PI controllers are inductor filter voltage references V_{id} and V_{iq} which get superimposed with V_{gd} and V_{gq} in order to produce the inverter output voltage references V_d^* and V_q^* for SVPWM as in the proposed model. The reference input voltage of SVPWM gets generated making use of the formulations of inverse park transformation (dq0 to abc) which is expressed by the following equations:

$$V_a = V_d \sin(\omega t) + V_q \cos(\omega t) + V_o$$

$$V_b = V_d \sin(\omega t - \frac{2\pi}{3}) + V_q \cos(\omega t - \frac{2\pi}{3}) + V_o$$

$$V_c = V_d \sin(\omega t + \frac{2\pi}{3}) + V_q \cos(\omega t - \frac{2\pi}{3}) + V_o$$

RESULTS AND DISCUSSION

The novel center-tapped primary winding transformer based five level inverter (C-T^2 Inverter) with common dc supply is simulated in a MATLAB/Simulink environment using the sim power-system Toolbox. The proposed three phase (C-T^2 Inverter performances are evaluated using SVPWM technique and the achieved power quality indices obtained at three-phase Grid. Parameters such as Panel Voltage (V_{PV}), Panel Current (I_{PV}), Panel Power (P_{PV}), dc link voltage (V_{dc}), Inverter Voltage (V_{inv}), Grid Voltage

Table 2: The PV panel design specifications

Parameter	Value
Short circuit current at reference condition/SC	5.48 A
Open circuit voltage at reference condition/V_{OC}	43.6 V
MPP voltage at reference condition V_{mpp}	35.8 V
MPP current at reference condition I_{mpp}	5.03 A
Series resistance R_S	0.1133
Irradiance at Standard Test Conditions (STC)	1000 w m^{-2}
Cell temperature at standard test conditions	25 _c
Maximum power @ STC	180 W
Vdc (DC bus) voltage	325 V

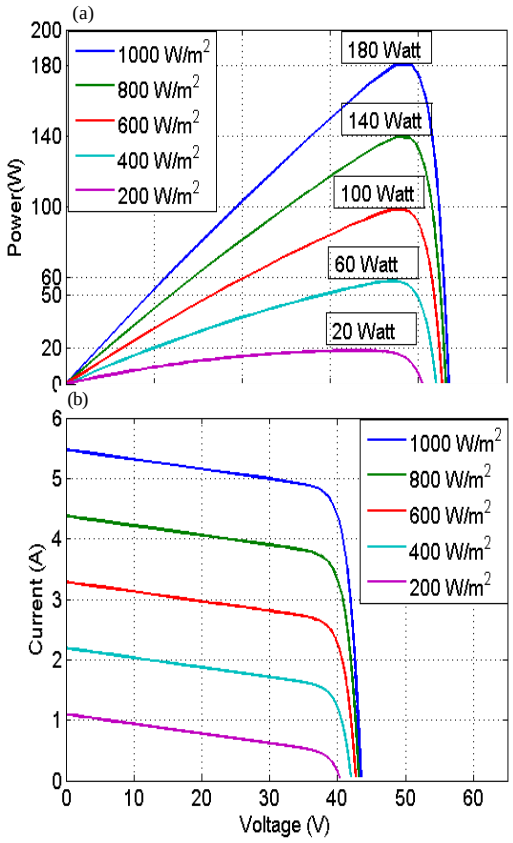

Fig. 6: The P-V curve and I-V curve

(VG_{abc}) and Grid current (IG_{abc}), respectively of the proposed topology are evaluated to demonstrate its proper functioning. Moreover, power quality indices such as power factor (PF), Total Harmonic Distortion (THD) of Grid current are analysed for determining power quality at ac mains. The solar panel specifications used for the simulation study are given in Table 2.

The number of solar panels exploited for supporting simulation is six, i.e., a panel with six connected in series. The maximum power rating of every PV panel is 180 W at STC as provided in Table 2. Hence, the total power rating of the inverter amounts to 1 kW. The maximum power point tracking performed by P&O control algorithm is illustrated in Fig. 6. Figure 6a exhibits the convergence of

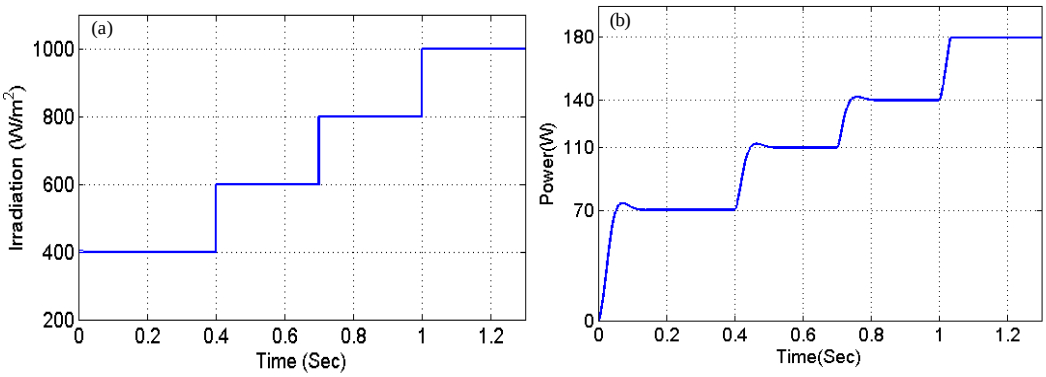

Fig. 7: Dynamic irradiation and maximum power tracking

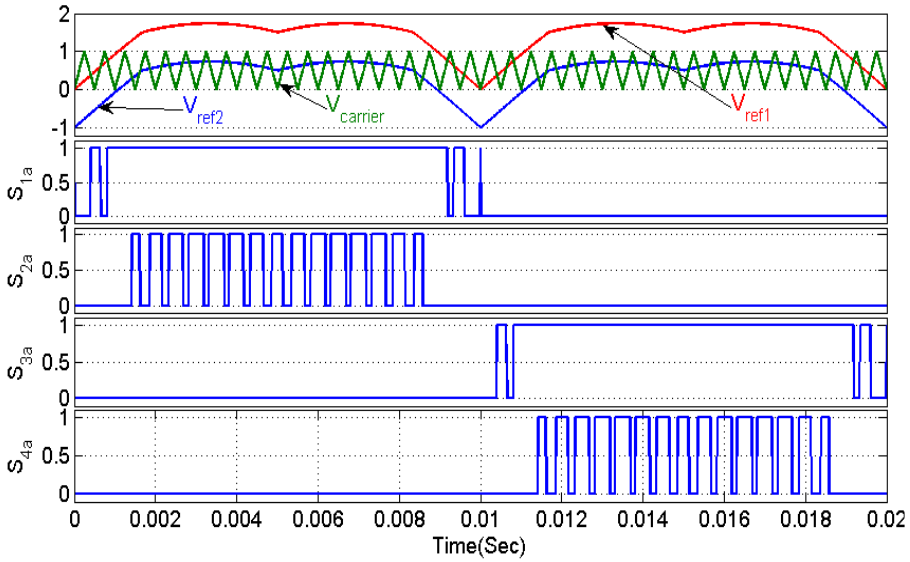

Fig. 8: Switching signals generation using SVPWM

panel Power and Voltage (P-V CURVE) at various irradiation conditions, in the same manner, convergence of panel current and voltage (I-V CURVE) at different irradiation conditions is illustrated in Fig. 6b.

For the purpose of validating the performance of the MPPT algorithm based on P&O, step changes in the irradiance is provided as illustrated in Fig. 7. At first, the irradiance is fixed at 400 W m^{-2} and abruptly it is varied to 600 W m^{-2} at 0.4 sec, 800 W m^{-2} at 0.8 sec and 1000 W m^{-2} at 1sec as indicated in Fig. 7a. Figure 7b illustrates the respective power delivered from the PV panel. From Fig. 7b it is shown that the maximum power which is delivered by the PV panel when irradiance is 1000 W m^{-2} is 180 W; just like that the minimum power delivered by the PV panel if the irradiance is 400 W m^{-2} is 70 W which is observedclearly.

Figure 8 shows the way the PWM Switching signals (SVPWM) are generated by using two reference signals and a triangular carrier signal. The resulting PWM signals for proposed topology switches S_{1a}-S_{1a}, respectively are shown in Fig. 8. Two reference signals V_{ref1} and V_{ref2} which is shown as the red and blue colour in Figure. 8. It will take turns to be compared with the carrier signal ($V_{carriers}$ at a time. If V_{ref1} exceeds the peak amplitude of carrier signal ($V_{carrier}$) then V_{ref2} will be compared with the carrier signal ($V_{carrier}$) until it reaches zero. At this point onward, V_{ref1} takes over the comparison process until it exceeds carrier signal ($V_{carrier}$). This will lead to a switching pattern for SVPWM. Note that four switches of the single phase inverter S_{1a}-S_{4a} are operating at a high switching rate that is equivalent to the frequency of the carrier signal.

The proposed C-T^2 Inverter is assessed on the basis of the switching pattern of SVPWM which is illustrated in

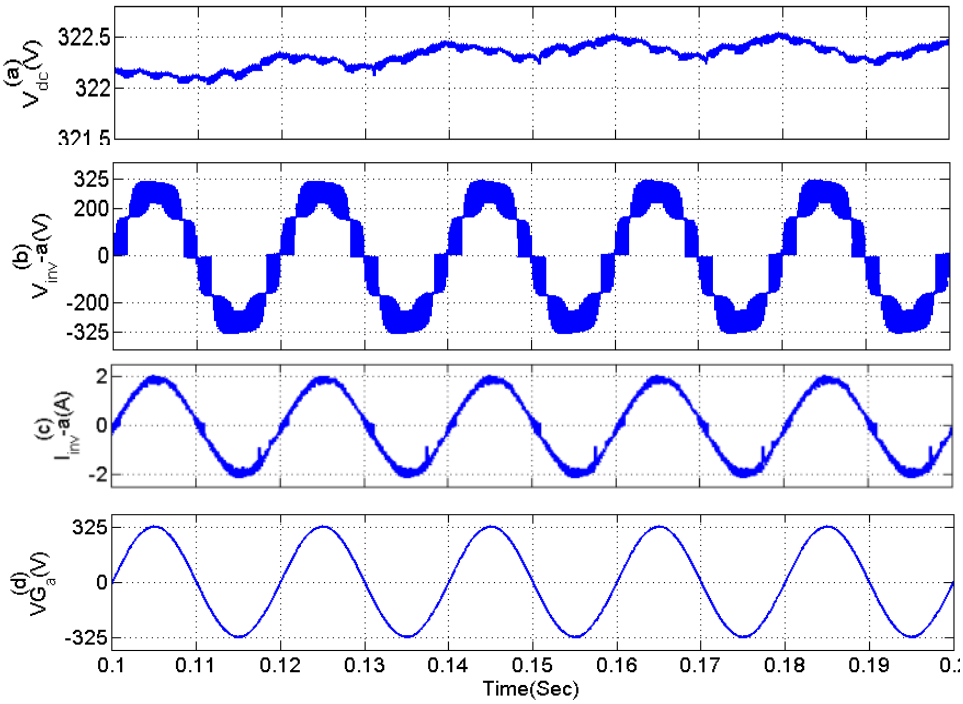

Fig. 9: Inverter-A (single phase) output waveforms

Fig. 9. The PV panels are employed as the input voltage sources. The voltage across the PV panels is called as V_{PV}. The V_{PV} is incremented by the dc-dc boost converter in order to exceed grid voltage VG_{abc} and the voltage across the dc link capacitor is referred to as V_{dc} as indicated in Fig. 9a. The configuration of the proposed C-T^2 five-level inverter is done by two voltage balancing dc capacitors, an C-T^2 inverter with a filter for single phase. The two dc capacitors act as energy buffers between the dc-dc converter and the five-level inverter. The five level inverter proposed is used for generating five output-voltage levels, i.e., 0, $+V_{dc}/2$, $+V_{dc}$, $-V_{dc}/2$, V_{dc}, $-V_{dc}$ as in Fig. 9b. The half of the dc bus voltage ($\pm V_{dc}/2$) is attained by suitable switching of proposed inverter with primary centre tap transformer. Moreover the filtered inverter current and grid voltage per phase is shown in Fig. 9c and d, respectively.

For grid synchronization three phase C-T^2 inverter current is then purified by means of LC filter, after which the filtered current gets fed into the grid. The filtered current looks nearly similar to a sine wave and this current which is in phase with the grid voltage as illustrated in Fig. 10a and b also. The harmonic spectra of supply current is shown in Fig. 10c, respectively. This validates the proposed C-T^2 inverter can achieve the tasks of converting PV power to ac power with unity power factor, low THD%, effectively.

Table 3: Power utility devices comparison of five level inverters

	No. of power devices				Total DC	
Configuration	S_W	D	T	Total	sources	Size
Topology 1	24	-	-	24	6	Large
Topology 2	24	-	2	26	1	Medium
Proposed topology	12*	6	1	19	1	Compact

Excluding components of grid side filter and boost converter; *denotes that IGBT without body diode will be employed in the proposed topology

The proposed topology and the already available topologies are briefly compared and the results are tabulated in Table 3. It indicates the total number of Power Devices (Switch-Sw, Diode-D, Inductor-L, Capacitor-C, Three phase Transformers-T) along with the total number of DC sources. The Topology 1 configuration is not desirable for the application required because of its need of large Power Devices; it takes up big space and has significant losses.

In comparison with the different Topologies, this new Topology has considerably lesser number of components and less number of conducting devices while the proposed configuration provides the minimum conduction losses owing to the conduction of the least number of components while operating in the grid connected mode.

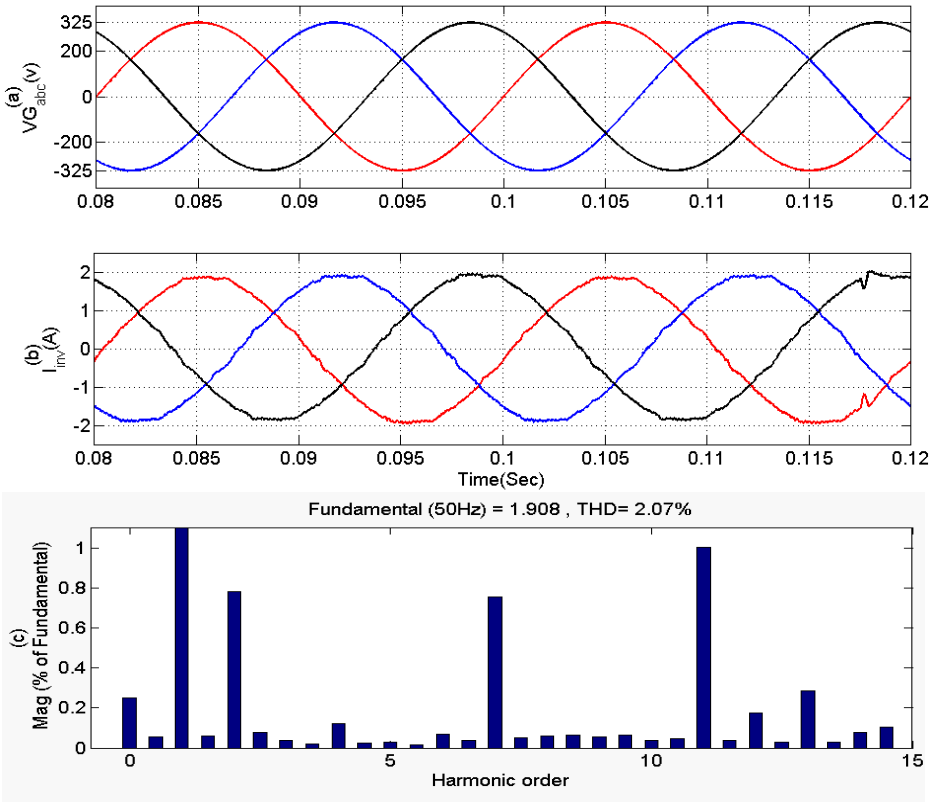

Fig. 10: Proposed three phase C-T^2 five-level inverter: a) Grid voltage; b) Inverter current and c) Harmonic spectra of inverter current

CONCLUSION

A proposed center-tapped primary winding transformer based five level inverter C-T^2 Inverter) performance is evaluated through MATLAB. The developed C-T^2 Inverter topology components is minimal (i.e., 19) compared with existing MLI topologies. The grid synchronization is done using SVPWM with unity power factor and low 2.07% THD, effectively. This approach will be used efficiently in more applications like FACTS devices, Motor Drives, etc.

REFERENCES

Bendre, A., G. Venkataramanan, D. Rosene and V. Srinivasan, 2006. Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation. Ind. Electron. IEEE. Trans., 53: 718-726.

Carrasco, J.M., L.G. Franquelo, J.T. Bialasiewicz, E. Galvan and R.P. Guisado *et al.*, 2006. Power-electronic systems for the grid integration of renewable energy sources: A survey. IEEE Trans. Ind. Electron., 53: 1002-1016.

Chen, A. and X. He, 2006. Research on hybrid-clamped multilevel-inverter topologies. Ind. Electron. IEEE. Trans., 53: 1898-1907.

Cheng, Y., C. Qian, M.L., Crow, S. Pekarek and S. Atcitty, 2006. A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage. Ind. Electron. IEEE. Trans., 53: 1512-1521.

Chiasson, J.N., B. Ozpineci and L.M. Tolbert, 2007. A five-level three-phase hybrid cascade multilevel inverter using a single DC source for a PM synchronous motor drive. Proceeding of the Twenty Second Annual IEEE Conference on Applied Power Electronics APEC, February 25-March 1, 2007, IEEE, Anaheim, CA., USA., ISBN: 1-4244-0713-3, pp: 1504-1507.

Kang, F.S., S.J. Park, M.H. Lee and C.U. Kim, 2005. An efficient multilevel-synthesis approach and its application to a 27-level inverter. Ind. Electron. IEEE. Trans., 52: 1600-1606.

Krug, D., S. Bernet, S.S. Fazel, K. Jalili and M. Malinowski, 2007. Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives. Ind. Electron. IEEE. Trans., 54: 2979-2992.

Lai, J.S. and F.Z. Peng, 1996. Multilevel converters-a new breed of power converters. IEEE Trans. Ind. Appl., 32: 509-517.

Lezana, P., C.A. Silva, J. Rodriguez and M.A. Perez, 2007. Zero-steady-state-error input-current controller for regenerative multilevel converters based on single-phase cells. Ind. Electron. IEEE. Trans., 54: 733-740.

Marchesoni, M., M. Mazzucchelli and S. Tenconi, 1988. A non conventional power converter for plasma stabilization. Proceedings of the 19th Annual IEEE Power Electronics Specialists Conference, April 11-14, 1988, Kyoto, Japan, pp: 122-129.

Meynard, T.A. and H. Foch, 1992. Multi-level conversion: High voltage choppers and voltage-source inverters. Proceedings of the 23rd Annual IEEE Conference on Power Electronics Specialists, June 29-July 3, 1992, Toledo, Spain, pp: 397-403.

Nabae, A., I. Takahashi and H. Akagi, 1981. A new neutral-point-clamped PWM inverter. IEEE Trans. Ind. Appl., IA-17: 518-523.

Rech, C. and J.R. Pinheiro, 2007. Hybrid multilevel converters: Unified analysis and design considerations. Ind. Electron. IEEE. Trans., 54: 1092-1104.

Rodriguez, J., J.S. Lai and F.Z. Peng, 2002. Multilevel inverters: A survey of topologies controls and applications. Ind. Electron. IEEE. Trans., 49: 724-738.

Rodriguez, J., S. Bernet, B. Wu, J.O. Pontt and S. Kouro, 2007. Multilevel voltage-source-converter topologies for industrial medium-voltage drives. Ind. Electron. IEEE. Trans., 54: 2930-2945.

Soto, D., R. Pena, L. Reyes and M. Vasquez, 2003. A novel cascaded multilevel converter with a single nonisolated DC link. Proceeding of the 34th Annual IEEE Conference on the Power of Electronics Specialist PESC'03, June 15-19, 2003, IEEE, New York, USA, ISBN:0-7803-7754-0, pp: 1627-1632.

Tolbert, L.M., Z.P. Feng and T.G. Habetler, 1999. Multilevel converters for large electric drives. IEEE Trans. Ind. Appl., 35: 36-44.

Watson, A.J., P.W. Wheeler and J.C. Clare, 2007. A complete harmonic elimination approach to DC link voltage balancing for a cascaded multilevel rectifier. Ind. Electron. IEEE. Trans., 54: 2946-2953.