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Analysis and Design of Low Power All Digital Phase Locked Loop via Dynamic Logic-Phase Frequency Detector in a Standard 0.25-µm CMOS Technology

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Abstract: A low power design of All Digital Phase Locked Loop (ADPLL) have become more attractive. It has better programmability, testability, portability and stability on ADPLL various actions and has good noise immunity. All digital system clock generation digital phase locked loop instead of traditional analog PLL is widely studied. The proposed new dynamic logic- phase frequency detector extends the detection range and eliminates the polarity reversal issues and increasing the speed of locking range at the output. Note the comparison between the proposed phase error such as the design of low power clock and the feedback clock is divided power Consumption respectively. ADPLL design through a dynamic logic phase frequency detector and is fabricated in parallel DTC and consumed the associated power 1.75 and 8.16 mW, respectively from 1.8 volts of electricity.

Key words: All Digital Phase Locked Loop (ADPLL), Time-to-Digital Converter (TDC), vernier, delay latch, India

INTRODUCTION

Phase-Locked Loop or Phase Lock Loop (PLL) is an old technology dating from 1930. It is a control system generates an output signal related to the phase of the phase an input reference signal shown in Fig. 1. The widespread use PLL began in the 1940s television receivers. PLL is analog signal, it has four types, namely linear PLL; digital phased locked loop; all digital phased locked loop; software PLL. Only digital signals are input to the ADPLL instead of traditional analog PLL. The charge-pump design has various approaches using switches and inverters and a passive RC low-pass filter. The disadvantages of analog PLL is sensitive to operating variation, phase noise is high and the reference clock cycle requiring is more as a result, the lock time is not faster. These limitations are overcome by ADPLL to achieve the flexible clock generation and the fast locking ability of the reference clock cycle. Design of ADPLL with each functional story is provided, building block such as DTC and the DCO. One of the dynamic logic-phase frequency detectors that virtually eliminates dead zone is a design based on dynamic CMOS logic in which the PFD's output signals are directly used to reset the PFD without any intermediate logic the design has been further modified by high performance dynamic logic to eliminate the probability of short-circuit current. The reported dynamic-logic phase frequency detector features near zero phase error. However, there is still need for blind-zone improvement. Dynamic phase compensation is to accomplish fast locking in All Digital PLL.

The recommended configuration is implemented using ADPLL design to reduce area and lower power. ADPLL effective performance is based on high resolution as well as high conversion rate has not been an easy task, similar to an ADC. A digital circuit offers many advantages compared to the analog or linear PLL architecture. Furthermore, analog functional blocks reduce the sensitivity to Process-Voltage-Temperature (PVT) variations. ADPLL has two operation modes which are frequency acquisition mode and phase acquisition mode (Chuang *et al*., 2012), a coarse-fine time-to-digital converter that amplifies a time residue to improve time resolution (Kim *et al*., 2013), edge locations are digitally measured by using the time-to-digital converter (Chen *et al*., 2011). Another type of PLL is novel hardware-based All-Digital Phase-Locked Loop (ADPLL) is proposed for grid interface converters to detect the frequency and phase angle based on the voltage zero crossings (Lee and Abidi, 2008), TDC efficiently generates the exponent-only information for fractional time difference (Daniels *et al*., 2010), phase-error compensator is introduced to avoid big phase-error downfalls caused by large output glitches originating from a high-speed accumulator (Wu *et al*., 2010), delay line in the reference signal path allows the time-to-digital converter core to

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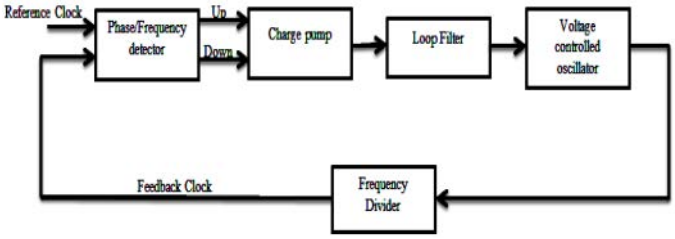

Fig. 1: General block diagram of basic PLL

operate at a low duty cycle with about 96% reduction of its average power consumption (Lee *et al*., 2012; Hung and Liu, 2011), Frequency Estimation Algorithm (FEA) for an All-Digital Phase-Locked Loop (ADPLL) instead of the traditional binary frequency-searching algorithm (Lee *et al*., 2012; Xu *et al*., 2010), Adaptive Loop Gain Controller (ALGC) reduces the nonlinearity of the Bang-Bang Phase Frequency Detector (BBPFD) and reducing output jitter (Dudek *et al*., 2000), two unique characteristics of discrete-time circuits not readily possible with the traditional analog implementations: sequential use of coarse-to-fine step size varactors; hitless gear shifting (Kratyuk *et al*., 2007), An inductor is used to extend the frequency tuning range of a 40-GHz digitally controlled oscillator (Kim *et al*., 2010).

MATERIALS AND METHODS

Proposed algorithm: The modification of the Dynamic-Logic PFD is shown in Fig. 2. The goal of this design is to create a delayed input signal (REF1 and VCO1) with a delay larger than that of the blind-zone; therefore it is termed as the Delayed-Input-Pulse Dynamic PFD (DIP-PFD). The REF and VCO signals are buffered at the input by a predetermined delay τ that is larger than the blind-zone (τ>TRST). When, the PFD is operating in the blind-zone, a delayed version of the input signal is activated so that its rising edge comes after the reset phase and allows the PFD to properly detect the rising pulse edge. The operation in linear range (φ error [0, 2π-Δ]) is described below. Initially, both REF and VCO are low. The nodes U1 and D1 are precharged high (Fig. 3). When, the REF signal is leading the VCO signal, U2 is pulled low on the rising edge of the REF signal and the circuit generates UP pulse. When the VCO signal arrives, D2 is pulled low on the rising edge of VCO signal and the circuit generates a DN pulse.

The UP and DN pulses initiate a reset operation that deactivate the outputs, hence the width difference between UP and DN pulses is equal to the phase difference of two input signals (Fig. 4). Circuit diagram of the DIP-PFD a typical example of a timing waveform for the operation in the blind-zone (φ error [2π-Δ, 2π]) is shown in Fig. 5.

The only way to increase the detection range of the DPFD is to decrease the reset time of the PFD. The reset time of the DPFD is actually given by the sum of the discharge time of pre-charge-node of first stage, the charging time of pre-charge-node of second stage and the discharge time of the output inverter. During the reset operation, the DPFD can be considered as cascade connection of three inverter stages. It consists of transistors U2-U3 (D2-D3), U5-U6 (D5-D6) and U8-U9 (D8-D9). So by proper inverter sizing, the inverter delay is reduced.

The UP pulse is generated if the input REF signal is leading the VCO signal. This UP pulse turns off MU2 to block any changes through MU1. Then, the DN pulse is generated on the VCO rising edge. Reset operation is initiated and at the end the UP and DN signals are pulled low. If the REF rising edge comes during the reset phase, it will be delayed by ô to produce REF1. Since, the delay is larger than the reset phase width (τ>TRST), REF1 rising edge comes after the reset phase and it can be detected by PFD. Hence, the DIP-PFD eliminates the possibility for polarity reversal at its outputs.

A timing diagram in Fig.4 shows the PFD operating in the blind-zone. When the REF signal is leading the VCO signal with phase difference between 2π-Δ to 2π, the rising transition of REF occurs during the reset phase. Because of UP and VCO are both high at that time, CTRL1 signal is low and the pass transistor MU0 is OFF. The rising edge of REF is blocked by the MU0 until the reset phase is finished. Then the REF rising edge is propagated through MU0 and allows the PFD to correctly detect the REF edge. Therefore, the DIP-PFD eliminates the blind-zone problem, extending the detection range.

By interchanging the transistors U6 and U7 (D6 and D7), the signal path length is reduced because the resistance and capacitance U6 (D6) will not come in the

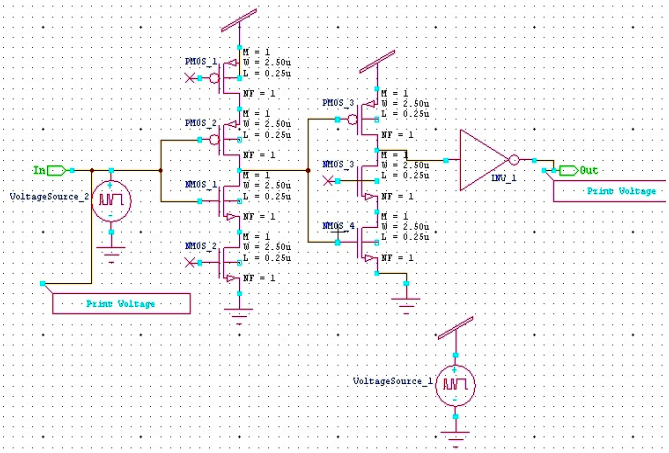

Fig. 2: Dynamic logic DPFD up conversion

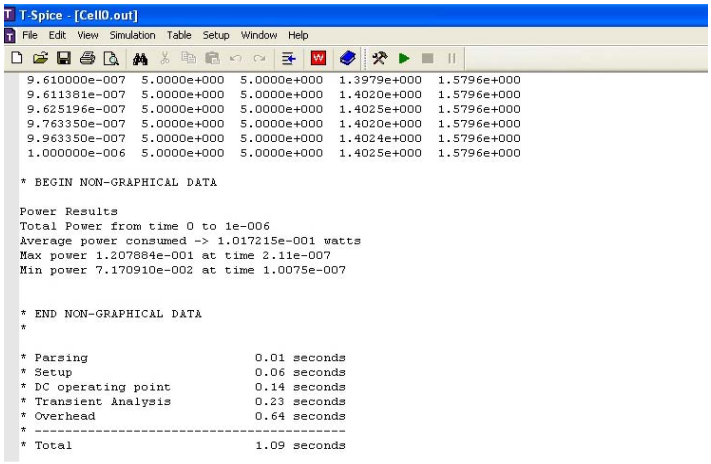

Fig. 3: Timing and power result on DPFD operating in up conversion

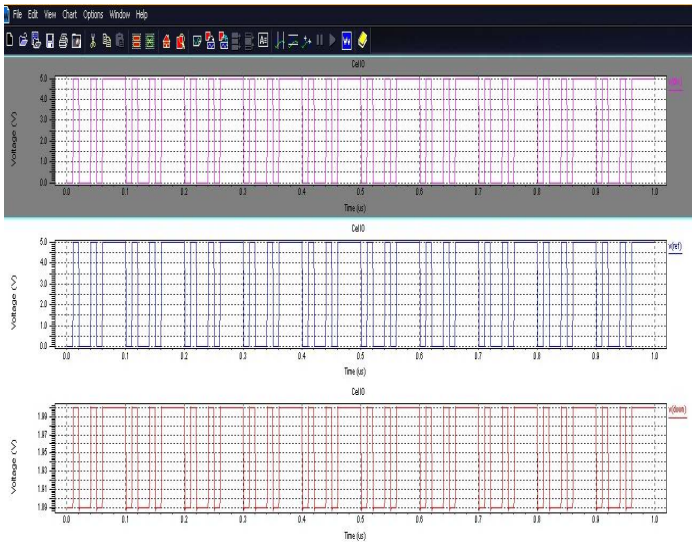

Fig. 4: Timing diagram of DPFD operating in up conversion

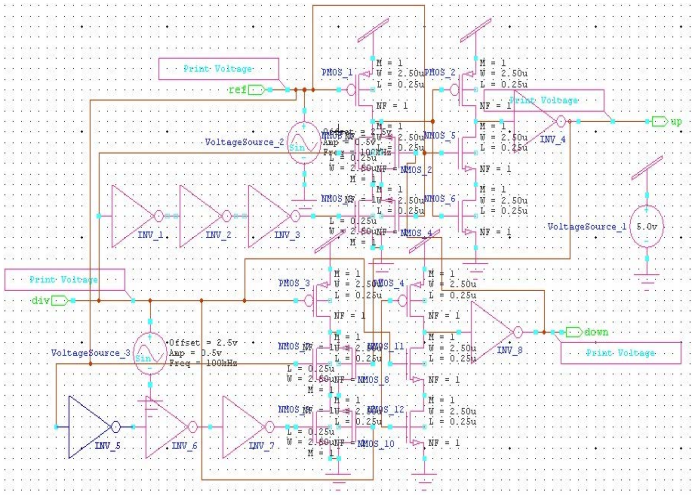

Fig. 5: Dynamic logic PFD down conversion

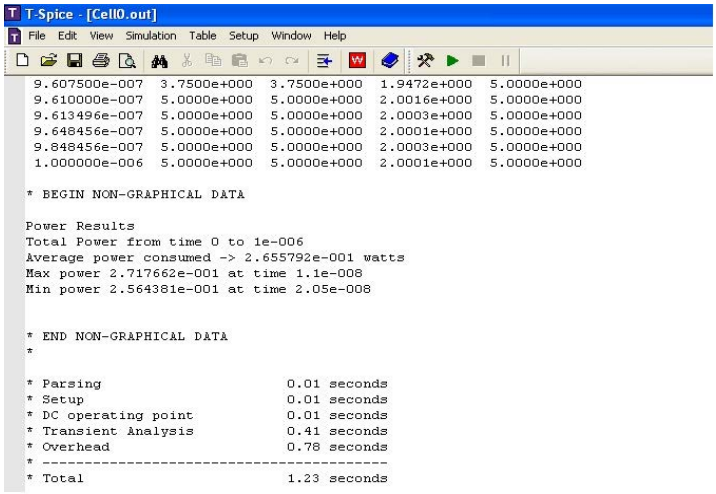

Fig. 6: Timing and power analysis of PFD with down conversion

signal path. This will reduce the delay of the circuit and in turn, the reset time. As the final step, pre-charge transistors are included to further increase the detection range of the DPFD.

In an effort to design a PFD capable of working at gigahertz frequency with minimum dead-zone, minimum phase offset and reduced blind-zone, we have proposed a new domino-logic PFD. Our design goals are accomplished by overcoming the drawbacks existing in previous dynamic PFDs. Circuit integrity is maintained in this design (Fig. 6 and 7).

Implementation: The block diagram of proposed ADPLL is shown in Fig. 8. The parallel TDC shown in Fig. 9. It 5 requires 28 transistors per delay stage in an implementation one D flip-flop uses 24 transistors. Figure 9 requires nine transistors per stage. Hence, the proposed ADPLL transistor count is mainly reduced by the TDC circuit.

Parallel TDC: The start signal applied to all delay elements in parallel. The schematic design of parallel TDC is shown in Fig. 9. There is on the output signal will stop all delay elements at the same time, as models. Instead of propagating the differential start signal, stop signal is delayed to avoid differential mismatch problem. Configuring the gates not in a chain but in parallel

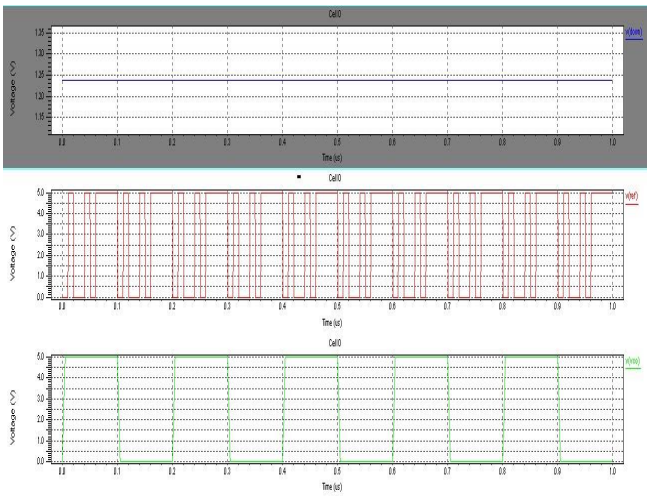

Fig. 7: Timing diagram of DPFD operating in down conversion

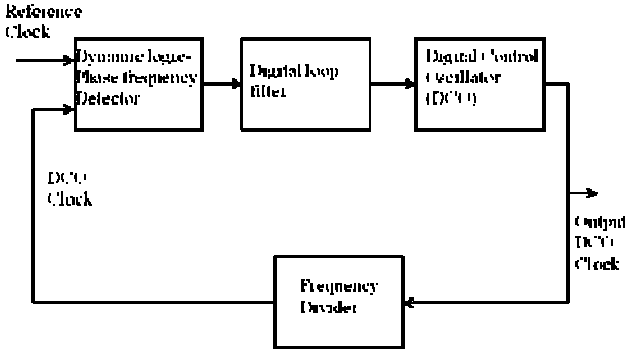

Fig. 8: Block diagram of proposed ADPLL

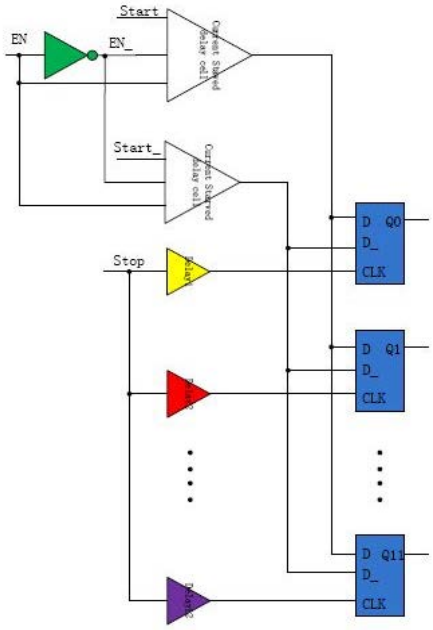

Fig. 9: Diagram of parallel TDC

generates TDC depicted in Fig.10. The start signal applied to all delay elements in parallel. On the rising of stop signal the outputs of all delay elements are sampled at the same time. Instead of propagating the differential start signal, stop signal is delayed to avoid differential mismatch problem. The delay cells connected to stop signal are sized for delays:

$$Td_i = Td_0 + \Delta Td.N \quad (1)$$

The time difference between the delayed stop signal is quantized with a resolution Tlsb = ΔTd. The conversion results are available immediately after the rising of stop signal (Fig. 11).

Digital loop filter: Digital loop filter shown in the schematic diagram in Fig. 12-14. Digital loop filter to suppress high frequency signal from phase frequency detector and elements dosing low pass filter. It oscillator provides a control signal is proportional to the phase difference between the reference and PLL output, since

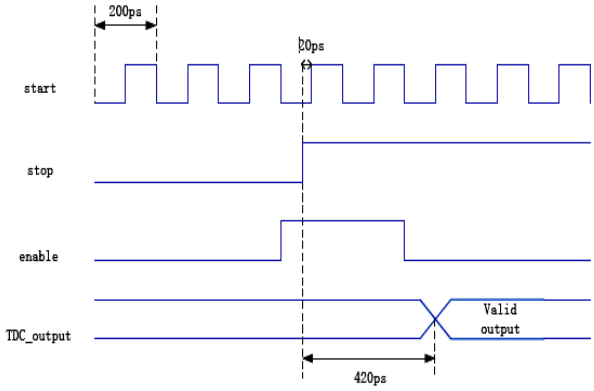

Fig. 10: Timing of the interfaces of parallel TDC

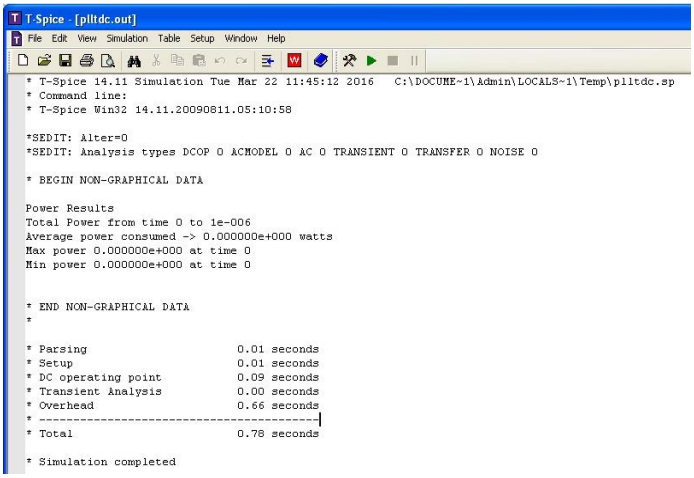

Fig. 11: Timing and power result on parallel TDC

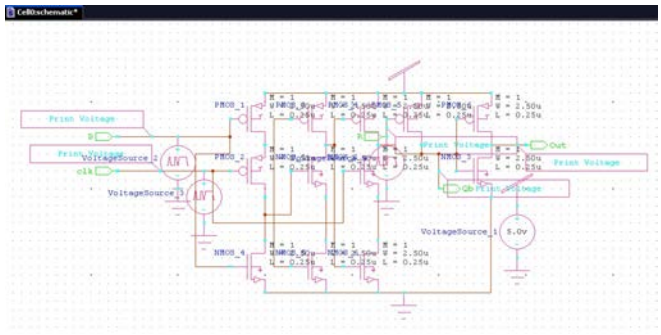

Fig.12: Schematic design of digital loop filter

conventional phase/frequency detector and charge pump. The width of the phase error encoding free ratio pulses train, instead DTC does not phase-domain operation. Any reference in terms of accelerating the build a digital loop filter allows you to see the between the point of reference for optimal performance phase noise and phase noise oscillator. As a result, simply ADPLL for Bluetooth designed to provide the first or second row Filter, in contrast to the third-order filter traditional PLLs. Cellular systems, however the best filter is needed and actively. The first phase of the protected 400 kHz attenuate noise offset. That there is such a sharp filter, it is possible in a controlled manner traditional PLLs.

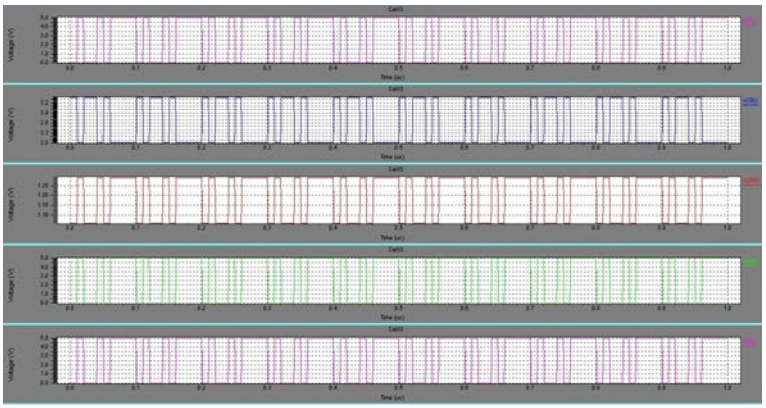

Fig. 13: Timing diagram of digital loop filter

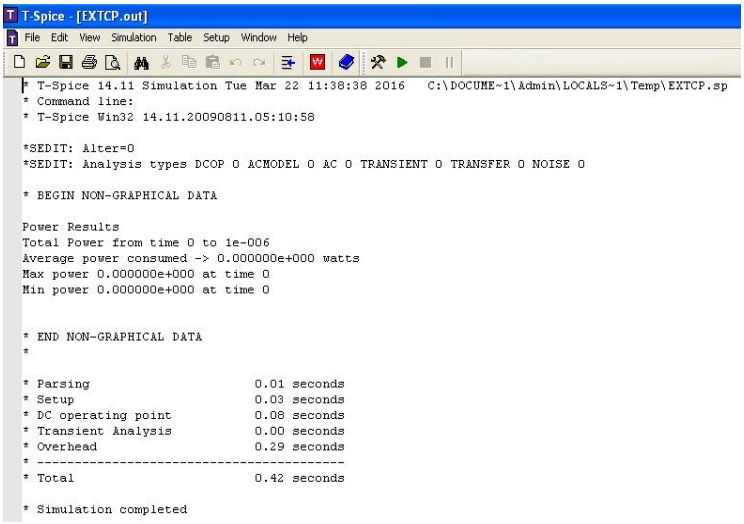

Fig. 14: Timing and power result on digital loop filter

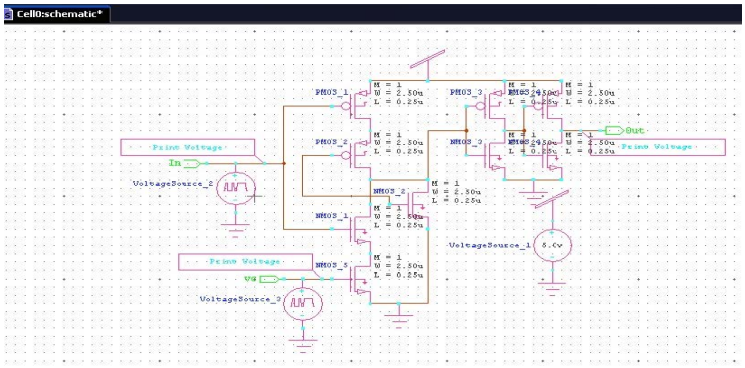

Fig. 15: Schematic design of DCO

Digitally Controlled Oscillator (DCO): The DCO is the combination of a Digital-to-Analog Converter (DAC) and a Voltage Controlled Oscillator (VCO).The Schematic design of DCO shown in Fig. 15-17.

The DCO is a three-staged ring oscillator that consists of a couple of normal delay cells Type-1 and one delay cell with a phase-shifting function Type-2. For the resettable design, we employed the last delay cell of

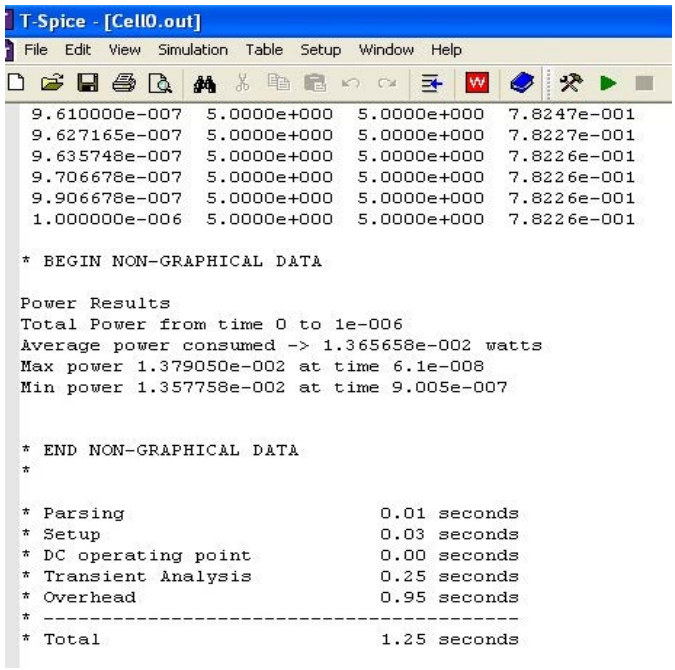

Fig. 16: Timing and power analysis of DCO

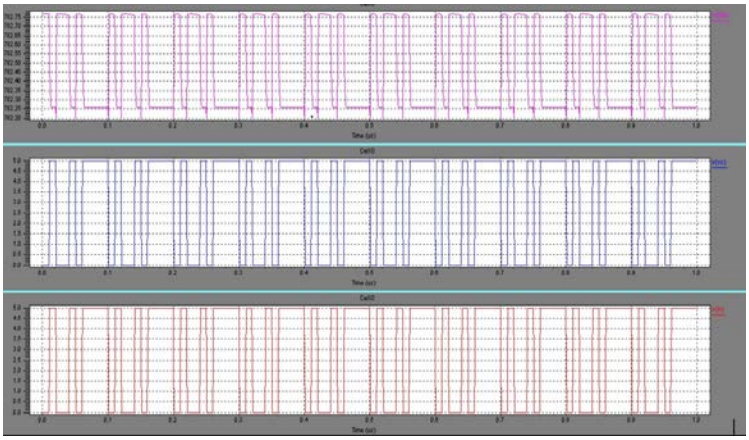

Fig. 17: Timing wave form of DCO

Type-2. When rst is asserted to 0, the last cell is transformed from an inverting buffer to a non inverting buffer. The rest of the first two delay cells of the same value, i.e., 1 are initialized at 0 and the total base DCO name, the status of the DCO 360° is the oscillating stops and keeps this position. First time 1 returns, DCO oscillating resumes from this reset level. In this design, each delay cell voltage swing. The replica bias circuit is determined. Once rst returns to 1, the DCO resumes oscillating from this reset status. In this design, voltage swing of each delay cell is determined as by the replica bias circuit. Each delay cell has an exceptional setting a difference supply noises. Digital capacitance tuning is usually realized by adding or removing some of the size of the unit varactor, the frequency step size too small, according to the minimum amount of capacitance which is usually varactor only by small amounts of a particular technology. In this work, a capacitance tuning program varactor funds being used to apply the incremental amount. It can achieve both high frequency resolution (approximately 6 KHz) and large linear frequency tuning range with small differential nonlinearity. One of the key design criteria for a DCO to provide and accept the need to maintain sufficient control of the word resolution thermo decoder. Simulation of the system is that it is an important factor in the performance of the digital PLL.

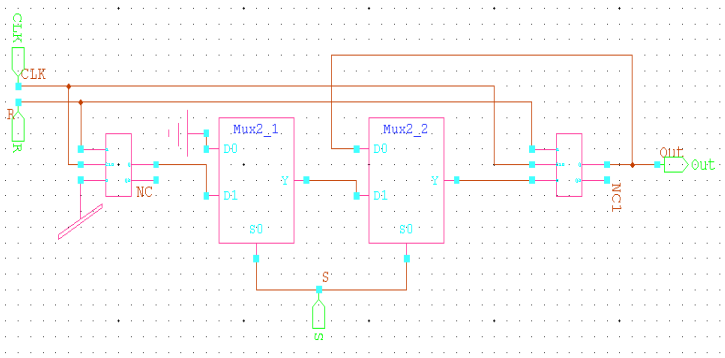

Fig. 18: Schematic design of frequency divider

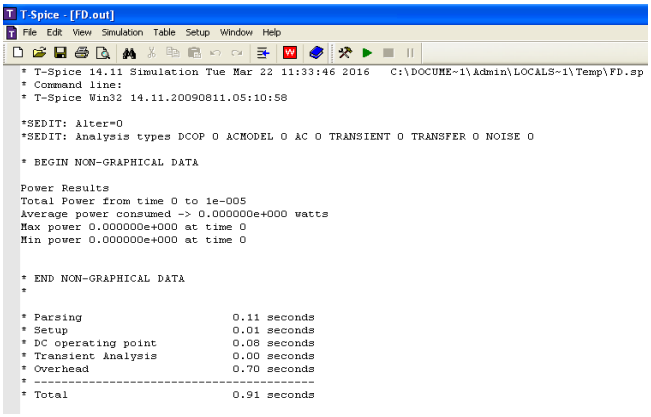

Fig. 19: Timing and power result on frequency divider

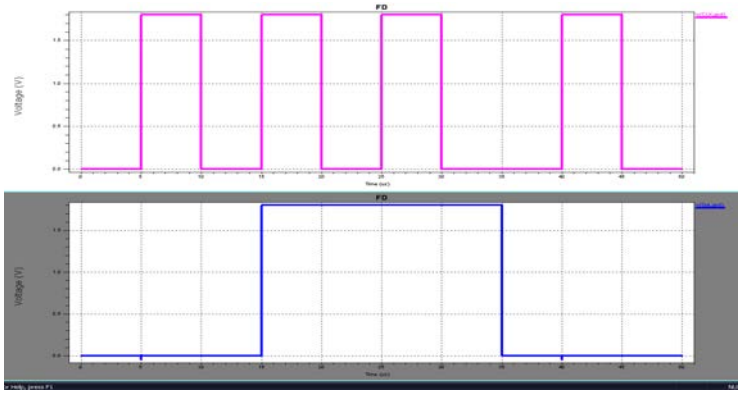

Fig. 20: Timing diagram of frequency divider

DCO was by design all seven-bit input using a linear feedback shift register sequences tested. DCO operating range 320 MHz to 180 MHz. The control word of design which belongs to the content of the "00000000" the DCO frequency is 49.93 MHz and for "11111111" it is 322.9MHz.

Frequency divider: The frequency divider schematic design is shown in Fig. 18-20. It's divider between the oscillator feedbacks into the phase detector to produce the frequency synthesizer. It's particularly useful for the radio transmitter applications and it's also divided between reference clock and reference input to the phase detector. Release DCO must be formulated to match the reference frequency. It is an input frequency (clock) in good time depending on the input to be divided by a border. Deciding on what range of input clock frequency

will divided. There is a clock frequency controls the frequency divider input. Input 4-bit number. Following the reset input will be added to the circuit itself. The denominator consists of 4-bit divide by Frequency divider, PLL with a multiplication factor of four to carry implemented using divider D flip-flops. Two light DCO clock is an input and the second non-inverted output. There DCO clock is divided by four lock flip-flop. The study is divided DCO clock continues PFD any differences are identified by reference clock signal. Cause a frequency or phase variation PFD become activated and re-synchronization of the two clocks will be achieved.

We use the dual-modulus frequency divider which includes a counter that has two possible counts and can operate only for integer divisors.

RESULTS AND DISCUSSION

Figure 21-23 shows the overall implementation of ADPLL and it consumes the power of 5.76 mW from a 1.8 V supply. The proposed system is to design a low power ADPLL using a dynamic logic phase frequency detector consumes a power of 1.75 mW. The proposed system of parallel TDC consumes power of 8.16 mW. ADPLL was implemented in a standard IBM 13 CMOS process technology.

The Proposed ADPLL was simulated using EDA tool with 0.25-μm technology at 386 MHz frequency. It consumes 5.76 mW. The proposed algorithm of dynamic logic phase frequency detector increases fast locking ability and reduces delay time which helps to quickly lock with the input reference signal (Table 1 and Fig. 24 and 25).

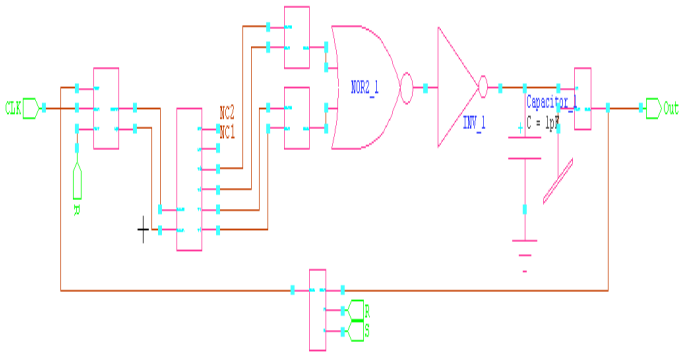

Fig. 21: Overall implementation of ADPLL

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* BEGIN NON-GRAPHICAL DATA

Power Results
v1 from time 0 to 0.0005
Average power consumed -> 1.695588e-003 watts
Max power 6.771167e-003 at time 0.00047
Min power 1.985536e-004 at time 4.50001e-005


* END NON-GRAPHICAL DATA
*

* Parsing                          0.03 seconds
* Setup                            0.06 seconds
* DC operating point               0.09 seconds
* Transient Analysis               5.30 seconds
* Overhead                         1.64 seconds
* ---------------------------------------------
* Total                            7.12 seconds
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Fig. 22: Over all implementation of power result in proposed ADPLL

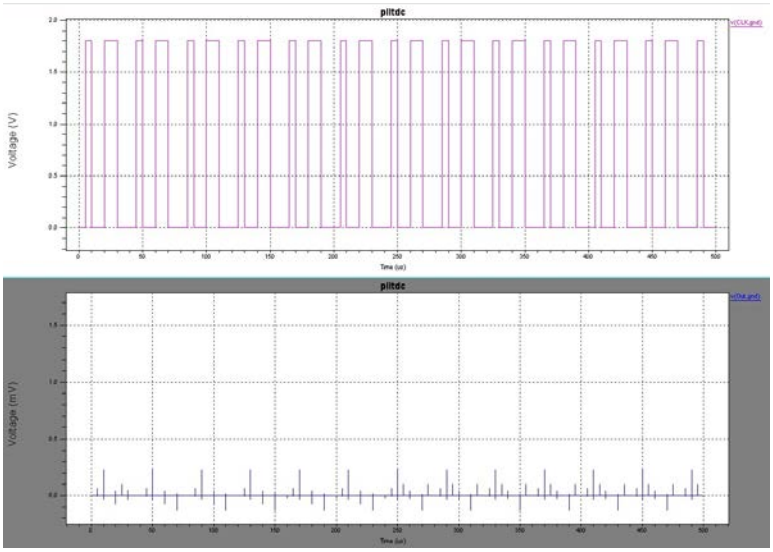

Fig. 23: Timing diagram of overall ADPLL

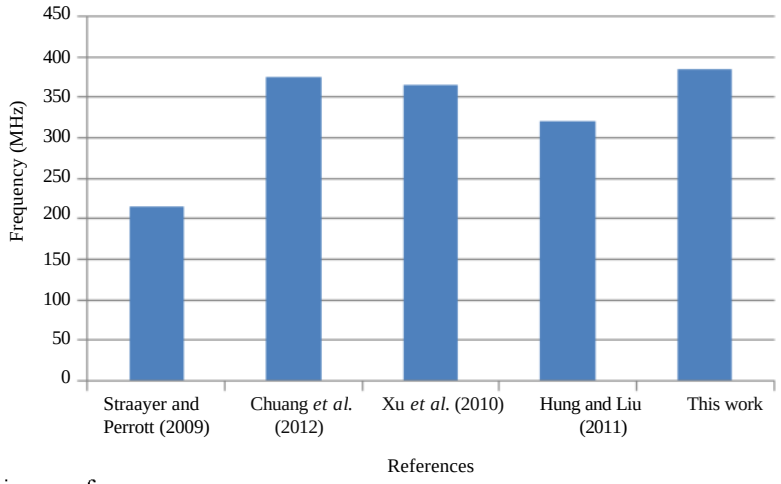

Fig. 24: Chart comparison on frequncey range

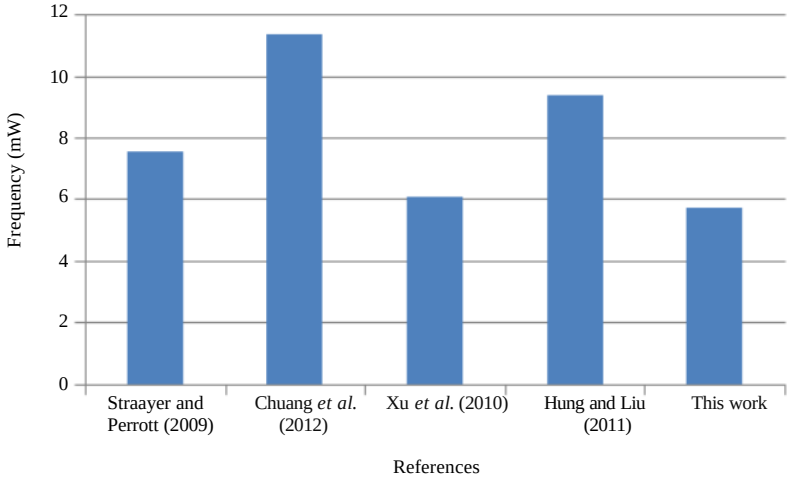

Fig. 25: Chart comparison on power analysis

Table 1: Various parameter analysis

Parameters	References				
	Straayer and Perrott (2009)	Chuang *et al.* (2012)	Xu *et al.* (2010)	Hung and Liu (2011)	This work
Proposed system	TDC	FFCD	DCPLL	DCO	DPFD
Frequency range	215 MHz	376 MHz	366 MHz	320 MHz	386 MHz
Power	7.6 mW	11.394 mW	6.1 mW	9.43 mW	5.76 mW

CONCLUSION

In this research, ADPLL architecture with dynamic logic phase frequency detector and parallel TDC maximum power consumption is 1.75mW and 8.16 mW from a 1.8 V supply. The overall implementation of the proposed ADPLL which consumes the power on 5.76 mW. On comparing the various parameters dynamic logic phase frequency detector architecture in ADPLL provides the better solution of fast locking, high noise immunity and consumes low power.

RECOMMENDATIONS

The schematic approach of the ADPLL has been performed the simulation level efficiently. Since the schematic approach of the layout design can be performed by hand mechanism. While, using the layout function with the back-end EDA tool it could be performed on power area and lock time difference of the two various implementations. Layout design part in which is vary the power and area optimization compare with the schematic approach for reduce the area and power efficiently here by elaborate the layout contribution with the simple complexity of the design with high frequency up-to 255GHz.

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