Asian Journal of Information Technology 15 (11): 1670-1677, 2016
ISSN: 1682-3915

Design of a Reduced Carry Chain Propagation Adder Using FinFET

[1]S. Saravanan and [2]V.M. Senthil Kumar
[1]Department of Electrical and Electronics Engineering,
Muthayammal Engineering College, Rasipuram, Tamil Nadu, India
[2]Department of Electronics and Communication Engineering,
Vivekanandha College of Engineering for Women,
Elayampalayam, Tiruchengode, Tamil Nadu, India

Abstract: In this research, a FinFET based methodology for the design of self timed adder is proposed which provides lesser power consumption when compared to CMOS. The FinFET based adder is designed to reduce the carry chain Propagation delay time. The adder is designed using double gate FinFET in 32nm technology. The Proposed design based on FinFET further reduces the second order effects which occur in CMOS based digital circuits below 65 nm technology. A Self Controlled Voltage Level (SVL) Circuit for the adder drastically reduces the standby power. The design also eliminates the short channel effects occurring in conventional CMOS circuits. Experiments were carried out on designing a FinFET based NAND logic gate using SVL technique and the performance is compared with the conventional CMOS based NAND gate. The proposed FinFET based self timed adder performance is compared with the existing conventional design. The power is reduced by 20% in the proposed design. Experimental results on the 32 nm predictive technology model for FinFET adder design demonstrate the effectiveness of the proposed optimization framework.

Key words: FinFET, SVL, adder, carry chain propagation, NAND gate, independent gate, shorted gate

INTRODUCTION

In today's communication field plenty of handheld devices have been innovated. The advancement in technology happened due to miniature of transistors to realize higher speed and packing density. Due to extreme large integration the modern VLSIs face problem in reducing the power consumption. The first step in reducing the power consumption is to reduce the supply voltage but it also reduces the current driving capability of the device. To improve the driving capability and to achieve higher performance new devices is the choice in the first degree. Even though, CMOS technology improved the performance of digital circuits but moving towards smaller devices creates problem. When CMOS devices are scaled below 45 nm the circuits faces problems like Short Channel Effects (SCE), Sub-Threshold Leakage (STL) device variations and gate dielectric leakage. This is due to the fact that the controllability of the gate over depletion region reduces when scaling the devices below 65nm technology (Mishra *et al*., 2011). The SCE creates major issues including the variation in threshold voltage, lack of pinch off, Drain Induced Barrier Lowering (DIBL) and parasitic effects. The width quantization reduces (Gupta and Roy, 2013) the flexibility in design and hence becomes more critical due to process variations in scaled technologies. The other important issue of planar single gate MOS devices (Swahn and Hassoun, 2006) is the Random Doping Fluctuations (RDF) in channel area. The problem is due to threshold voltage mismatch among different devices in single chip of same technology. Circuits using FinFET will provide better reduction in leakage current and short channel effects. In a research, Swahn and Hassoun (2006), it was estimated that in 70 nm CMOS technology the active mode leakage power is 40% of that of total power consumption. But the same is 62.56% in 45 nm technology. In FinFET, the front and back gate can be controlled independently which will improve performance and reduce power consumption (Muttreje *et al*., 2007; Khndelwal and Akashe, 2013) in their reseach investigated the different mode of FinFET. The parameters like leakage current delay and total power consumption were analyzed and from the analysis, it is found that the leakage power is 60% less in SVL based inverter than its conventional counterpart. Even though the reduction of leakage power is predominant few works

Corresponding Author: S. Saravanan, Department of Electrical and Electronics Engineering, Muthayammal Engineering College, Rasipuram, Tamil Nadu, India

(Ghai *et al*., 2013) have received attention on the design of circuits for analog systems using FinFET. Analog parameters like transconductance, output resistance and open circuit gain is analyzed. These works helped to understand the parameters and functionality of the FinFET. Lin *et al*. (2014) proposed a sub/near-threshold computing for ultra low power application. An improved analytical model is proposed to capture the variations of the drain current with respect to gate and drain voltage. In depth analysis were made for stack sizing of FinFET logic cells in sub/near threshold region using 32 nm predictive technology model. In the advantage of the multigate fin device for low standby power circuit is analyzed (Agortinelli *et al*., 2010). To study the effectiveness of transistor-stacking and back biasing investigation is done using ring oscillators and mirror full adders .The implementation of fast and energy efficient adaptive back biased circuits concludes the effectiveness of FinFET technology.

Optimization of leakage current and leakage power of FinFET: Scaling of conventional CMOS devices below 35nm will create short channel effects like V roll off and drain induced barrier lowering. The other issues are increasing leakage current, sub threshold leakage and gate direct funneling leakage and hot carrier effects. The gate leakage causes increased power consumption. Power consumption is given by for inverter:

$$P = ACV^2F+VI\,leak \quad (1)$$

The first term in Eq. 1 is the dynamic power (charging and discharging of C_L). Where of is the gate switching frequency, C-total C_L and A-fraction of gate switching. The second term is the standby due to leakage current the leakage current is given by:

$$I_{leak} = I_{sub} + I_{ox} \quad (2)$$

The first term dynamic power is reduced by FinFET device, since the charging and discharging of C_L takes place with higher magnitude when compared to CMOS as the leakage current is suppressed. Next the gate switching frequency.

A new device methodology for the carry propagation reduction adder is proposed for 32 nm FinFET technology occupying lesser area. The structure is an adopted version of an existing CMOS self timed adder. The main contributions is on designing FinFET based device and introducing SVL technique in a logic device.

MATERIALS AND METHODS

FinFET technology has recently seen a major increase in adoption for use within computational integrated circuits manufactured using advanced technologies like 65 and 45 nm. The FinFET technology promises to deliver superior levels of scalability needed to ensure that the current progress with increased levels of integration within integrated circuits can be maintained. The FinFET offers many advantages in terms of IC processing and has been adopted as a major way forwards for incorporation within IC technology. One such proposed design is this work where the circuit is adopted and implemented using FinFET.

Device structure of FinFET: The FinFET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed as shown in Fig. 1a and b by Choi *et al*. (2002). The device is formed on thin Silicon On Insulator (SOI) finger termed fin. On the top of the silicon fin nitride has been deposited on a thin pad oxide to protect the silicon fin during gate poly-SiGe etching. The FinFET transistors employ a single gate stacked on top of two vertical gates allowing for essentially three times the surface area for electrons to travel. Gate work-function tailoring is essential to adjust the threshold voltage. Therefore, for the gate material poly-SiGe has been chosen. The crucial geometric device dimensions are shown in Fig. 1a.

A single poly silicon layer is deposited over a fin. Here, fin itself acts as a channel and it terminates on both sides of source and drain. FinFET consists of two gates: front gate and back gate, source and drain. Front gate is used to control the channel conduction and back gate is used to control the threshold voltage. The labels in the figure stands for L_g: printed gate length, L_{eff}: effective gate length which is determined by the distance of the junctions, T_{fin}: Height of the fin, W_{fin}: Width of the fin which is the distance between the gate oxides of the two gates (Fig 1b).

The FinFETs are not available as discrete devices due to the problem in manufacturing similar GATE. However, FinFET technology is becoming more widespread as feature sizes within integrated circuits and there is a growing need to provide very much higher levels of integration with less power consumption within integrated circuits. The wide range of application includes low power design in digital circuit such as RAM because

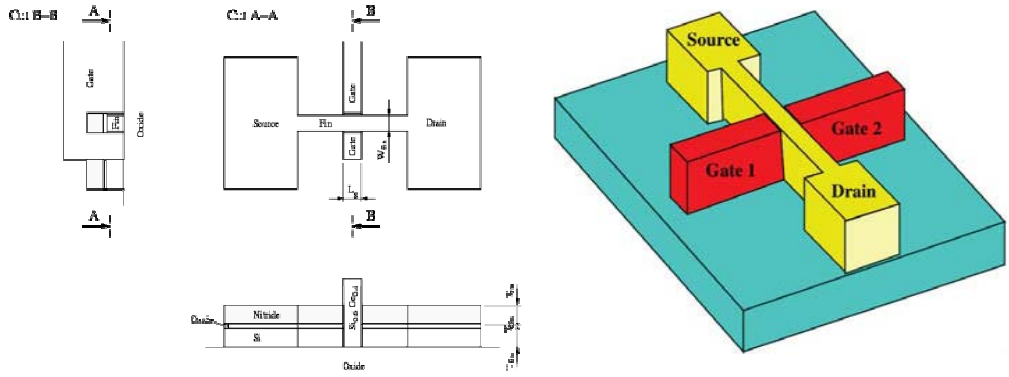

Fig. 1: a) Views of the FinFET layout; b) FinFET device structure

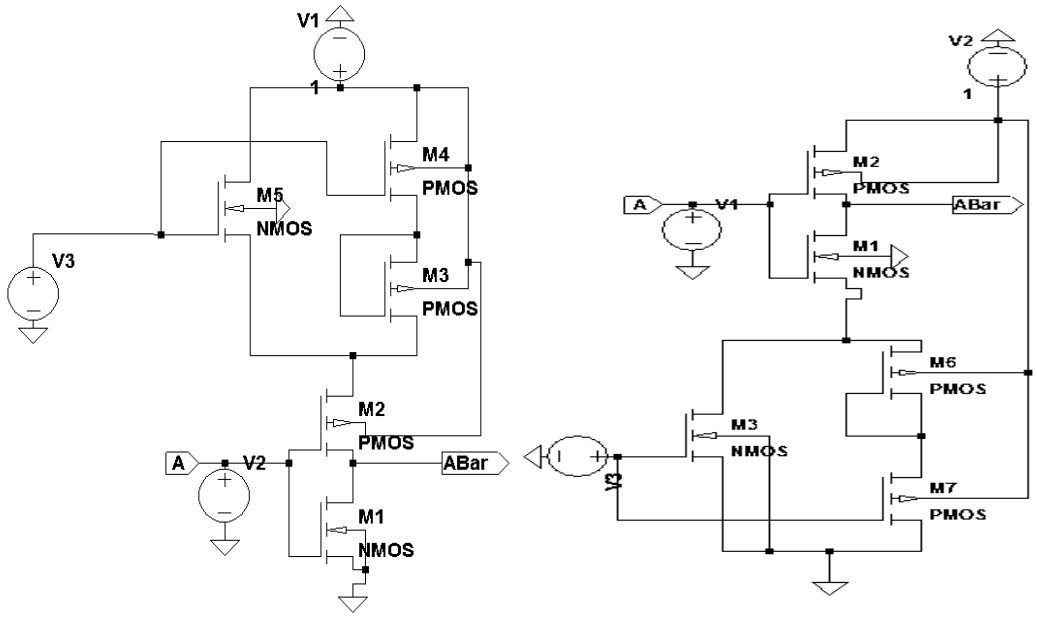

Fig. 2: a) Upper SVL circuit; b) lower SVL circuit

of its low off-state current. Power amplifier or other application in analog area which requires good linearity. The advantages of FinFET are much lower power consumption allows high integration levels. Early adopters (Choi *et al*., 2002) reported 150% improvements. FinFETs operate at a lower voltage as a result of their lower threshold voltage and possible to pass through the 20 nm barrier previously through as an end point.

SVL technique: The self controllable voltage level reduces leakage power and delay (Drazdziulis and Edefors, 2003; Pendey and Akashe, 2014). The leakage current is reduced by proposing a modified self-controllable voltage level for the adder controlled by clock, the method is classified into Upper SVL (USVL) and Lower SVL (LSVL). The Basic idea behind the working is the SVL will provide the maximum supply voltage V_{DD} during active mode and slightly lower supply voltage during standby mode. In addition to that the ground level voltage is slightly increased relatively during standby mode by which the sub threshold voltage and leakage power is reduced. The USVL circuit is shown in Fig. 2a.

USVL: The Upper SVL circuit is designed with a wide channel pull-up PMOS transistor working as a switch and connected parallel with multiple NMOS devices. The NMOS is connected in series. The NMOS devices work in linear region and forms series of resisters. The circuit sinks the power consumption but controls the leakage current. An input clock pulse is applied (Fig. 2b).

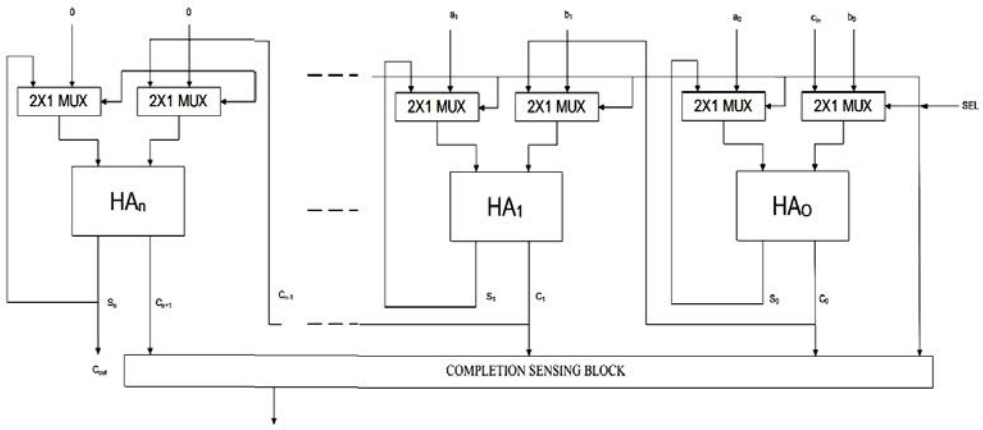

Fig. 3: Architecture of PASTA

LSVL: In Lower SVL the circuit is incarnated with one NMOS and multiple PMOS devices. Clock pulse is applied to the NMOS Circuit. The PMOS Circuit is connected in series and grounded.

The SVL is applied to the self timed adder circuit. When the load circuit is active, the PMOS switch in the Upper SVL and PMOS switch in the lower SVL are turned ON by the clock and inverted clock. The resister configuration of series PMOS and Series NMOS in LSVL and USVL are turned OFF. Now the maximum supply voltage V_{DD} to the pull up circuit and minimum ground-level V_{SS} to the pull down Circuit is provided by the USVL and LSVL respectively. This phenomenon increases the operating speed of the adder. When, the adder or load circuit is in standby mode all the NMOS and PMOS resister configured devices of SVL is turned ON and the PMOS and NMOS switch of SVL turned OFF.

The USVL circuit will generate a lower supply voltage and LSVL circuit will relatively generate a higher ground-level voltage. This will relatively increase the back gate bias voltage which will increase the reverse bias of cut off PMOS and NMOS device. The increase in back gate will reduce the leakage currents of the cut-off NMOS and PMOS devices of the load circuit. In addition, the V_{DS} voltage of the cut off MOSFET will decrease and effect of Drain Induced Barrier Lowering (DIBL) is reduced.

Parallel self timed adder: In literature, various arithmetic circuits (Moshgelani *et al*., 2013; Chin *et al*., 2015; Mishra and Akashe, 2015) like adders, multipliers and encoders are implemented using FinFET are presented. The carry propagation is one of the important issues which slow down the speed of multipliers and adders. Most of the delay occurs due to the carry propagation. The parallel self timed adder architecture (Rahman *et al*., 2015) accepts two operands as inputs and performs addition for each bit. Self timed adders work on the principle of timing assumptions or/and operation for the correct operation. The self timed adder is the asynchronous circuit which avoids the bundled delay phenomenon in synchronous circuit. The circuit is faster since it senses the early completion block so the bundled delay is reduced. In few adders (Cheng *et al*., 2000) an asynchronous request is used to initial the adder and the processor receives the acknowledge signal when the process is completed by validating the flow of carry signal. These adders uses carry-completion sensing unit with dual rail carry block.

The adder iterates the half addition using previously generated carry and sums until all carry bits are consumed and settled at zero level. The architecture of the self timed adder is shown in Fig. 3. The architecture consists of a two input multiplexer, half adder and a completion selection and detection unit.

The select line to the multiplexer is the handshaking signal of value 0-1 transition. Initially, the select line will be '0' to select the actual operand. During subsequent iterations the select line will be '1' based on the feedback or carry. The circuit works in two phases namely the initial phase and the iterative phase. During the initial phase, the circuit performs the addition operation and during the iterative phase the feedback path through multiplexer block is activated. The complete recursion process takes many carry transitions. Similarly, the operands and results go through several transitions for the final result. The speed of the adder is determined by the single-bit computation time. The adder terminates once all carries are zero.

Implementation A FinFET based NAND gate implementation for SVL, LSVL and USVL in shorted gate

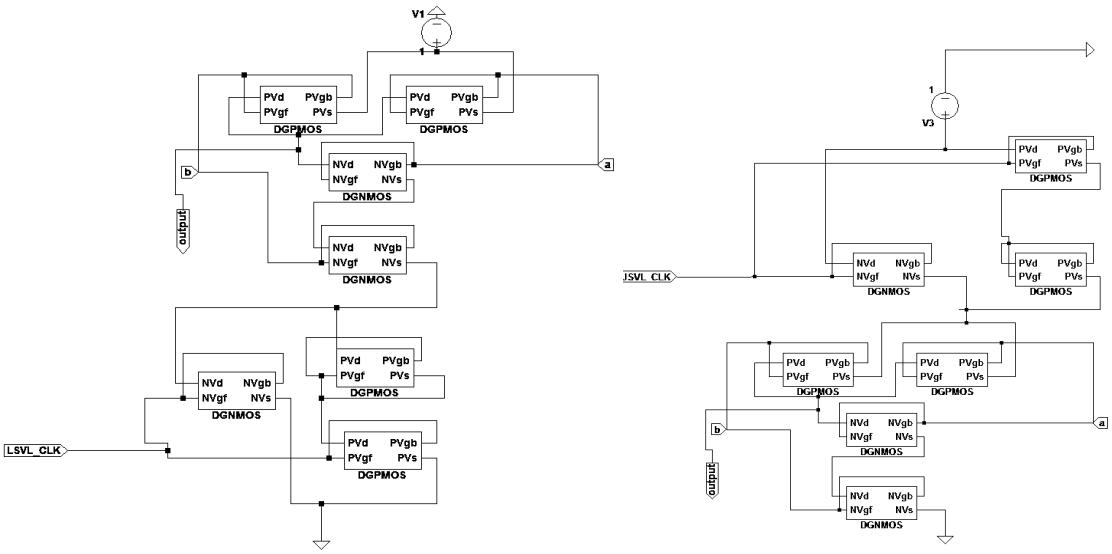

Fig. 4: a) FinFET SG LSVL NAND gate; b) FinFET SG USVL NAND gate

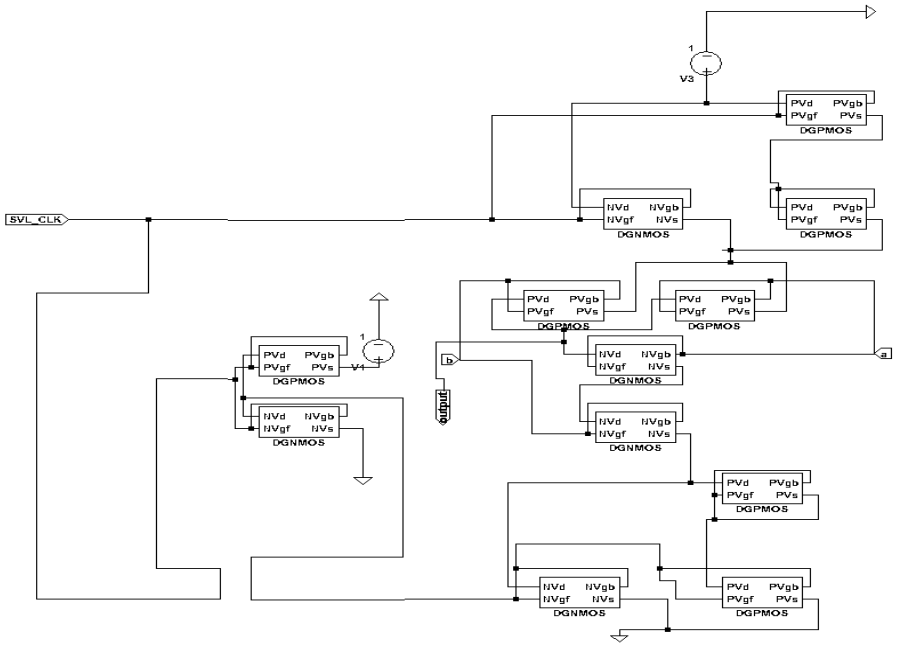

Fig. 5: FinFET SG SVL NAND gate

mode is shown in Fig. 4a and b. For the implementation predictive technology model for 32 nm used. The supply voltage is 1V, for CMOS implementation the predictive technology model for 32 nm is used. The number of transistors is same for both FinFET and CMOS circuits. The number of transistors is more in the SVL circuit but the power consumed is less. Figure 5 shows the FinFET shorted gate SVL NAND gate. The SVL circuit contains 12 transistors controlled by a SVL clock.

The implementation of the recursive parallel self timed adder circuit is shown in Fig. 6, for multiplexers and gates, we have used the predictive technology model file implementations. The half adder is designed using XOR and AND gate having 14 transistors and 6 transistors, respectively.

Figure 6a shows the FinFET based PASTA adder circuit diagram. 4-bit implementation is carried out to validate the performance with respect to carry propagation delay. In Fig. 6b and Fig. 7a and 7b shows the FinFET based PASTA adder circuit for LSVL, USVL and SVL schemes, respectively. Among this the SVL

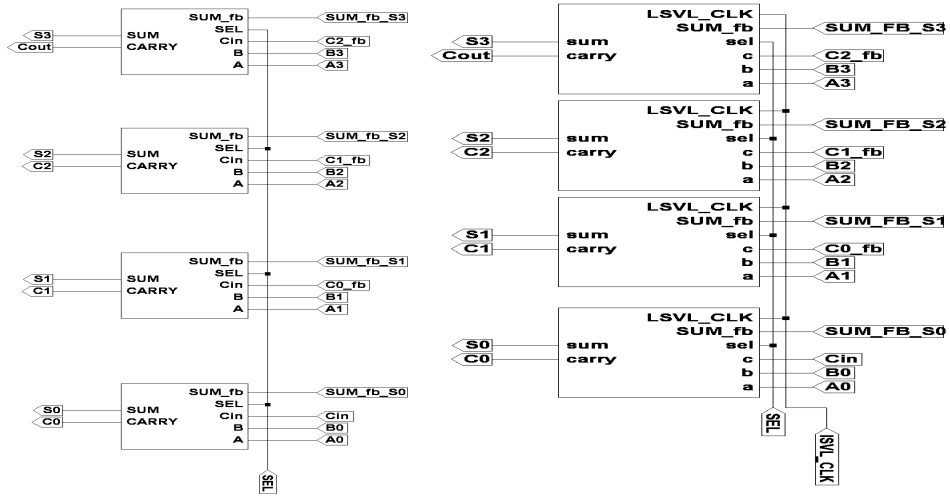

Fig. 6: a) FinFET PASTA adder; b) FinFET LSVL PASTA adder

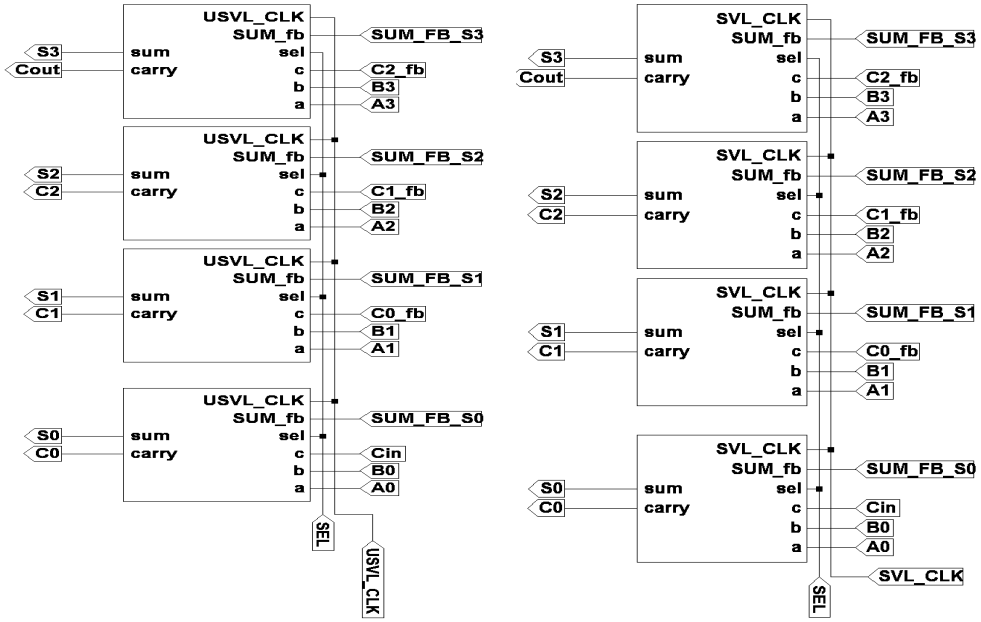

Fig. 7: a) FinFET USVL PASTA adder; b) FinFET USVL PASTA adder

based design contains more transistors. But as the approach is towards 32 nm the power is drastically reduced when compared to 90 nm technology.

RESULTS AND DISCUSSION

The power consumption of NAND logic gates implementation using CMOS and FinFET is shown in the Table 1. The results show that the power dissipation in FinFET is lesser in the order of 3 compared to CMOS. The SVL, LSVL and USVL circuit outputs are also compared. The average power consumption of different device adders for different circuits (SVL) are shown in Table 2. The FinFET dominates and outperforms the CMOS in its consumption of power.

The measure of average power consumed is measured for a 4 bit adder in 32nm technology even though the existing adders in literature show decreasing average power consumption as the process length is decreased, the proposed FinFET based self timed adder consumes least power among the self-timed adders. The power consumption is reduced by nearly 20% when compared to the CMOS design.

Table 1: Power analysis for NAND gate

	NAND GATE implementation (Power consumption)			
Device	Conventional	LSVL	USVL	SVL
CMOS	4.16677 23 µW	7.77681 µW	4.05663 µW	0.70152 µW
FinFET	12.1142 pW	1.13552 pW	1.50559 pW	3.25589 pW

Table 2: Power analysis for parallel self timed adder

	Parallel self timed adder (PASTA) (Power in watts)			
Device	Conventional	LSVL	USVL	SVL
CMOS	265.78 µW	98.4491 nw	61.3975 nW	183.384 nW
FinFET	6.17417 µW	76.466 nW	65.792 nW	136.407 nW

Table 3: Power analysis for parallel self timed adder

VDD in volts	CMOS PASTA adder	FinFET PASTA adder
	Leakage power	Leakage power
0.25	9.39127 µW	0.17922 µW
0.3	9.47427 µW	0.24336 µW
0.35	12.5946 µW	0.49930 µW
0.4	16.3919 µW	0.54776 µW
0.45	21.0592 µW	0.58017 µW
0.55	38.5943 µW	0.91457 µW
0.6	47.5451 µW	1.12054 µW
0.65	58.1696 µW	1.96630 µW
0.75	91.4178 µW	2.75398 µW
0.8	114.993 µW	3.54129 µW
0.85	144.808 µW	4.12273 µW
0.9	184.675 µW	4.76721 µW
0.95	230.094 µW	5.41572 µW
1	265.078 µW	6.17417 µW

The circuit is further analyzed by executing the circuit using different supply voltage and the leakage power is observed. Table 3 shows the performance of CMOS and FinFET based self timed adder for various supply voltage. The leakage power is very much reduced in the FinFET design making it more efficient.

CONCLUSION

In this research a FinFET based self timed adder is proposed. The proposed architecture reduces the carry propagation time and power consumption. The reduction in power is achieved using FinFET which intuitively reduces the leakage current. The work is carried out in 32 nm technology using synopsis HSPICE. The performance is enhanced using the SVL technique. The experiments were carried out using SPICE models. The analysis and performance of FinFET based inverter with and without SVL is observed. The work is extended for a 2 input NAND gate to observe the performance for a logic gate. From the observation it is found that the FinFET based NAND gate performance is 97% better when compared to a conventional CMOS logic. The power consumption is in the range of few picowatts when CMOS logic utilized in the microwatt range. So, a power improvement is achieved. The experimental results show that the LSVL performance is comparatively good with other methods. The work is further extended to the design of an adder using FinFET. Finally the FinFET outperforms the performance of a CMOS adder.

REFERENCES

Agostinelli, M., M. Alioto, D. Esseni and L. Selmi, 2010. Leakage-delay tradeoff in FinFET logic circuits: A comparative analysis with bulk technology. Very Large Scale Integrat. Syst. IEEE. Trans., 18: 232-245.

Cheng, F.C., S.H. Unger and M. Theobald, 2000. Self-timed carry-lookahead adders. Comput. IEEE. Trans., 49: 659-672.

Chin, H.C., C.S. Lim and M.L.P. Tan, 2015. Design and performance analysis of 1-bit FinFET full adder cells for subthreshold region at 16 nm process technology. J. Nanomaterials, Vol. 16,

Choi, Y.K., T.J. King and C. Hu, 2002. Nanoscale CMOS spacer FinFET for the terabit era. Electron Device Lett. IEEE., 23: 25-27.

Drazdziulis, M. and L.P. Edefors, 2003. A gate leakage reduction strategy for future CMOS circuits. Proceedings of the 29th European Conference on Solid-State Circuits, September 16-18, 2003, IEEE, Estoril, Portugal, ISBN: 0-7803-7995-0, pp: 317-320.

Ghai, D., S.P. Mohanty and G. Thakral, 2013. Comparative analysis of double gate FinFET configurations for analog circuit design. Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS), August 4-7, 2013, IEEE, Columbus, Ohio, pp: 809-812.

Gupta, S.K. and K. Roy, 2013. Device-circuit co-optimization for robust design of finFET-based SRAMs. Des. Test IEEE., 30: 29-39.

Khandelwal, S. and S. Akashe, 2013. Design of a FinFET based inverter using MTCMOS and SVL leakage reduction technique. Proceedings of the IEEE Students Conference on Engineering and Systems (SCES), April 12-14, 2013, IEEE, Allahabad, India, ISBN: 978-1-4673-5628-2, pp: 1-6.

Lin, X., Y. Wang and M. Pedram, 2014. Stack sizing analysis and optimization for FinFET logic cells and circuits operating in the sub/near-threshold regime. Proceedings of the 15th IEEE International Symposium on Quality Electronic Design, March 3-5, 2014, IEEE, Santa Clara, California, ISBN: 978-1-4799-3945-9, pp: 341-348.

Mishra, P., A. Muttreja and N.K. Jha, 2011. FinFET Circuit Design. In: Nanoelectronic Circuit Design. Niraj, K., J.D. Chen (Eds.). Springer, New York, USA., ISBN: 978-1-4419-7444-0, pp: 23-54.

Mishra, V. and S. Akashe, 2015. Calculation of Power Delay Product and Energy Delay Product in 4-Bit FinFET Based Priority Encoder. In: Advances in Optical Science and Engineering. Lakshminarayanan, V., I. Bhattacharya (Eds.). Springer New Delhi, India, ISBN: 978-81-322-2366-5, pp: 283-289.

Moshgelani, F., D. Al-Khalili and C. Rozon, 2013. Ultra-low leakage arithmetic circuits using symmetric and asymmetric finFETs. J. Electr. Comput. Eng., Vol. 2013.

Muttreja, A., N. Agarwal and N.K. Jha, 2007. CMOS logic design with independent-gate FinFETs. Proceedings of the 25th International Conference on Computer Design ICCD, October 7-10, 2007, IEEE, Chico, California, USA., ISBN: 978-1-4244-1257-0, pp: 560-567.

Pandey, V. and S. Akashe, 2014. Design techniques for self voltage controllable circuit on 2: 1 multiplexer using 45 nm technology. Intl. J. Comput. Appl., 89: 1-18.

Rahman, M.Z., L. Kleeman and M.A. Habib, 2015. Recursive approach to the design of a parallel self-timed adder. Very Large Scale Integr. Syst. IEEE. Trans., 23: 213-217.

Swahn, B. and S. Hassoun, 2006. Gate sizing: FinFETs vs 32nm bulk MOSFETs. Proceedings of the 43rd Annual Conference on Design Automation, July 24-28, 2006, San Francisco, California, ISBN: 1-59593-381-6, pp: 528-531.