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# Sliding Mode Control for Voltage Regulation in Positive Output Elementary Parallel Connected Boost Converter

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**Abstract:** The necessity of higher current and providing a back-up when one unit fail, demands the parallel operation of dc-dc converters. One of the problems of the parallel operating power converters is to regulate the output voltage and equalize the output currents of modules. This study provides the design of sliding mode controller (SMC) for parallel operated DC-DC boost converter. The output voltage regulation and load sharing behaviors are studied for the designed SMC for disturbances viz. line voltage variations of converters, load variation and other circuit components changes. The performance evaluation is done in hardware and MATLAB-Simulink tool finally the results are compared with conventional proportional-integral (PI) controller.

**Key words:** Parallel Connected Boost Converter, Sliding Mode Controller, PI Controller, Voltage Regulation

## INTRODUCTION

DC-DC step-up converters are widely used in computer hardware and industrial applications such as computer peripheral power supplies, car auxiliary power supplies, servo-motors drives and medical equipment (Peter, 1979; Wang *et al*., 1994). In recent years, the DC-DC conversion technique has been greatly developed. The main objective is to reach a high efficiency, high power density and cheap topology in a simple structure. Generally in power supply applications DC-DC converter modules are operated in parallel due to the reasons like higher power demand, improving the power system reliability and the operational redundancy (N+1 redundancy-N is the number of units needed to power the load, plus 1 as the back-up) (Rajagopalan *et al*., 1996). There is also a trend in manufacturing the standard power converter modules which can be connected in parallel to cover a wide power range. This significantly reduces the costs of development and existing systems can be extended easily. The parallel operation offers the advantages such as expandability of output power, reliability and ease of maintenance. The main challenges in the parallel operations are output voltage regulation and load current sharing at different disturbances.

The average generalized PI output feedback regulator as a steer for defining the switched implementation of the average sliding mode features through a sigma-delta modulation strategy has been addressed by Ramirez *et al*. (2013). The control loop of a parallel connection of two nonidentical paralleled positive output elementary super lift luo converters using the SMC theory for current distribution control in continuous conduction mode Kumar and Jeevananthan (2011). A droop method has been proposed for the converter parallel operation, which adaptively controls the reference voltage of each module. The scheme improves the output voltage regulation and the current sharing of the conventional droop method (Kim *et al*., 2002). A robust controller for parallel dc dc buck converters has been coined by combining the concepts of integral-variable-structure and multiple-sliding-surface control Mazumder *et al*. (2002). Grid connected solar PV system with SEPIC converter compared with parallel boost converter based MPPT (Raj *et al*., 2014). Nonlinear back-stepping adaptive controller has been proposed for the design of parallel DC-DC buck converters with uncertainties of load and power disturbance. The relationship between the control elements and circuit parameters has been determined by simulation analysis. The relationship between current sharing difference and circulating current for two parallel connected dc-dc converters has been investigated Augustine *et al*. (2013). Although, there may exist a trade-off between current sharing difference and voltage regulation, the proposed droop index algorithm gives better performance and low voltage regulation. The

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detailed analysis and design procedure are explained for two DC-DC boost converters connected in parallel. The effectiveness of proposed method is verified using MATLAB simulation.

The uncertainties in the source, load and other circuit parameters make the parallel operation of DC-DC converters hallenging. This study provides the design of Sliding Mode Controller (SMC) for parallel operated DC-DC boost converter. The output voltage regulation and load sharing behaviours are studied for the designed SMC for disturbances viz. line voltage variations of converters, load variation and other circuit components' changes. The performance of the developed controller in parallel boost converter is validated at the different working conditions through the simulation in the comparison with PI controller.

## MATERIALS AND METHODS

**Principle of operation and SMC:** Variable Structure Control (VSC) with sliding mode or Sliding-Mode Control (SMC) is one of the effective nonlinear robust control approaches since it provides system dynamics with an invariance property to uncertainties once the system dynamics are controlled in the sliding mode (Decarlo *et al*., 1988). For the non-linear system like positive output elementary cascade boost converter, the sliding mode controller is a more suitable approach. Sliding mode control has been presented as a good alternative to the control of switching power converters (He *et al*., 2010). The main advantage over the classical control schemes is its insusceptibility to plant parameter variations that leads to invariant dynamics and steady-state response in the ideal case. In this paper, a sliding mode controller for the positive output elementary cascade boost converter is proposed.

**System description:** The Positive Output Elementary Parallel Connected Boost Converter (POEPCBC) is shown in Fig. 1. It includes dc supply voltage $V_{in}$, capacitor C, input inductor L, power switch (n-channel) S, freewheeling diode D, load resistance R. The principle of the sliding mode controller is to make the capacitor voltage $V_C$ follows as faithfully as possible a capacitor voltage reference.

In the description of the converter operation, it is assumed that all the components are ideal and that the proposed converter operates in a continuous conduction mode. Fig. 2 shows equivalent circuit while Fig. 3 and Fig. 4 represent two topological modes for a one cycle period of operation. When the switch S is closed in Fig. 3, inductor current iL rises quite linearly, diode current D is reverse polarized and capacitor C supplies the energy to

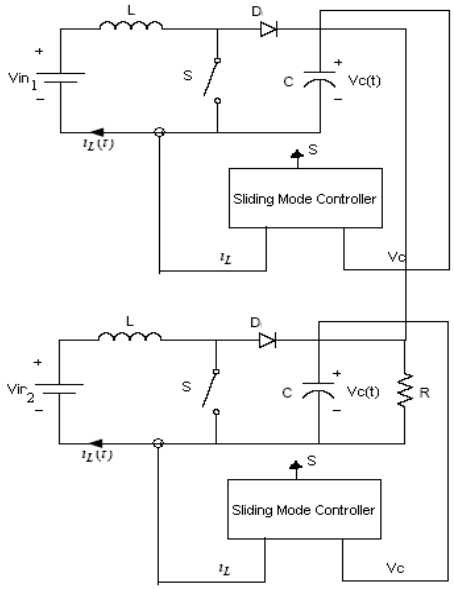



Fig. 1: The positive output elementary parallel connected boost converter controlled by sliding mode.

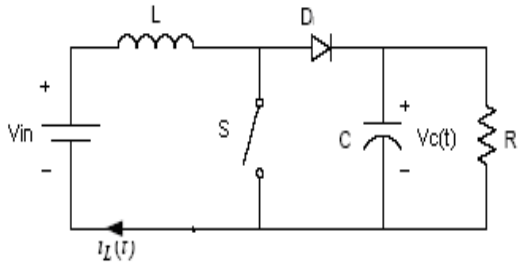



Fig.2: Equivalent circuit for the positive output elementary cascade boost converter.

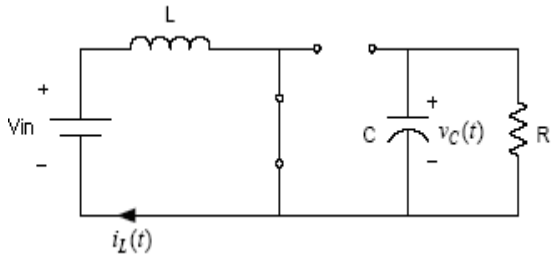
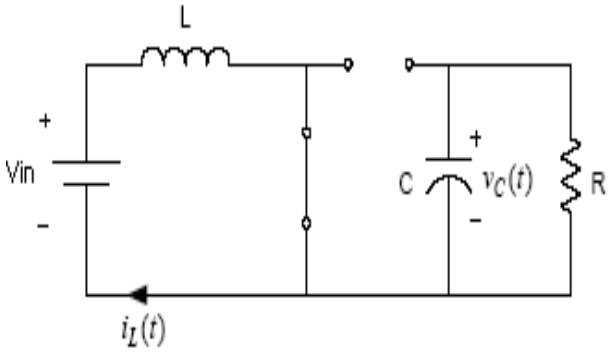



Fig. 3: Mode 1 operation

output stage. Once the switch S is open in Fig. 4, inductor current iL is forced to flow through the diode D, capacitor C and load. The current $i_L$ decrease while capacitor is recharged. The ripple inductor current is:

$$\Delta i_L = \frac{V_{in}}{L} dT = \frac{V_o - V_{in}}{L}(1-d)T \quad (1)$$




Voltage transfer gain:

$$G = \frac{V_o}{V_{in}} = \frac{1}{1-d}$$
$$G = \frac{V_o}{V_{in}} = \frac{1}{1-d} \quad (2)$$

Inductor average current:

$$I_L = (1-d)\frac{V_o}{R} \quad (3)$$

The state-space modelling of the equivalent circuit with state variables iL and VC is given by:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} -\frac{V_C}{L} \\ 0 \end{bmatrix} ? + \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix} \quad (4)$$

$v = Av+B\gamma+C$

Where:

$\gamma$ = The status of the switches,
v and v = Are the vectors of the state variables
$(i_L, V_C)$ = The derivatives, respectively

$$\upsilon = \begin{cases} 1 \rightarrow S \rightarrow ON \\ 0 \rightarrow S \rightarrow OFF \end{cases} \quad (5)$$

**Sliding mode controller:** When good transient response of the output voltage is needed, a sliding surface equation in the state space, expressed by a linear combination of state-variable errors $\varepsilon_1$ (defined by difference to the references variables), can be given by:

$$S = (i_L, V_C) = K_1\varepsilon_1 + K_2\varepsilon_2 \quad (6)$$

Where coefficients $K_1$ and $K_2$ are proper gains, $\varepsilon_1$ is the feedback current error and $\varepsilon_2$ is the feedback voltage error,

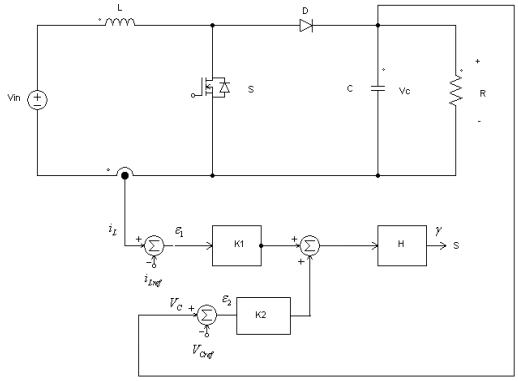



Fig. 5: Sliding mode controller scheme.

Or;

$$\varepsilon_1 = i_{L1} - i_{Lref} \quad (7)$$

$$\varepsilon_2 = V_C - V_{Cref} \quad (8)$$

By substituting Eq. 7 and Eq. 8 in Eq. 6, one obtains:

$$S = (i_L, V_C) = K_1(i_L - i_{Lref}) + K_2(V_C - V_{Cref}) \quad (9)$$

The signal $S(i_L,V_C)$, obtained by the implementation of Eq. 9 and applied to a simple circuit (hysteresis comparator), can generate the pulses to supply the power semiconductor drives. The resulting control scheme is shown in Fig. 5. Status of the switch $\gamma$ is controlled by hysteresis block H which maintains the variables S $(i_L,V_C)$ near zero. The system response is determined by the circuit parameters and coefficients $K_1$ and $K_2$. With a proper selection of these coefficients in any operating condition, high control robustness, stability and fast response can be achieved.

In theory, the sliding mode control requires sensing of all state variables and generation of suitable references for each of them. However, the inductor current reference is difficult to evaluate since that generally depends on load power demand supply voltage and load voltage. To overcome this problem, in implementation the state variable error for the inductor current ($i_{L1}$-$iL_{ref}$) can be obtained from feedback variable $i_{L1}$ by means of a high-pass filter in the assumption that their low-frequency component is automatically adapted to actual converter operation. Thus, only the high-frequency component of this variable is needed for the control. This high pass filter increases the system order and can heavily alter the converter dynamics. In order to avoid this problem, the cut-off frequency of the high-pass filter must be suitably lower than the switching frequency to pass the ripple at the switching frequency but high enough to allow a fast converter response.

**Design calculation:** In the design of the controller, Ideal power switches; Power supply free of dc ripple and converter operating at high-switching frequency are assumed. The controller design describe the selection of controller parameters, switching frequency, duty cycle, inductor current, voltage capacitor by Caceres and Barbi (1999). The main purpose of this section is to use to calculate the proposed converter components value, controller parameters and simulation studies. The validation of the system performance is done for three regions viz. line variation, load variation and components variations. Simulations have been performed on the POEPCBC circuit with parameters listed in Table 1.

The performance of proposed method is evaluated using Matlab/Simulink. The signal $S(i_L,V_C)$, obtained by the simulation implementation of (9) and applied to a simple circuit (hysteresis comparator), can generate the pulses to supply the power semiconductor drives. Status of the switch γ is controlled by hysteresis block H which maintains the variables $S(i_L,V_C)$ near zero.

**Design of PI controller:** A PI controller is chosen for providing the better output voltage regulation in POEPCBC. The DC output voltage is sensed and compared with reference output voltage and error signal is obtained. This error signal is processed by the PI controller to maintain the output voltage constant. The PI parameters, Proportional gain ($K_p$) and Integral times ($T_i$) are obtained by using Zeigler-Nichols tuning method. The Transfer Function (TF) model of equation is obtained from the state space average model of the following equation using MATLAB, then:

$$TF = \frac{-7.958e^{-12}s^2 + 1.667e^8 s + 1.389e^{12}}{s^3 + 666.7s^2 + 8.333e^7 s} \quad (10)$$

For simplifying the design aspect, the term $-7.958e^{-12}s^2$ in the numerator of the TF model is very small and hence, it can be neglected. Therefore, the new TF becomes:

Table 1: Parameters of chosen POEPCBC

| Parameters name | Value |
|---|---|
| Input Voltage ($V_{in}$) | 12V |
| Output Voltage ($V_o$ =$V_C$) | 36V |
| Inductor (L) | 100 µH |
| Capacitor © | 30 µF |
| Nominal Switching Frequency (Fs) | 100 kHz |
| Determination the Ratio $K_1$/L | 7453 |
| Determination the Ratio $K_2$/C | 248433 |
| Co-efficient $K_1$ | 0.745 |
| Co-efficient $K_2$ | 7.45 |
| Load Resistance (R) | 50 |
| Output Power ($P_o$) | 25.92 W |
| Input Power ($P_{in}$) | 27.684 W |
| Input Current ($I_{in}$) | 2.307 A |
| Efficiency η | 93.62 % |

$$TF = \frac{1.667e^8 s + 1.389e^{12}}{s^3 + 666.7s^2 + 8.333e^7 s} \quad (11)$$

The characteristic equation with proportional control is expressed by:

$$s^3 + 666.7s^2 + s(8.333e^7 + K*1.667e^8) + K*1.389e^{12} = 0 \quad (12)$$

The Routh-array of above equation is:

$$s_3 : 8.333e^7 + K*1.667e^8$$
$$s_2 : K*1.389e^{12}$$
$$s_1 : 8.333e^7 + 2247116969*K$$
$$s_0 : K*1.389e^{12}$$

from this Routh-array technique, the range of K for stability is $(-8.333e^7 + 2247116969*k) > 0, k > 0.037$. $<k<0.037$ So, the ultimate critical gain $K_{cr}$=0.037 and their corresponding $\omega_n$ = 210447 rad/sec and $P_{cr}$=2* = pi$\omega_n$ $2.9856e^{-5}$. After turning the controller using this method, the POEPCBC is providing a sustained oscillation with ultimate gain for stability and can be found by $K_{cr}$ = 0.02 and their corresponding ultimate period $P_{cr}$ = 0.0012s. Using this method the value of $K_p$=$K_{cr}$/2=0.01205 and integral time $T_i$=$P_{cr}$/.2=0.0133s are determined.

## RESULTS AND DISCUSSION

The main purpose of this section is to discuss the simulation studies of the POEPCBC with SMC. Here the PI controller is used for comparison with the designed controller. The validation of the system performance is done for different conditions viz. the start-up transient, line variation, steady state and component variations. Simulations are performed on the POEPCBC circuits with the specifications are listed in Table I. Fig. 6 and 7 shows the average output currents and the gate pulse of paralleled modules without a controller for different input voltages ($V_{in1}$=12V and $V_{in2}$=15V). It can be seen that the

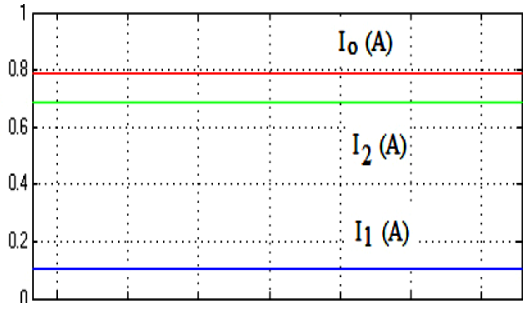



Fig. 6: Average output currents without a controller

Table 2: Performance of POEPCBC without controllers

| Change in $V_{in1}$ AND $V_{in2}$ (V) | $V_{01}$ (V) | $V_{02}$ (V) | $V_O$ (V) | $I_1$ (A) | $I_2$ (A) | $I_O$ (A) |
|---|---|---|---|---|---|---|
| 9 V -12 V | 33.92 | 33.92 | 33.92 | 0.040 | 0.645 | 0.685 |
| 12 V-15 V | 47.04 | 47.04 | 47.04 | 0.063 | 0.802 | 0.865 |
| Resistance (Ω) | $V_{01}$ (V) | $V_{02}$ (V) | $V_O$ (V) | $I_1$ (A) | $I_2$ (A) | $I_O$ (A) |
| 40 Ω | 34.42 | 34.42 | 34.42 | 2.414 | 1.041 | 3.455 |
| 50 Ω | 36.85 | 36.85 | 36.85 | 0.308 | 0.428 | 0.736 |
| 60 Ω | 36.92 | 36.92 | 36.92 | 0.315 | 0.300 | 0.615 |

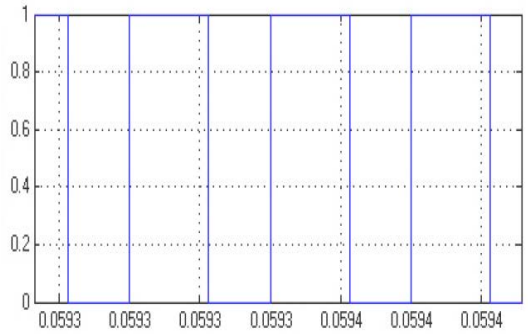



Fig. 7: Gate pulse of paralleled modules without a controller

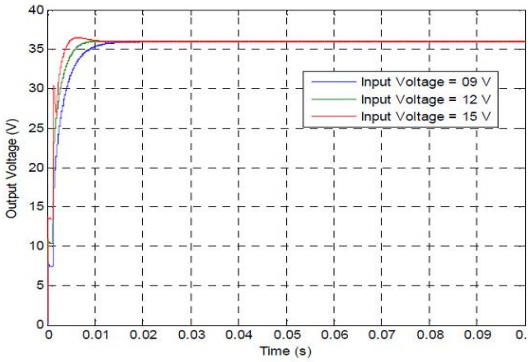



Fig. 9: Response at start-up for average output current of POEPCBC 1

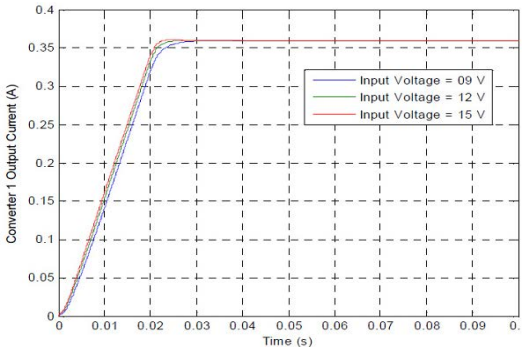



Fig. 8: Response at start-up for average output voltage of POEPCBC

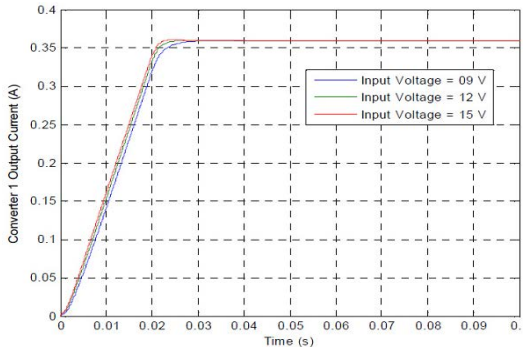



Fig. 10: Response at start-up for average output current of POEPCBC 2

current share of the modules are unequal. Table 2 lists the simulated results of the average output current/voltage for each of the modules and the POEPCBC without controllers for various input voltages and load resistances. From Table 2, it can be clearly seen that the output voltage regulation and the output current distributions of each of the modules and the POEPCBC are unequal.

**Start-up transients:** Figure 8 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different input voltages viz. 9V, 12V and 15V. It can be seen that the output voltage of the paralleled modules has a little overshoot and a settling time of 0.008s for $V_{in}$=15V whereas for 12V and 9V there are negligible overshoots and a settling time of 0.01s and 0.012s for designed SMC, respectively. Fig. 9 shows the dynamic behavior at start-up for the output voltage of paralleled module-1 for different input voltages viz. 9V, 12V and 15V. It can be seen that the output voltage of the paralleled modules has a little overshoot and a settling time of 0.022s for $V_{in}$=15V whereas for 12V and 9V there are negligible overshoots and a settling time of 0.025s and 0.028s respectively.

Figure 10 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different input voltages viz. 9V, 12V and 15V. It can be seen that the output voltage of the paralleled module-2 has a little overshoot and a settling time of 0.022s for $V_{in}$ = 15V whereas for 12V and 9V there are negligible overshoots and a settling time of 0.025s and 0.028s respectively. The overshoot behavior imitates the conclusions of the previous cases. Figure 11 shows the dynamic behavior at

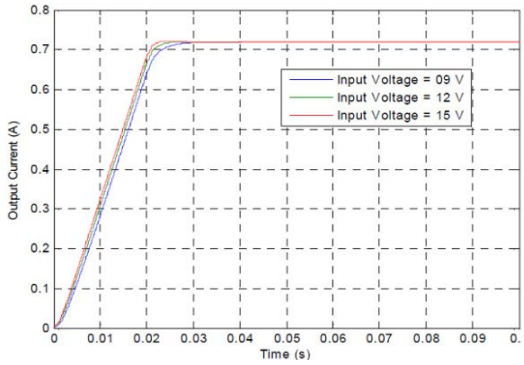



Fig. 11: Response at start-up for average output current of POEPCBC

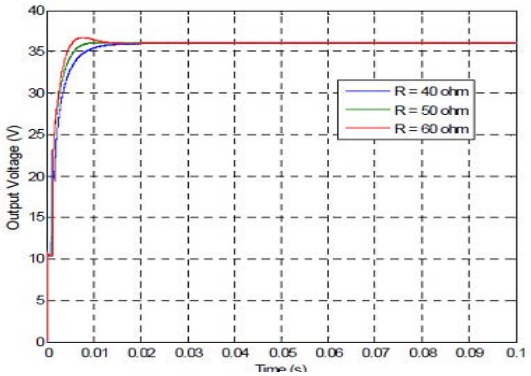



Fig. 12: Response at start-up for output voltage of paralleled modules

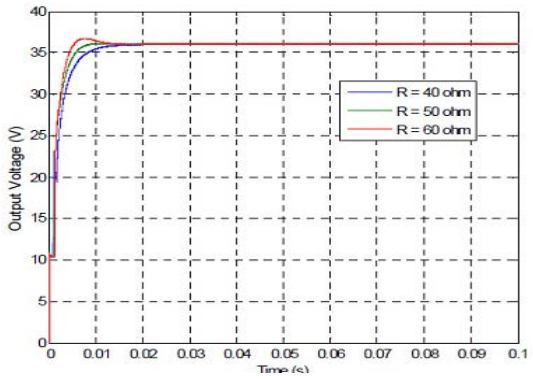



Fig. 13: Response at start-up for average output current of POEPCBC 1

start-up for the average output current of paralleled modules. Fig. 12 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different load resistances like 40, 50 and 60Ω. It can be seen that the output voltage of the paralleled modules has a slight overshoot and settling time of 0.012s for R = 60Ω, whereas the output voltage of the paralleled modules for R = 50Ω and R = 40Ω has a negligible overshoot and settling times of 0.013s and 0.014s with the designed SMC. Fig. 13

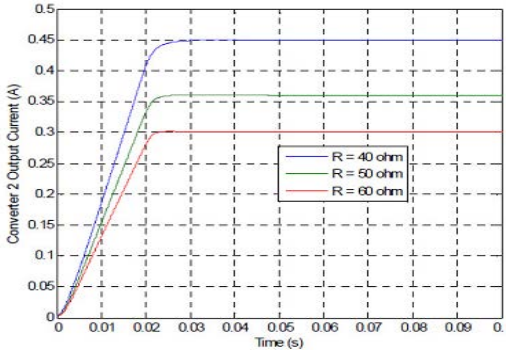



Fig. 14: Response at start-up for average output current of POEPCBC- 2

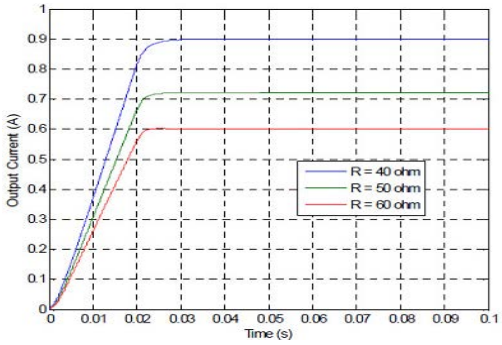



Fig. 15: Response at start up for average output current of POEPCBC

shows the dynamic behavior at start-up for the average output current of paralleled module-1 for different load resistances like 40Ω, 50Ω and 60Ω. It can be seen that the output voltage of the paralleled module-1 for R = 40Ω, R = 50Ω and R = 60Ω has a negligible overshoot and settling times of 0.03s, 0.025s and 0.021s with the designed controller.

Figure 14 shows the dynamic behavior at start-up for the average output current of paralleled module-2 for different load resistances like 40Ω, 50Ω and 60Ω. It can be seen that the output current of the module-2 for R = 40Ω, R = 50Ω and R = 60Ω has a negligible overshoot and settling times of 0.03s, 0.025s and 0.021s with the designed SMC. Figure 15 shows the dynamic behavior at start-up for the average output current of paralleled module-2 for different load resistances like 40Ω, 50Ω and 60Ω. It can be seen that the output current of the modules for R = 40Ω, R = 50Ω and R = 60Ω has a negligible overshoot and settling times of 0.03s, 0.025 and 0.021s with the designed SMC.

Table 3 lists the simulated results of the average output current and voltage of each of the modules and the

Table 3: Voltage/current profiles of POEPCBC for input voltages/load resistances with nominal input voltage/load in start-up region

| Parameters | Voltage profile | | | | | |
|---|---|---|---|---|---|---|
| Line Variation 9V - 15V(Start-up region) | PI Controller | | | SMC | | |
| | $V_{o1}$ (V) | $V_{o2}$ (V) | $V_O$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $V_O$ (V) |
| | 36.05 | 36.05 | 36.05 | 36 | 36 | 36 |
| Load Variation 40Ω-60Ω(Start-up region) | Current Profile | | | | | |
| | PI Controller | | | SMC | | |
| | I1 (A) | I2 (A) | IO (A) | I1 (A) | I2 (A) | IO (A) |
| 40 Ω | 0.441 | 0.441 | 0.882 | 0.45 | 0.45 | 0.90 |
| 50 Ω | 0.358 | 0.358 | 0.716 | 0.36 | 0.36 | 0.72 |
| 60 Ω | 0.291 | 0.291 | 0.582 | 0.3 | 0.3 | 0.6 |

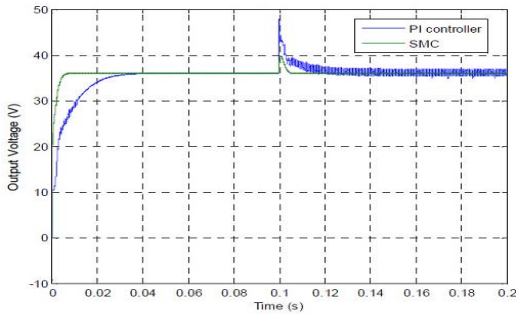



Fig. 16: Response of output voltage of paralleled modules (12V to 15V)

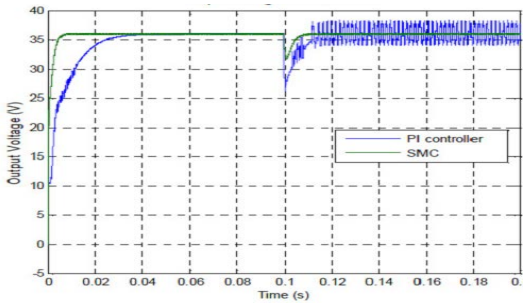



Fig. 17: Response of output voltage of paralleled modules (12-9V)

POEPCBC with controllers for various input voltage and load resistances in the start-up region. From Table 3, it can be seen that the voltage regulation and the current distributions of each of the modules and the POEPCBC using the designed SMC show excellent performance in comparison with a conventional PI controller.

**Line variations:** Figure 16 shows the response of the average output voltage of paralleled modules using both a PI controller and SMC for an input voltage step change from 12V to 15V (+30% line variations) at time = 0.1s. It can be seen that the output voltage of the paralleled modules using SMC has a maximum overshoot of 3.8 V and a settling time of 0.01s, while the output voltage of the paralleled modules using a PI controller has a severely affected overshoot of 12V and a long settling time of 0.02s respectively. Fig. 17 shows the response of the average output voltage of the SMC with paralleled modules using both a PI controller and SMC for an input voltage step change from 12V-9V (-30% line variations) at time = 0.1s. It can be seen that the output voltage of the paralleled modules using the SMC has a maximum overshoot of 4V and a settling time of 0.01s, while the output voltage of the paralleled modules using a PI controller has a maximum overshoot of 10V and a long settling time of 0.02s respectively.

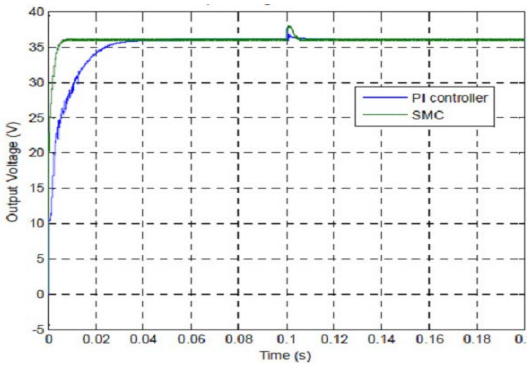



Fig. 18: Response of output voltage of paralleled modules (50 and 60Ω)

**Load variations:** Figure 18 shows the response of the output voltage of paralleled modules using both a PI controller and SMC for load step change from 50Ω to 60Ω (+20% load variations) at time = 0.1s. Here the output voltage of the paralleled modules using SMC has a small overshoot of 1.8V with a settling time of 0.01s, while the output voltage of the paralleled modules using PI controller has a severely affected overshoot of 16V and a settling time of 0.02s respectively. Fig. 19 shows the response of the output voltage of paralleled modules

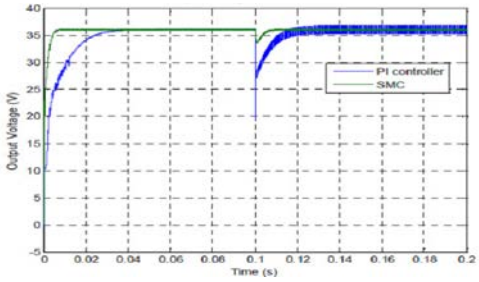



Fig. 19: Response of output voltage of paralleled modules (50? and 40?)

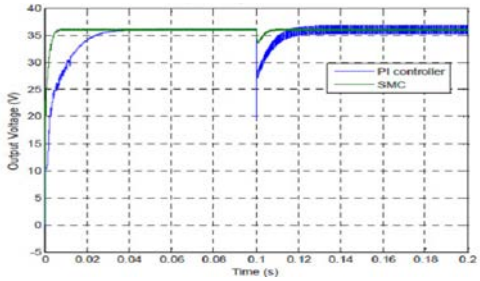



Fig. 20: Inductor current iL1 and output voltage in steady state region using SMC

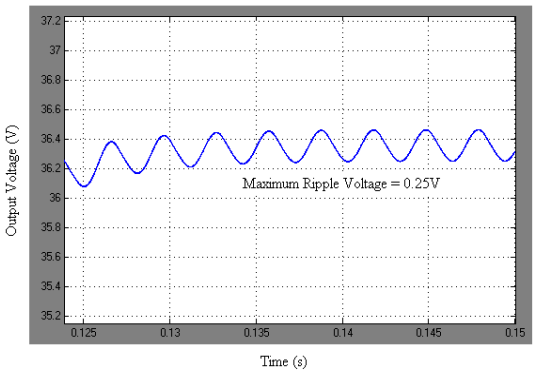



Fig. 21: Output voltage in steady state region using PI controller

using both a PI controller and SMC for load step change from 50Ω-40Ω (-20% load variations) at time = 0.1s.

**Steady state regions:** Figure 20 shows the instantaneous output voltage and the inductor current of paralleled modules in the steady state using SMC. It is evident from this figure that the output voltage ripple is very small, about 0.03V and the peak to peak inductor ripple current is 0.32A for an average switching frequency that is 100kHz closer to the theoretical designed. Figure 21 shows the instantaneous output voltage of paralleled

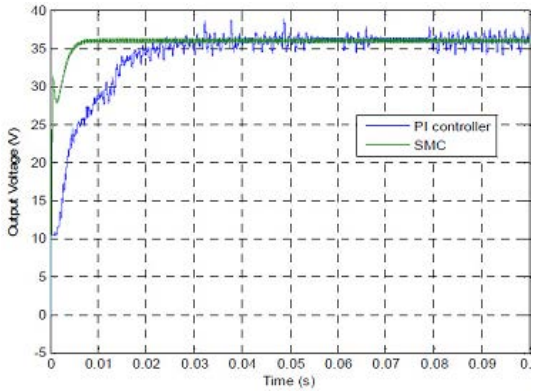



Fig. 22: Performance of POEPCBC output voltage (100µH to 500µH)

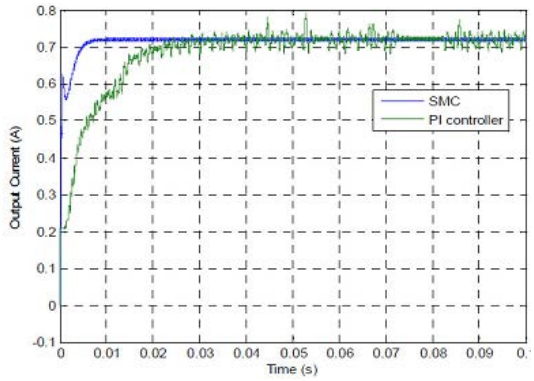



Fig. 23: Performance of POEPCBC output current (100µH to500 µH)

modules in the steady state using PI controller. It is evident from the figure that the output voltage ripple is little high about 0.025V.

**Circuit components variations:** Figure 22 and 23 represents the response of the output voltage and current of paralleled modules using both SMC and a PI controller for the variation of inductor L from 100-500µH. It can be seen that the change does not influence the paralleled converters behavior due to the proficient design of the designed controller in comparison with a conventional PI controller.

An interesting result is illustrated in above Fig. 24 and 25. It shows the response of the output voltage and the current of the paralleled modules with both a PI controller and the proposed controller scheme for a variation in the capacitors values from 30-100µF. It can be seen that the SMC is very successful in suppressing the effect of the capacitive variation except that a negligible output voltage ripple with a quick settling time and a proper current distribution in comparison with

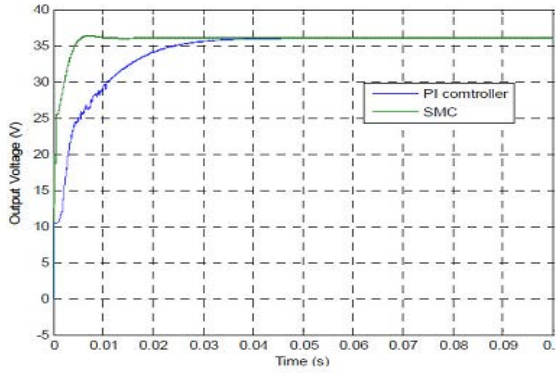



Fig. 24: Performance of POEPCBC output voltage (30μF to 100μF)

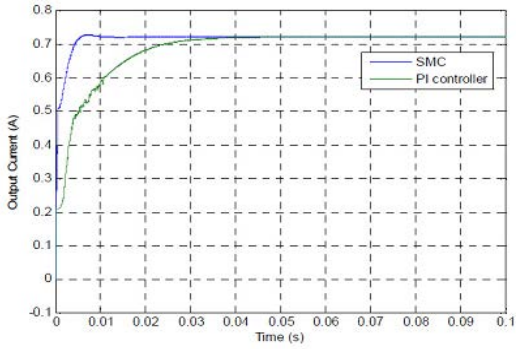



Fig. 25: Performance of POEPCBC output current (30μF to 100μF)

a conventional PI controller. In summary from Figure 24 and 25, it is obviously specified that the simulated graphs of developed SMC has excellent performance of POEPCBC in comparison with a conventional PI controller during circuit component variation.

The main purpose of this section is to discuss the experimental results of POEPCBC with the designed SMC. The verification of the model performance is completed for different conditions. The laboratory prototype model is performed on POEPCBC circuits with the same specification as the simulations

The parameters are as follows

Q IRFN 540 (MOSFET);
D FR306 (Diodes);
C 30μF/100V (Electrolytic and plain polyester type);
L 100μH/5A (Ferrite Core)

The parameters of the controller coefficients are: $K_1$ = 0.667, $K_2$ = 0.217 and $\delta$ = 0.5 as calculated in the previous section. The designed SMC is implemented in an analog platform and its operation is as follows; the inductor current and the capacitor voltages $V_{c1}$ and $V_{c2}$ of the POEPCBC are sensed by using an LA 25–NP current sensor, resistances, capacitors and LM324 operational amplifiers which are then compared with reference signals by using an LM324 operational amplifier that gives error signals. The inductor current error signal is further processed through a HPF (20kHz) for the purpose of filtering out the low frequency component of the converter as the controller allows only high frequency signals. The output of the entire designed controller signals are summed and compared using an LM311 to generate the PWM. First time gate drive control signal of the generated gate signal is passed through the opt-isolator (MCT 2E) and the driver circuit (transistors SK100, 2N2222 and the resistance arrangement) and then to the MOSFET. In MOSFET there is an internal capacitor in the gate terminal. Therefore, the transistors (2N2222 and SK100) are used as a quick charging and discharging capacitor and also for amplification. The output of the driver is directly connected to the gate of the MOSFET (IRFN 540) through the resistance as shown in Fig. 26. Using SMC, the switching frequency of the gate pulse is varied to regulate the output current and the voltage and also to improve the dynamic performance of the POEPCBC.

**Start-up region:** Figure 27 shows the dynamic behavior in the start-up for output voltage in POEPCBC for different input voltage viz. 9V, 12V and 15V. it can be seen that output voltage of POEPCBC has a little overshoot and settling time of 0.005s for Vin = 15V, where for 12V and 9V there are negligible overshoots and settling time of 0.007s and 0.01s for the designed SMC respectively. Fig. 28 shows the dynamic behavior in the start-up for output voltage of POEPCBC for different load resistances like 40Ω, 50Ω and 60Ω. It is seen that output voltage of POEPCBC has a slight overshoot and settling time of 0.005s for R = 60Ω, R = 50Ω and R = 40Ω, the output voltage has negligible overshoot and settling times of 0.007s and 0.01s in start-up with designed SMC respectively. Figure 29 and 30 shows the dynamic behavior at start-up for the average output currents of modules-1 and modules-2 for $V_{in1}$ = 12V and $V_{in2}$ = 15V. It can be seen that the output current of modules-1 and modules-2 for $V_{in1}$ = 12V and $V_{in2}$ = 15V has an equal current distribution.

**Line variations:** Figure 31 shows the simulation response of average output voltage of POEPCBC using SMC for input change from 12V to 15V (+30% line variations) at time = 0.11s and 0.05s from these Figures, it is clearly found that both the simulated and experimental response of output voltage of the POEPCBC using SMC has maximum overshoot of 2.5V and settling time of 0.025s.

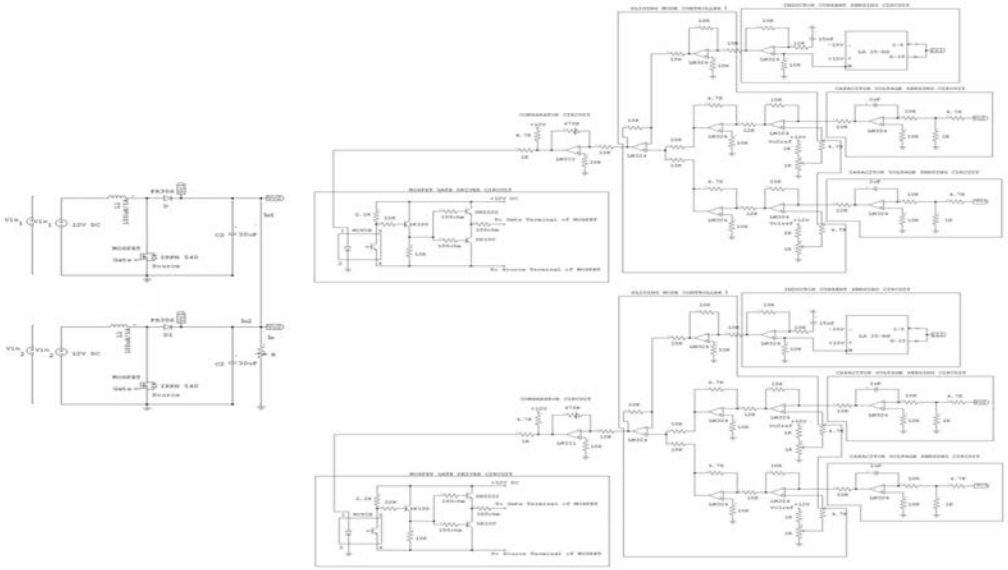


Fig. 26: Prototype model of POEPCBC using SMC

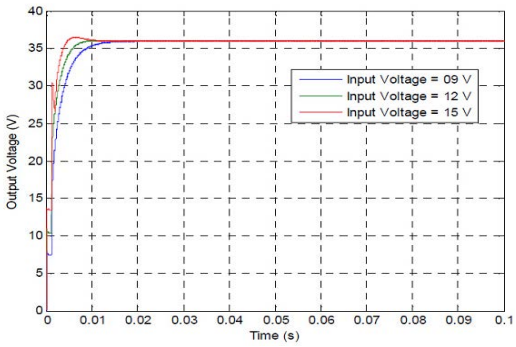



Fig. 27: Start-up response of avereage output voltage of POEPCBC (R=50)

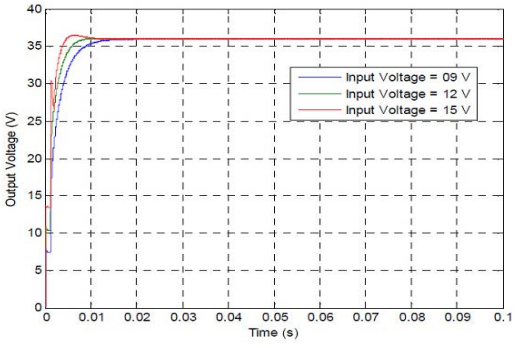



Fig. 28: Start-up response of avereage output voltage of POEPCBC (Vin=12V)

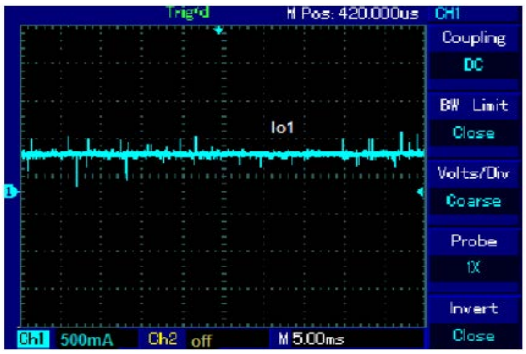



Fig. 29: Start-up response of various input voltage (Vin1=12V and Vin2=15V) and average output current of POEPCBC 1 [Ch1: 500mA/Div-load current]

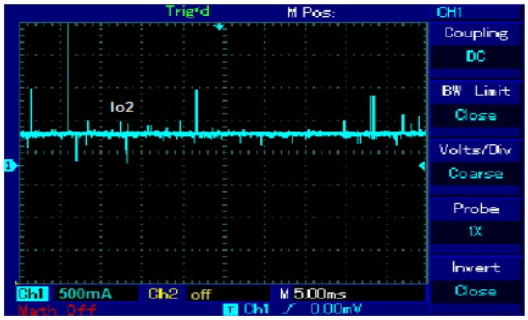



Fig. 30: Start-up response of various input voltage (Vin1 = 12V and Vin2 = 15V) and average output current of POEPCBC 2 [Ch1:500mA/Div-load current]

Figure 32 shows the experimental response of the average output voltage of the POEPCBC using SMC for and input voltage step change from 12V to 15V (+30% line variations) at time = 0.02s. From these Figures, it is clearly found from the experimental response that the

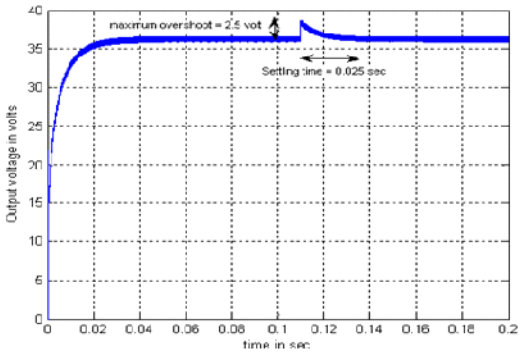



Fig. 31: Output voltage of POEPCBC (12V to 15V

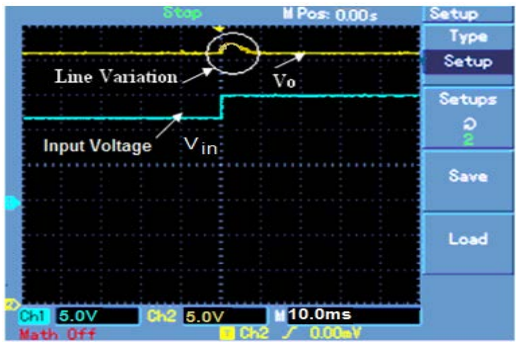



Fig. 32: Output voltage of POEPCBC for input step change from 12 -15 V at time 0.05s with R= 50Ω [Ch1:5V/Div-output voltage and Ch2:5V/ Div-input voltage]

output voltage of the POEPCBC using SMC has a maximum overshoot of 2.5V and a settling time of 0.02s.

Figure 33 shows the simulation response of average output voltage of POEPCBC using SMC for input change from 12V to 9V (+30% line variations) at time = 0.11s and 0.05s. From these Figures, it is clearly found that both the simulated and experimental response of output voltage of the POEPCBC using SMC has maximum overshoot of 2.3V and settling time of 0.02s. Figure 34 shows the experimental response of the average output voltage of the POEPCBC using SMC for an input voltage step change from 12V to 9V (-30% line variations) at Time = 0.02s. It can be seen from the experimental response that the output voltage of the POEPCBC using SMC has a maximum overshoot of 2.3V and a setting time of 0.02s.

**Load variations:** Figure 35 shows the simulated response of output voltage of POEPCBC using SMC for load change 50Ω-60Ω (+20% load variations) at time = 0.05s. It could be seen that both simulation and the experimental

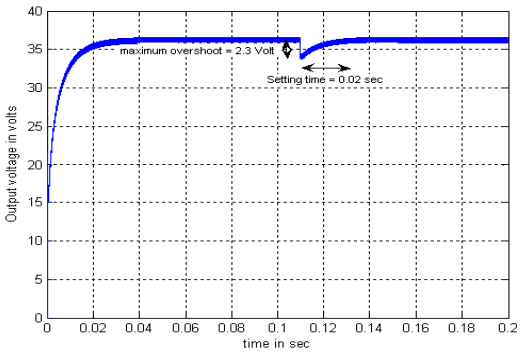



Fig. 33: Output voltage of POEPCBC (12 V to 9V)

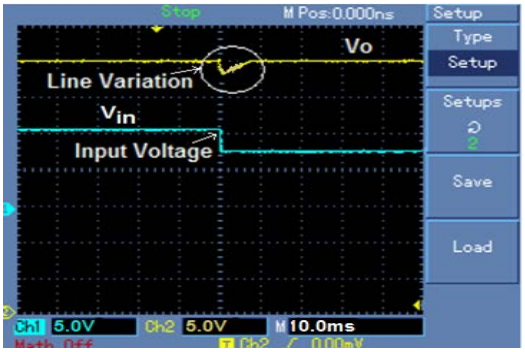



Fig. 34: Output voltage of POEPCBC for input step change from 12-9V at time 0.05s with R=50Ω [Ch1:5V/Div-output voltage and Ch2:5V /Div-input voltage]

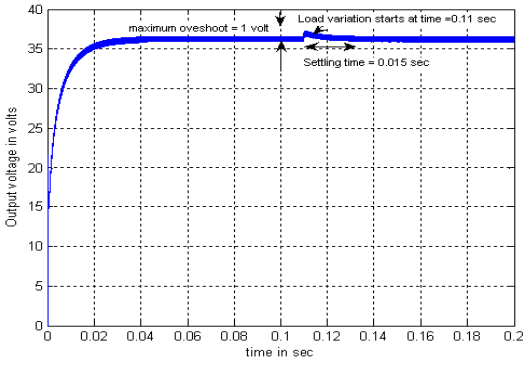



Fig. 35: Output voltage of POEPCBC (50-60Ω)

results of output voltage of POEPCBC using SMC has a small overshoot of 1V with quick settling time of 0.015s. Figure 36 shows the experimental response of the output voltage of the POEPCBC using SMC for a load step change from 50Ω-60Ω (+20% load variations) at time = 0.05s. It can be seen from the experimental results that the output voltage of the POEPCBC using SMC has a small overshoot of 2V with a quick setting time of 0.01s.

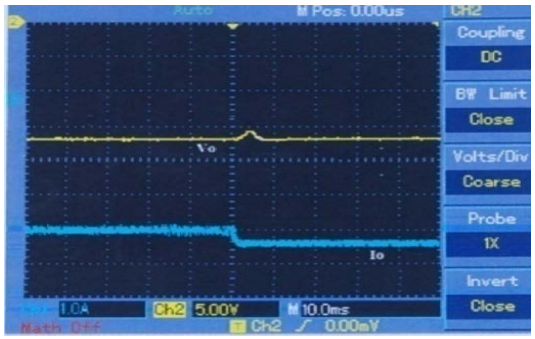



Fig. 36: Output voltage of POEPCBC when load value takes a step changes from 50-60Ω at time 0.05s with Vin=12V [Ch 1:5V/Div-output voltage and Ch2:500mA/Div-load current]

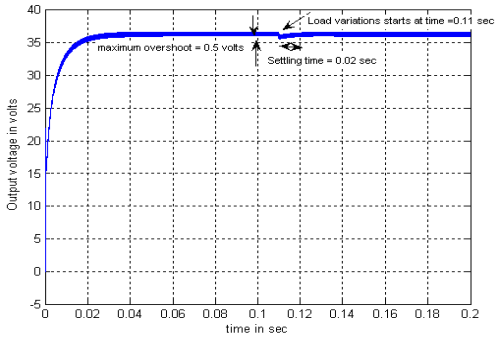



Fig. 37: Output voltage of POEPCBC (50-40Ω)

Figure 37 shows the experimental and simulated response of output voltage of POEPCBC using SMC for load change 50Ω-40Ω (+20% load variations) at time = 0.05s. It could be seen that both simulation and the experimental results of output voltage of POEPCBC using SMC has a small overshoot of 0.5V with quick settling time of 0.02s. From Fig. 35 and 37, it is clear that the experimental results exhibit close agreement with simulation results under load variation with the designer controller.

Figure 38 shows the experimental response of the output voltage of POEPCBC using SMC for a load step change 50Ω to 40Ω (-20% load variations) at time = 0.05s. It can be seen from the experimental results that the output voltage of the POEPCBC using SMC has a small overshoot of 2V with a quick setting time of 0.01s. Table 4 shows the experimental and simulated results of the average output current and voltage of each of the modules and the POEPCBC with the developed controllers for various input voltages and load resistances in the start-up region. From Table 4, it is clearly found that the voltage that the voltage regulation and the current

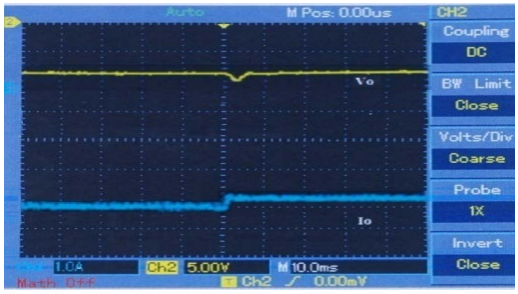



Fig. 38: Output voltage of POEPCBC when load value takes a step changes from 50-40Ω at time 0.05s with Vin=12V [Ch 1 :5V/Div-output voltage and Ch2:500mA/Div-load current]

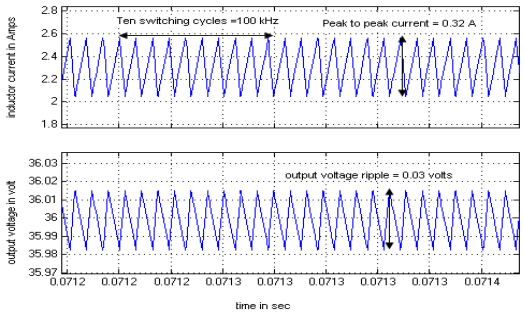



Fig. 39: Inductor current iL and output voltage of POEPCBC in steady state condition using SMC

distributions of each of the modules and the POEPCBC using the designed SMC show excellent performance with a clearance of 2%.

**Steady stage regions:** Figure 39 shows the simulation instantaneous output and the inductor current of POEPCBC in the steady state region using developed controller. It is evident from the figure that the output voltage ripple is very small about 0.18V/0.03V and peak to peak inductor ripple current is 0.42A/0.32A for the average switching frequency of 100kHz closer to theoretical value listed in Table 1. Figure 40 shows the experimental instantaneous output voltage and inductor current of the paralleled modules in the steady state region using the SMC. It is marked from the figure that the load voltage ripple is very low about 0.45V and that the peak to peak inductor ripples current is 0.4A for an average switching frequency of 100kHz and is closer to the theoretical designed value listed in Table I.

In summary, from this it is clearly signified that the experimental results of the POEPCBC using the designed SMC match the simulated results with a tolerance of 2%. The proposed SMC performed well in all of the working

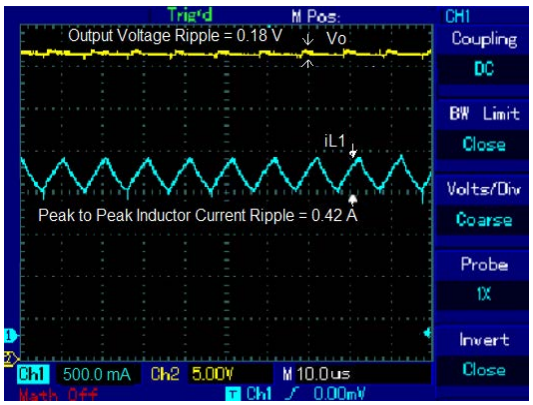



Fig. 40: Experimental response of output voltage and inductor current iL of POEPCBC in steady state condition using SMC [Ch 1:500mA/Div-inductor current]

Fig. 41: Laboratory prototype set-up model of POEPCBC using SMC

conditions of the POEPCBC. Figure 41 illustrates the experimental set-up model of the SMC for the POEPCBC.

## CONCLUSION

This study has successfully demonstrated the design and suitability of the sliding mode controlled based possitive output elementry parallel connected boost converter. The simulation based performance analysis of a sliding mode controlled positive output elementary parallel connected boost converter circuit has been presented along with its state averaged model. The proposed control scheme has proved to be robust and its triumph has been validated with load and line regulations and also with circuit components variations. Therefore, the system achieves a robust output voltage against load disturbances and input voltage variations to guarantee the output voltage to feed the load without instability. The approach thus has several advantages for it credits: stability even for large supply, load variations and circuit components variations, robustness, good dynamic behaviour and simple implementation. The proposed configuration, thus claims its use in applications such as computer peripheral equipment and industrial applications, especially for high output voltage projects.

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