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An Efficient 2D DWT-A Distributed Arithmetic with Rapid Arithmetic Coder for Medical Image Compression

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Abstract: Image compression plays a very important role in image processing. Image compression means minimizing the size in bytes, without humiliating the quality of image to an unacceptable level. Image compression allows more images to be stored in a given amount of memory space and reduces the time required for images to be transfer. Discrete wavelet transforms is the most adaptive transformation technique for image compression but its arithmetic operation is so complex. In order to overcome the above problem 2D DWT Distributed Arithmetic (DA) for real time signal processing was used. The design and implementation of medical image compression using an efficient 2D DWT-A using DA based with rapid arithmetic coder is proposed. The architecture consists of efficient 2D DWT-A using DA based which was implemented in previous work. In the proposed method, a rapid arithmetic coder is implementing, the coder is modified with carry select adder using BEC-1 and position control unit. Instead of using leading check detection, a position control unit is implementing. The position control unit is used to reduce the area and power consumption. The overall architecture reduces the arithmetic computation, area utilization and high speed performance.

Keywords: Discrete wavelet transforms, 2D DWT, Distributed Arithmetic (DA), real time signal, arithmetic coder, carry select adder using BEC-1

INTRODUCTION

In telemetric applications and telemedicine, image compression acts a very important position. The images can be transmitted over computer networks at great distances so as that they could be applied in a multitude of purposes. For example, it is required that medical images be transmitted so as that reliable, improved and fast medical diagnosis executed by several centers could be made easy. To this conclusion, image compression is an imperative research matter. The complexity, on the other hand, in numerous applications lies on the fact that, while high compression rates are preferred, the applicability of the reconstructed images relies on whether some important features of the original images are protected after the compression process has been concluded.

Diagnosis is effectual in medical image compression applications, only when compression techniques preserve all the related and significant image information required. This is the case with lossless compression techniques. Lossy compression techniques, alternatively are more competent in terms of storage and transmission needs however there is no warranty that they can preserve the feature required in medical image processing and diagnosis. Lossless compression technique is mostly preferred for medical image compression. The essential block diagram of image compression is displayed beneath in Fig. 1.

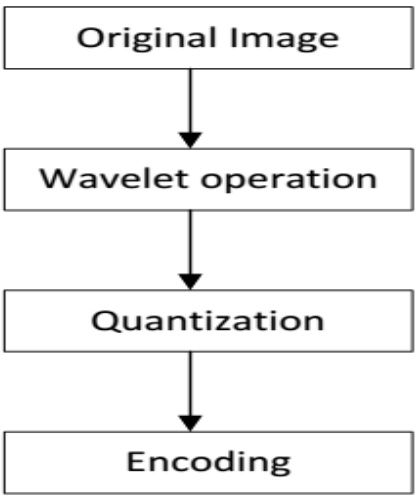

Fig. 1: Basic block diagram of image compression

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The most important transformation method applied for image compression is Discrete Wavelet transform (Debnath *et al*., 2008). The most significant section is encoding in image compression. Encoding is the process of changing information into symbols for transformation and storage. Many coding methods are applied such as Huffman coding (Lim *et al*., 2007), Entropy encoding (Permana, 2012) Run length encoding (Weinlich *et al*., 2013), etc. Arithmetic coding (Shah and Vithlani, 2011) offers more flexibility and improved efficiency when compared to these methods. Arithmetic coding is applied for lossless data compression. The most important drawback of arithmetic coding is computation speed is slow.

The 2D DWT Distributed Arithmetic (DA) technique (Mugilvannan and Ramasamy, 2013) is employed to surmount these defects. In our reseaqrch, we employ a efficient 2D DWT Distributed Arithmetic with rapid arithmetic coder. Using poly-phase DA design it was effective hardware utilization with low power consumption and reduction in multipliers was employed. In addition, the utilization of Look-Up Table (LUT) and high speed performance with the assist of Parallel DA scheme was executed. The adapted arithmetic coding with high speed performance is applied to develop the speed.

Literature review: For image compression, Nagabushanam *et al*. (2011) brought in design and FPGA implementation of modified distributive arithmetic based DWT-IDWT processor for image compression. In their research, an adapted distributive arithmetic based DWT architecture was progressed and executed on FPGA. The poly-phase architecture with adapted DA technique was executed for the Daubechies 2. The executed architecture used the area of 6% on Virtex-II pro FPGA and operated at 134 MHz. The latency of the executed architecture was 44 clock cycles and throughput was 4 clock cycles and therefore it was twice faster than the reference design. It was observed that in applications which needed low area, power consumption and high throughput, e.g., real-time applications, the poly-phase with DA architecture was more appropriate. The biorthogonal wavelets with dissimilar number of coefficients in the low pass and high pass filters, raised the number of operations and the difficulty of the design however, they had improved SNR than the orthogonal filters. Initially, the code was written in Verilog HDL and executed on the FPGA by means of a 32×32 random image. After that the code was taken through the ASIC design flow. The 8×8 memory is measured to accumulate the image for the ASIC design flow. The executed architecture facilitated fast computation of DWT with analogous processing. It had low memory necessities and uses low power.

Liu and Xu (2011) planned high speed architecture of arithmetic coder. They progressed high speed arithmetic coder architecture. In their effort, out-of-order execution mechanism for dissimilar types of situation was applied that could assign the context symbol to the idle arithmetic coding core with a dissimilar order compared with the input order. In one arithmetic coder, for the balance of the input rate of contexts, there present N cores for processed dissimilar contexts; N was the number of context type. The similar bit circuit was applied for unrolling the renormalization stage of arithmetic coding. An offered circuit was planned for unrolling the internal loop because of time used for under flowing which could practice under flowing situation in a few clock cycles. The executed architecture reached a throughput of 375.50 Mega contexts per second at its maximum based on field programmable gate arrays.

A novel architecture for an efficient implementation of image compression using 2D-DWT has been suggested by Parvatham and Seetharaman (2012) by means of 2D-DWT. Design and execution of image compression by means of 2D DWT was brought in their work. Modified flipping was a competent architecture which was developed for the execution of image compression by means of 2d DWT. The SOC technique was implemented for the execution of 2D DWT on Altera Field Programmable Gate Arrays (FPGAs) based SOC CYCLONE II EP2C35F672C6 kits with NIOS-II soft-core processor. The effect of executed architecture raised the speed and decreased the number of logical elements and registers. For signed multiplication, a novel multiplier algorithm called as Modified Baugh-Wooley Pipelined Constant Coefficient Multiplier (MBW-PKCM) was progressed. In order to execute MBW multiplier, Distributed Arithmetic architecture with constant coefficient multiplier was used. The executed effects illustrate that the Modified flipping Architecture (MFA) and MBW-PKCM decrease the hardware requirements and the speed of the design is raised.

Liu *et al*. (2012) proposed VLSI architecture of arithmetic coder used in SPIHT. Based on a simple context model, High-throughput memory-efficient arithmetic coder architecture for the Set Partitioning in Hierarchical Trees (SPIHT) image compression was planned. The architecture advantages from different optimizations executed at dissimilar levels of arithmetic coding from higher algorithm abstraction to lower circuits implementations. By designing a simple context model, the complex context model employed by software was alleviated which just used the brother nodes' states in the coding zero tree of SPIHT to create context symbols for the arithmetic coding. The easy context modeled results

in a regular access pattern during reading the wavelet transform coefficients which was expedient to the hardware implementation, however at a cost of slight performance loss. To evade rescanning the wavelet transform coefficients, a breadth first search SPIHT without lists algorithm was applied instead of SPIHT with lists algorithm. The coding bit-planes of each zero tree were practiced in similar. For dissimilar types of context, an out-of-order execution mechanism was developed that could assign the context symbol to the idle arithmetic coding core with a different order that of the input. In the compression system, the balance of the input rate of the wavelet coefficients, eight arithmetic coders were repeated. Along with, there present four cores to process dissimilar contexts in one arithmetic coder. To develop the architecture further, a number of dedicated circuits were planned. The Common Bit Detection (CBD) circuit was applied for unrolling the renormalization stage of the arithmetic coding. In order to shorten the critical path in the architecture, the Carry Look-Ahead adder (CLA) and fast multiplier-divider were in addition utilized. According to the input images an adaptive clock switch mechanism could discontinue several invalid bit-planes' clock for the power saving reason. Experimental results show that the designed architecture reaches a throughput of 902.464 Mb sec^{-1} at its maximum and attains savings of 20.08% in power consumption over full bit-planes coding plan based on Field-Programmable Gate Arrays (FPGAs).

For image compression with arithmetic coding, (Malviya *et al*., 2013) proposed 2D-discrete walsh wavelet transform for image compression with arithmetic coding. In their technique using DWT a novel plan for image compression was progressed. The Walsh Wavelets transform with arithmetic coding techniques was to take away redundancy from images. The method has two steps initially a two levels discrete wavelet transforms on chosen input image. The original image was decayed at dissimilar 8×8 blocks, after that apply 2D-Walsh-Wavelet Transform (WWT) on each 8×8 block of the low frequency sub-band. Initially, divided each sub-band by a factor and next applied arithmetic coding on each sub-band separately. Change each 8×8 block from LL2 and after that divided each block 8×8 separated into; DC value and compressed by Arithmetic coding.

Harika and Reddy (2013) proposed design and implementation of arithmetic coder used in SPIHT. Set Partitioning in Hierarchical Trees (SPIHT) algorithm for image compression was progressed with a arithmetic coder thus it compressed the Discrete Wavelet Transform decomposed images. The executed architecture was helpful from various optimization carried out at different levels of arithmetic coding from higher algorithm abstraction to lower circuit implementation. SPIHT had uncomplicated coding procedure and needed no tables which make a SPIHT algorithm an apt one for low cost hardware implementation. The wavelet transformed coefficients a breadth first search SPIHT without lists was applied in order to evade rescanning, rather than SPIHT with lists. High speed architecture was accomplished with the assist of Breadth First search. For loop unrolling the renormalization stage of arithmetic coding, dedicated circuit such as common bit detector was applied. Critical path in the architecture were shortened by used Floating point multiplier and take look ahead adder. The implemented design had been executed on Spartan 6 FPGA. A throughput of coder is 800 Mb sec^{-1} for a pixel precision of 8 bits with a resolution of 512×512.

Based on arithmetic coding (El-Arsh and Mohasseb, 2013) proposed a new light-weight JPEG2000 encryption technique based on arithmetic coding. In their research, a new multimedia security framework based on the nonlinear properties of the arithmetic coder which was employed by most image and video coding standards in the entropy coding stage was planned. The improved technique carries out concurrent entropy coding and encryption which decreased the delay and the needed system resources by manipulating the probability maps of the arithmetic coder. In addition, the suggested technique did not acquire any additional difficulty for executing encryption, nor did it raise the size of the compressed image. As a result, when applied the proposed technique to un-encrypted images, in contrast to standard encryption techniques, the decoder could yet gradually show the decoded/deciphered image. Moreover, there was no companion error-propagation generally related with that kind of encryption. Unlike most block ciphers, the suggested plan did not require to append any extra bits to the coded bit stream. Using arithmetic coding the suggested method could be employed to any multimedia coder. On the other hand, the executed method was tailored to the JPEG2000 standard. In addition, evaluations and measurements for this encryption method were initiated.

An efficient compression system for ECG signal using QRS periods and CAB technique based on 2D DWT and Huffman Coding has been proposed by Ranjeet *et al*. (2013). In their research, based on two-Dimensional Discrete Wavelet Transform (2D DWT) and Huffman coding technique an ECG compression system was offered. In their executed method, two dissimilar approaches were used to erect a 2D array of 1D ECG signal by means of cut and align (CAB) technique, thus ECG 2D array was decayed with 2D DWT which effect

more number of irrelevant coefficients. They were measured as zero amplitude value which speed up compression rate and Huffman coding sustains the signal quality due to its lossless nature of compression. The standard compression performance of algorithm was 65% with 0.999 correlation score.

MATERIALS AND METHODS

Without degrading the quality of the image, image compression is to minimize the size in bytes, the decreased in size permits more images to be accumulated in a specified amount of memory space. With the rising demand of storage and transmission of digital images, image compression is currently turned out to be an important application for storage and transmission. In compressing images, image compression makes use of different techniques and algorithms. The techniques so applied by image compression can be categorized as lossless and lossy compression. Lossless compression is desired for medical image compression. The method of compression applied relies on the desired quality of output. Image compression is commonly applied in medical, technical drawing, automotive and military applications.

Discrete Wavelet transform is the most well-liked transformation technique applied for image compression. The DWT can decay the signals into dissimilar sub-bands with both time and frequency domain. It furthermore supports characteristics like progressive image transmission, compressed image manipulation and region of interest coding. However the DWT operation is so difficult since the arithmetic operation count is more. In image compression technique there is one coder is employed for making codeword for the symbol. Frequently desire coder is arithmetic coder. Arithmetic coding is a structure of entropy encoding applied in lossless data compression. The most important difficulty of arithmetic coding is decreased in computation speed.

In order to minimize the arithmetic operation, area utilization and power consumption we employ an efficient 2D DWT-A distributed arithmetic with rapid arithmetic coder was executed in our suggested method of medical image compression. And an adapted arithmetic coder is implemented to decrease the computation speed.

Proposed method: The medical image compression by means of an efficient 2D DWT-A with a rapid arithmetic coder is suggested in our work. Discrete transformation is initially used on the source image data. The output extracted from 2D DWT-A DA is next offering to zigzag scanning. After achievement of these operations at last it

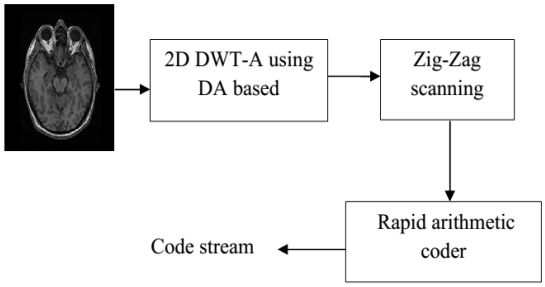

Fig. 2: Block diagram of proposed method

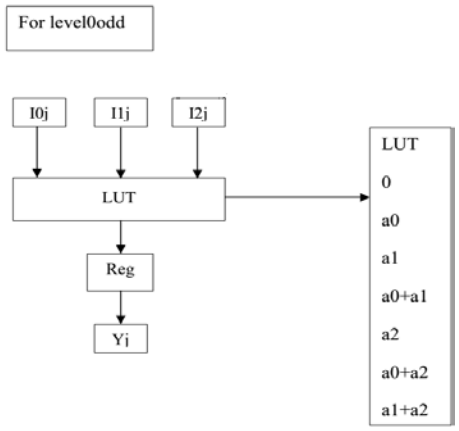

Fig. 3: Level 0 odd

is fed to rapid arithmetic coder. The code stream output is obtained from the coder. The actual image compression is carried out with VLSI by means of Xilinx 14.1 Vertex-5. The block diagram of the proposed method is shown in Fig. 2.

2D DWT-A using DA based: The 2DWT-A architecture performs fully parallel DA (Parvatham and Gopalakrishnan, 2012) implementation for the row-wise convolution operation which decrease the access time and a polyphase method in DA (Liu *et al*., 2012) as execution for the column-wise parallel-pipelined lifting operation to attain minimum shift-add operation. A fully parallel 8 bit PDA FIR filter executed is shown in Fig. 3. The 2D DWT-A DA method is detail explicated in our previous work. Using shift register, LUT and a binary-tree like adder which is scaled by a factor 2, the architecture attains maximum speed by splitting of the 8 bit input sample into eight 1-bit sub-samples. Figure 3 demonstrates the level 0 odd operation and Fig. 4 demonstrates the level 0 even operation and Fig. 5 demonstrates competent 2DWT-A architecture for row-wise convolution operation by means of Parallel DA method.

Parallel DA: The DA-based computations are naturally bit-serial. It takes 8 clock cycles to calculate one output

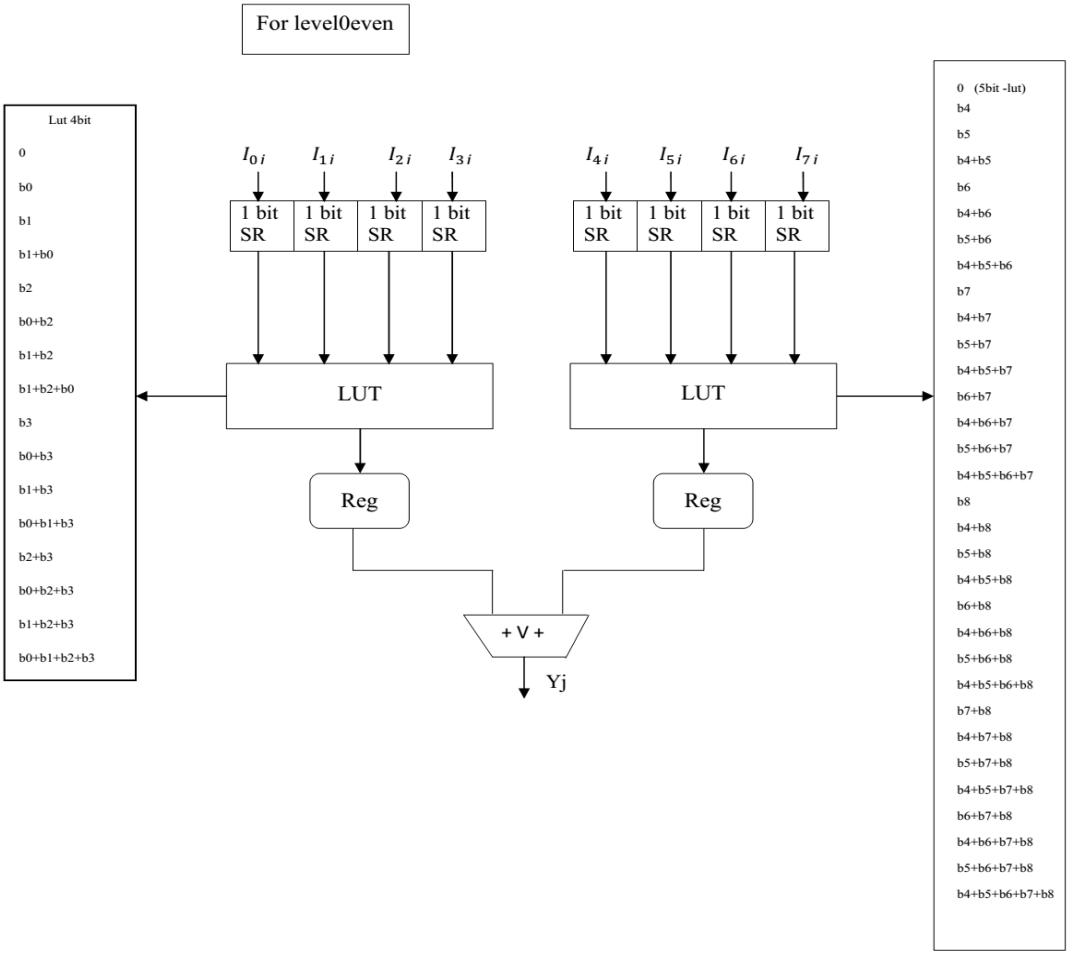

Fig. 4: Level 0 even

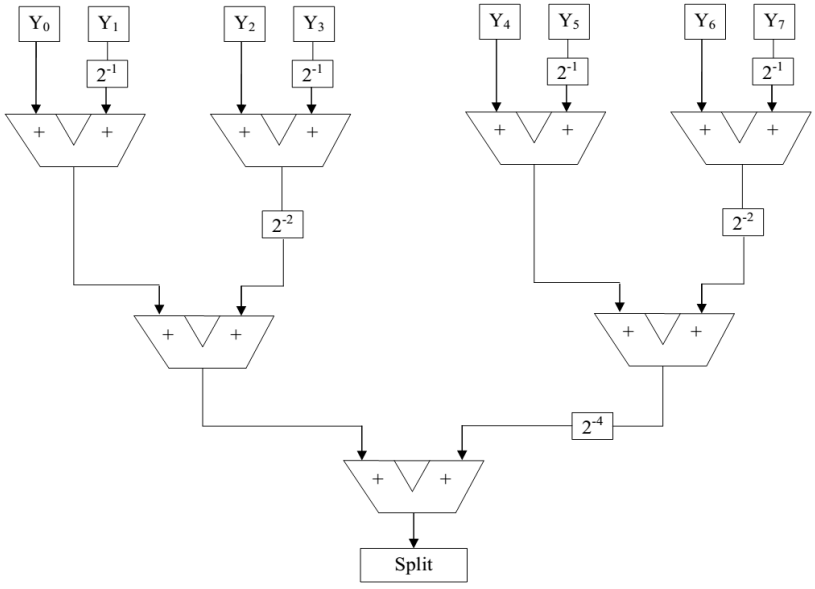

Fig. 5: Efficient 2DWT-A architecture for row-wise convolution operation using parallel DA method

for an 8 bit input (Liu *et al*., 2012). As a result, this Serial Distributed Arithmetic (SDA) filter has a low throughput. The number of bits of the input is practiced in a clock period relies on the filter design. The input word that are Partitioned into M sub-words requires M-times as many memory LUTs and this in turn increases the storage requirements. But, a new output is calculated every B/M clock cycles and not of every B cycles. A fully parallel DA (PDA) filter is proposed by factoring the input into single bit sub-words in order to attain maximum speed. A new output is calculated every clock cycle. Figure 3 demonstrates a parallel DA architecture for an N-tap filter. The 8 bit input word is separated into eight 1 bit sub-samples so as to attain higher throughput for the parallel 8-bit DA FIR filter completion. Figure 3 (Parvatham and Gopalakrishnan, 2012) displays the ultimate fully parallel PDA FIR filter where all 8 input bits are practiced in parallel and after that summed by a binary-tree like adder network. By a factor of 2, the lower input to each adder is scaled down. No scaling accumulator is required in this case as the output from the adder tree is the complete sum of products. The output from the 2D DWT-A DA contain four outputs, they are LL, LH, HL, HH and we take the LL value for our work since it have non zero values and high amplitude.

Zig-Zag scanning: The wavelet coefficients attained from the 2D DWT-A DA are scanned in a zigzag order. The zigzag scan begins from top-left corner of the matrix and then goes along the top row of the matrix. It directs to a coefficient sequence that encloses large number of trailing zero values which can be encoded much more competently by the subsequently entropy coding operation. Figure 6 demonstrates the zigzag scan order.

Principle of arithmetic coding: Arithmetic coding is an encoding technique applied in lossless image compression. Arithmetic coding is very much required in image and video compression applications. In arithmetic coding, a sequence of input symbol is symbolized by an interval of real number between zero and one. The interval to signify the information becomes smaller if the information is longer. Arithmetic coder allocates one codeword to each feasible inputs, the codeword is a half subinterval of the initial interval (0, 1) (Malviya *et al*., 2013).

Let us consider a set of symbols denoted as S. The probability for a given set of symbol $\{P_i\}\varepsilon[0,1]$. While, adding all the probability of the input symbol the total sum of the probability is equal to one, i.e. $\sum_{i=0}^{i-1} P_i(j) = 1$ and its cumulative probability is defined as cumulative count of the symbol 'i' $CP[i] = \sum_{j=0}^{i-1} P_i(j)$. Cumulative probability is

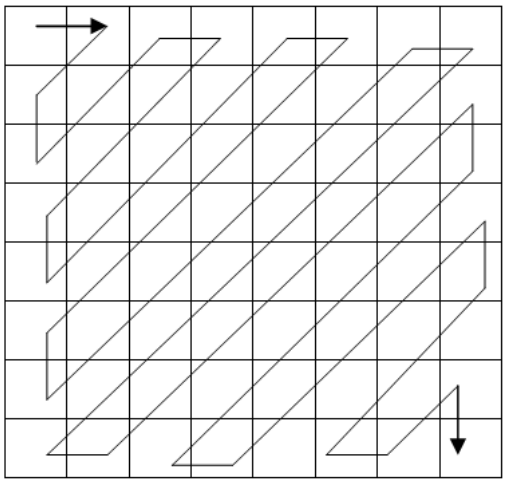

Fig. 6: Zig-Zag scan order

update by the value of symbol probability. For example to find out the cumulative probability value CP[1] and CP[2], it can be calculating by:

$$CP[1] = P[0]+P[1]$$
$$CP[2] = P[0]+P[1]+P[2]$$

and so on. In arithmetic coder three register are used they are range, high and low which can be defined as:

$$\text{Range} = \text{high-Low} \quad (1)$$

$$\text{High} = \text{low}+\text{range}\times\text{high range of symbol being coded} \quad (2)$$

$$\text{Low} = \text{low}+\text{range}\times\text{low range of symbol being coded} \quad (3)$$

From cumulative probability (CP [i-1], CP[i]) the low range and high range of the symbol is attained, i.e., low range of symbol being coded is the value of CP [i-1] and high range of symbol being coded is the value of CP [i]. At first the low and high value is fixed as zero and one correspondingly.

Architecture of rapid arithmetic coder: In this section architecture of rapid arithmetic coder is offered. The internal operations of the coder are performed in fixed length registers with a width of 16 bits to signify the symbol and cumulative probability and 16 bits for the range and low interval. In Fig. 7, the block diagram of rapid arithmetic coder is displayed.

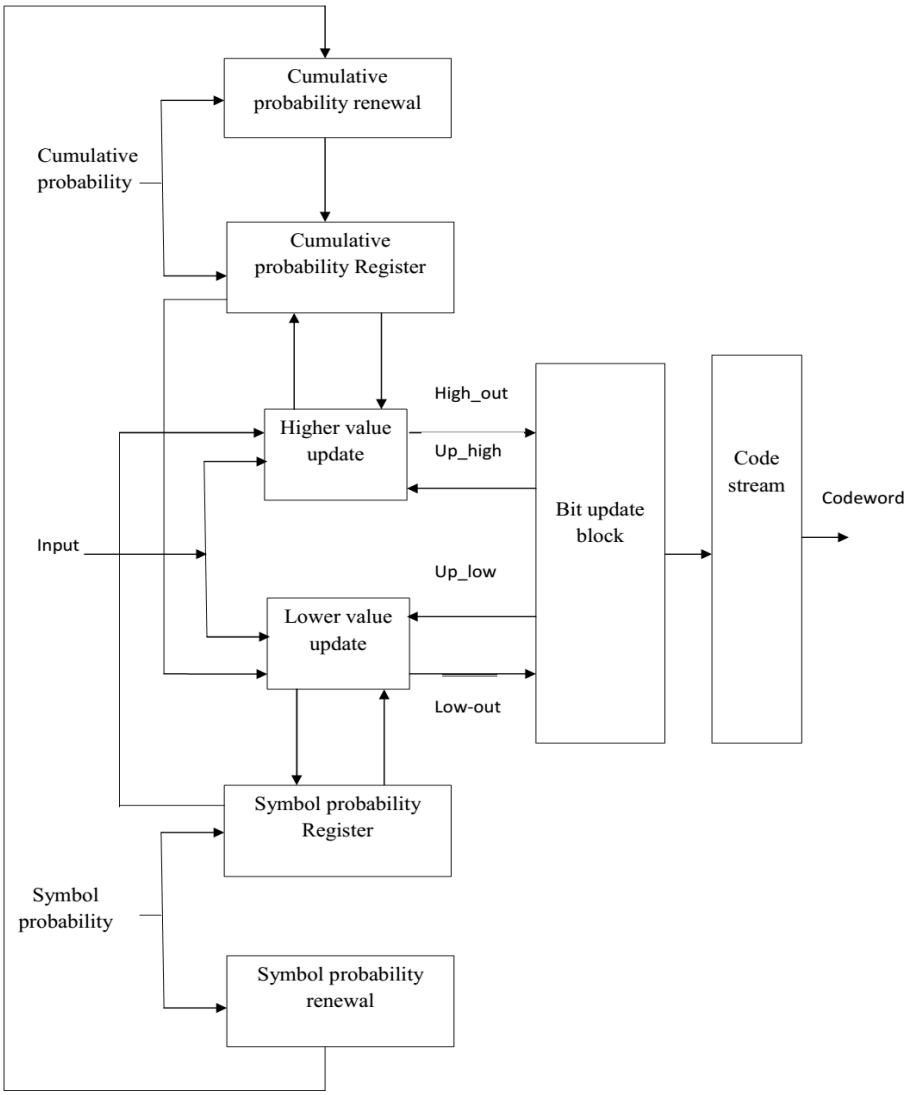

Fig. 7: Block diagram of rapid arithmetic coder

Higher value and lower value update: Higher value and lower value registers are the two registers in this method. The conventional method (Permana *et al*., 2012) and (Shah and Vithlani, 2011) employed carry look ahead adder for addition operation. The rapid arithmetic coder apply carry select adder using BEC-1[12] which is area competent and high speed in operation. From the Eq. 2 and 3, the higher value and lower value update can be computed. Output of higher and lower update units are up_high and up_low. A carry select adder using BEC-1 and a floating point multiplier is applied for speed up purpose. The cumulative probabilities CP[i] and CP[i-1] are provided from the cumulative probability register file. The computations for higher and lower value diagrams are demonstrated in Fig. 8.

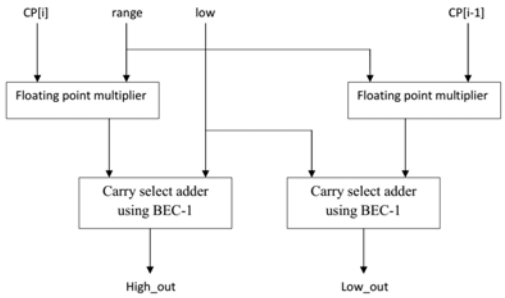

Fig. 8: Higher value and Lower value update calculation

Bit update block: In Fig. 9, the internal structure of bit update block is illustrated. The inputs of bit update are high_out and low_out values after completion of higher

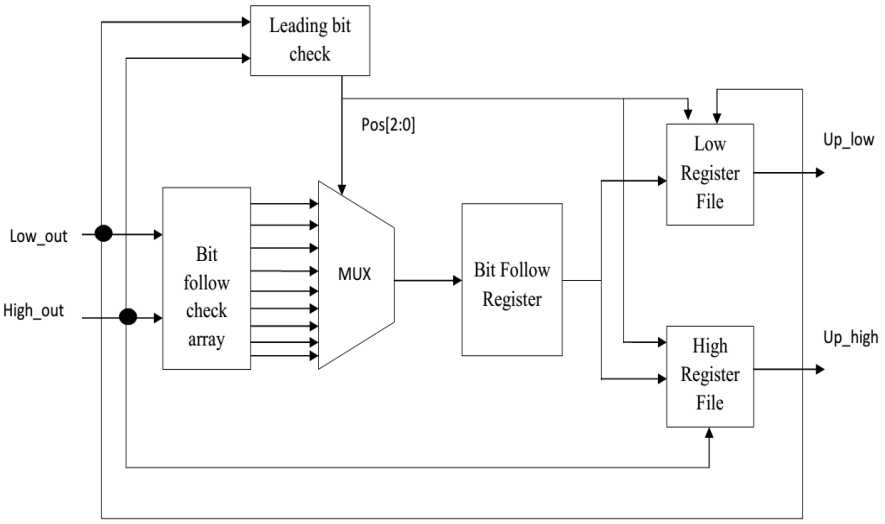

Fig. 9: Block diagram of bit update

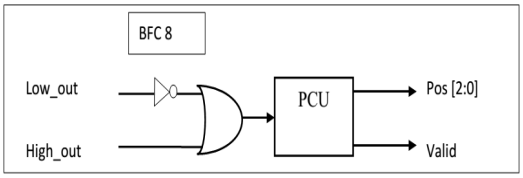

Fig. 10: Structure of BFC

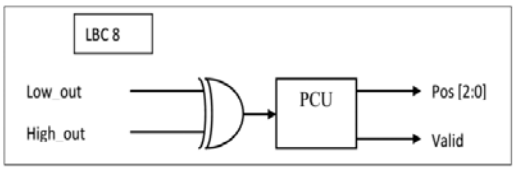

Fig. 11: Structure of LBC

value and lower value calculation of Eq. 2 and 3. For rapid arithmetic coder, the code bits are attained by an internal loop and records the same bit from the MSB to the LSB among two register. The low and high register files transferred Up_low and Up_high values to higher value update and lower value update applied for the next run.

The Leading Bit Check (LBC), in the bit update block detect out the common bits among low and high registers. In (Shah and Vithlani, 2011) they applied leading zero detectors for leading bit check and Bit Follow Check (BFC). We execute a Position Control Unit (PCU) instead of leading zero detectors in order to speed up the process and area efficient. The leading bit check contain logic gate and position control unit. The bit follow check array is for checking the mode of underflow operation. The BFC check eight possible cases for speed up purpose with the assist of pos [2:0] from LBC that selects one of the bits follow value from eight cases based on common bit position. In Fig. 10 and 11, the structure of BFC and LBC is explained and the internal structure of bit follow check array is illustrated in Fig. 12.

In Fig. 12, the proposed architecture of position control unit is demonstrated. The position control unit has temporary register to accumulate the 8 bits. This register reads the bit from most significant bit to least significant bit, for this purpose we employ left shifter to shift the bit to left position at each clock cycle. In first clock cycle it reads the first most significant bit and given to one multiplexer. The multiplexer check the bit to zero or one, whether the bit is zero then the input 1 from the multiplexer is added with position, i.e., is increased by one and counter is as well increased by one. The shifter shift the bit to left position and the temporary register read the next bit in next clock cycle. If the bit is one then the multiplexer input 0 is added with constant value one and the output shifts to valid and set the valid as one and the position output is the position value store in the position temporary register. This operation is carried on up to discover the one in the temporary register. Pseudo code for position control unit:

- Step 1: Read the most signifiant bit from temporary register
- Step 2: Check whether the bit is zero or one
- Step 3: If bit = 0, Position = position +1
- Step 4:Temporary register left shift by one
- Step 5: Got to step 1
- Step 6: If bit = 1, Valid = 1
- Step 7: Read position
- Step 8: Stop

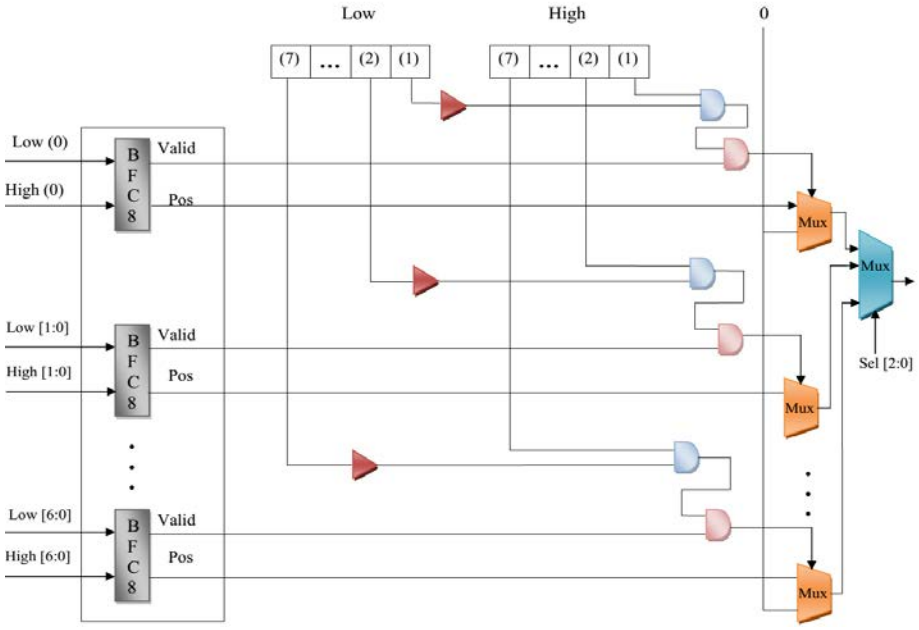

Fig. 12: Internal structure of bit follow check array

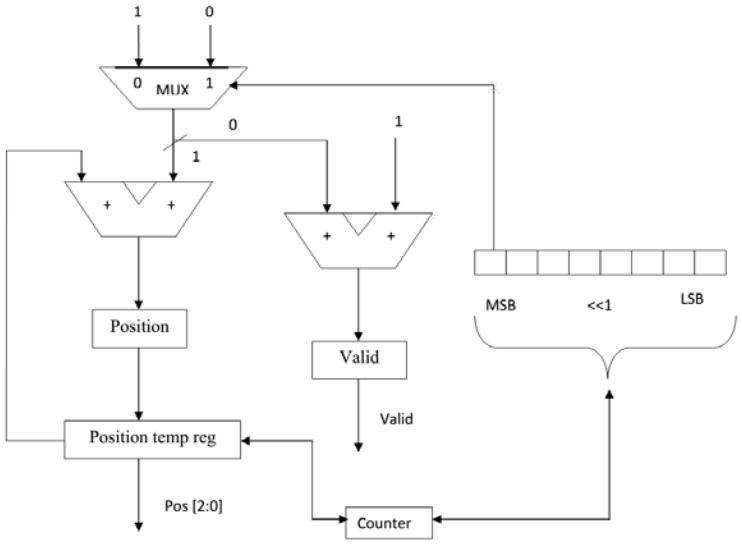

Fig. 13: Proposed architecture of Position control unit

Figure 13 demonstrates the clear explanation of position control unit. The consumption of area is enhanced and its performance is enhanced by applying the position control unit in the arithmetic coder. According to pos [2:0], the output from the leading bit check selects the bit value. The high register and low register value are moved according to the LBC and BFC values. The shifted value is next fed to low and high update calculation. The final bit value from the low register file is then given to code stream to assemble the bit in series to form a codeword.

RESULTS AND DISCUSSION

The experimental results of Image compression of an efficient 2D DWT-A distributed arithmetic with rapid arithmetic coder method are explained below. The design is simulated and synthesized using Xilinx 14.1 Vertex-5. The RTL schematic of efficient 2D DWT-A with rapid arithmetic coder is shown in Fig. 14.

Compression evaluation: Image compression is to reduce the bit size of an image by removing the spatial and

Table 1: Comparison of MSE

Method	Context based (Ansari and Anand, 2008)	Distributive arithmetic based DWT (Nagabushanam *et al*., 2001)	Proposed method
MSE	200.5	194	210

Table 2: Comparison of PSNR results

Method	EZW (Criminisi *et al*., 2004)	SPHIT (Hontsch and Karam, 2000)	2D Discrete Walsh Wavelet (Malviya *et al*., 2013)	Proposed method
PSNR	30.23	31.1	30.88	57.36

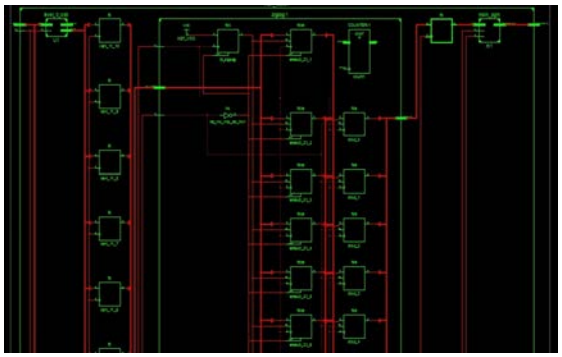

Fig. 14: RTL schematic of efficient 2D DWT-DA with rapid arithmetic coder

spectral redundancies as much as possible. For comparison of an image quality, a general evaluation tool, MSE, PSNR and compression ratio have been adopted.

MSE: The mean square error is a commonly used measure the variation between original image data and compressed image data.

$$MSE = \left[\frac{1}{mn} \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} (I_{i,j} - Q_{i,j})^2 \right] \quad (4)$$

Where:

$I_{i,j}$ = Original image data

$Q_{i,j}$ = Compressed image data

The value of MSE obtained is compared with other methods are tabulate in Table 1. Table 1 shows the MSE value of different method.

PSNR: Peak signal to noise ratio used to be a measure of image quality, the measure closeness with PSNR want to be high PSNR value.

$$PSNR = 20\log_{10}\left(\frac{MAXI}{MSE}\right) \quad (5)$$

The PSNR value obtained from the method is compared with other methods (Hontsch and Karam, 2000; Malviya *et al*., 2013), the comparison Table 2 is shown.

Table 2 shows that the method we implement gives better PSNR value that (Hontsch and Karam, 2000; Malviya *et al*., 2013) methods. The above values are plot in Fig. 15. Figure 15 shows that the PSNR value of the 2D DWT-A DA with rapid arithmetic coder is increased when compared to the conventional methods. Higher PSNR value indicates that the reconstruction of image is of higher quality.

Table 3: Different images comparison

Images	PSNR	RMSE	MSE	CR
CT	57.36	14.48	210.00	3.490
MRI	51.60	19.33	373.48	2.714
X-ray	53.40	17.65	311.63	3.950
Nuclear	56.86	14.85	220.54	2.780
PET	53.24	17.79	316.63	3.430

Table 4: The Xpower analyzer report for proposed method

Supply source	Voltage summary	Dynamic current (A)	Quiescent current (A)	Total current (A)
Vccint	1.0	0.049	0.236	0.285
Vccaux	2.5	0.000	0.032	0.032
Vcco25	2.5	0.001	0.002	0.003
Supply power (W)	-	0.051	0.321	0.372

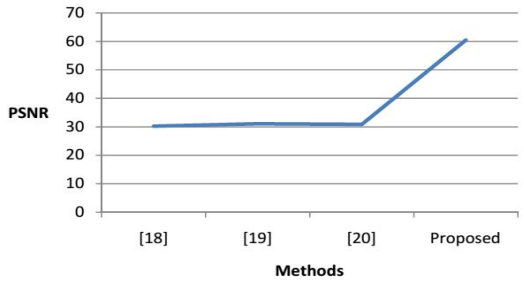

Fig. 15: PSNR comparison

Compression Ratio (CR): Compression ratio is the ratio between uncompressed size and compressed size

$$\text{Compression ratio} = \frac{\text{Uncompressed size}}{\text{Compressed size}} \quad (6)$$

Here, we compare the results with different types of images like CT, MRI, X-ray, Nuclear medicine, PET. Table 3 shows the comparison result of different images.

Power: The Xpower analyzer report is shown in Table 4. The dynamic power consumed by our method is 0.051 W and quiescent power is 0.321 W. Hence, the total power consumed in low power DWT image fusion method is

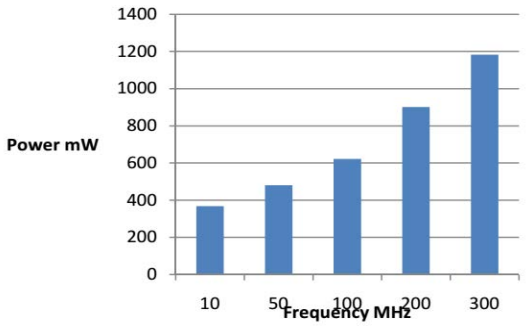

Fig. 16: Power vs frequency

Table 5: Power variation according to frequency

Frequency (MHz)	Power (mW)
10	368
50	481
100	622
200	902
300	1182

Table 6: The device utilization summary for our proposed image fusion method

Slice logic utilization	Used	Available	Utilization (%)	Note(s)
No. of slice register	1784	12480	14	
No. used flip flops	1775			
No. used flip Latches	7			
No. used as latch-thrus	2			
No. of slice LUTs	11079	12480	88	
No. used as logic	10952	12480	87	
No. using O6 output only	9386			
No. using O5 output only	40			
No. using O5 and O6	1526			
No. used as memory	106	3360	3	
No. used as shift register	106			
No. using O6 output only	106			
No. used as exclusive route-thru	21			
No. of route-thrus	147			
No. using O6 output only	51			
No. using O5 output only	92			
No. using O5 and O6	4			
No. of occupied slices	3026	3120	96	

0.372 W. Here, the value of power is take by the use Xilinx 14.1 Vertex-5. The power can be varied at different frequency that can be shown in Table 5 and Fig. 16. From Fig. 16, it shows that the power will be increases when the frequency is increases.

Area: Table 6 shows the device utilization summary for our proposed image fusion method. The proposed design utilizes 1,784 among the available 12,480 Slice Flip-flops which utilizes about 14% of the available resources and utilizes 11,079 input LUT's among the available 12,480 thereby utilizing about 88% of the resources. About 3,026 out of 3,120 available slices are occupied by our proposed design utilizing about 96% of available slices.

CONCLUSION

The alternate medical image compression methodological approaches presented in this paper, based on the 2D DWT-A distributed arithmetic with rapid arithmetic coder, allow compressing the images of better compression ratio. The implemented position control unit in the method used to reduce the area of the arithmetic coder architecture. Comparative measure is done on the basis of two parameters MSE and PSNR. It is found that PSNR value is in improvement of 51.81% and the MSE value is in improvement of 77.76% which were more enhanced than other traditional method. The result shows that we can achieve higher compression ratio for medical images. Our system when coded synthesized and simulated in Xilinx 14.1 Vertex-5. These results showed that, 2D DWT-A distributed arithmetic with rapid arithmetic coder method was improved. The maximum power utilized in the method for image compression was 368mW at 10 MHz frequency.

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