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NoC Architecture: A Closer Look

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Abstract: Network on Chip (NoC) is a communication framework for on-chip network. NoC has implemented the concept of packet switching from data communication in on-chip network. NoC consists of multiple nodes Processing Elements (PEs) connected together through routers. Routers are in turns connected together through bidirectional interconnects. NI connects the PEs to routers as it separates the data communication of PE from network communication.

Key words: Network on Chip (NoC), clocking mechanism, evaluation parameters, open source, implementation, NoC size

INTRODUCTION

NoC is a new solution for interconnection of Processing Elements (Pes) in System on Chip (SoC). NoC brings notable improvements over conventional bus. It has solved the delayed communication, congestion and higher latency problems. In this study, we are reviewing NoC architectures based on the different parameters which are: NoC clocking mechanism, evaluation parameters, topology, open source, implementation, NoC size, area, power dissipation/energy consumption, buffering and NoC routing algorithms.

NoC clocking mechanism: Communication between router, NI and PE is mostly asynchronous, synchronous, Globally Asynchronous and Locally Synchronous (GALS), mesochronous, plesichronous and heterochronous. According to literature search of the NoC architectures 29, 25, 13 and 5% of NoC architecture have synchronous, asynchronous, GALS and mesochronous clocking mechanism as shown in Fig. 1. While only a single architecture uses plesichronous clocking mechanism. These trends show that the NoC architectures are moving from synchronous communication to asynchronous communication. The reason is that asynchronous communication is faster and data/activity dependent, exploiting average case rather than worst case performance (Amde *et al*., 2005; Itzhak *et al*., 2012; Emerson, 1997). Designing

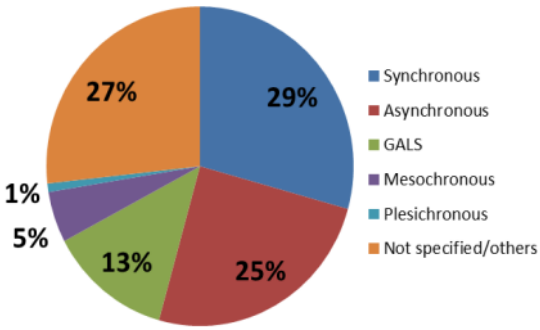

Fig. 1: Clocking mechanism

Asynchronous NoC is modular but it is more complex compared to synchronous NoC (Emerson, 1997). Designing a glitch free circuit which at the same time manages multiple clocks is more difficult to manage than global clock based communication. Therefore, scientists and researchers combined the idea of synchronous and asynchronous NoC communication by having GALS architecture. GALS architecture solves the timing issues in multiple PEs in a NoC because local synchronous PEs need not to synchronize with a single global clock. GALS approach consumes less power as compared to global clock approach as local PEs have more control over their clock independent from other synchronous PEs (Agarwal *et al*., 2009a). It depends on the applications requirements mapped on the NoC that whether synchronous, asynchronous or GALS architecture will support it and will increase the performance of the NoC. The clock frequency of the NoC architectures is measure

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in Hertz (Hz). The scale of the frequency used by the NoC architectures is Mega (M) and Giga (G) hertz.

Synchronous NoC: In synchronous NoC all network is connected with a single clock. The activities are synchronized based on this clock. The benefit of synchronous communication are that all the changes at the routers, PE and links occur at the same time at regular clock period. Synchronous circuits have the problem of clock skew, lack of modularity, electromagnetic interference noise, worst case performance and clock power consumption issues (Amde *et al*., 2005).

Examples of synchronous NoC are Dally *et al* (Dally and Towles, 2001), SPIN (Guerrier and Greiner, 2000), aSOC (Liang *et al*., 2000), ethereal (Rijpkema *et al*., 2003), OCN (Henriksson *et al*., 2003), Nostrum (Penolazzi and Jantsch, 2006; Millberg *et al*., 2004), Xpipes (Bertozzi and Benini, 2004), A 0.13 μm NoC (Mondinelli *et al*., 2004), RaSoC (Zeferino *et al*., 2004), QNoC (Bolotin *et al*., 2004), reconfigurable network on chip (Ching *et al*., 2005), a routing switch for on chip interconnection networks (Chi and Chen, 2004), spatial division multiplexing NoC (Leroy *et al*., 2005), CDMA router for on-chip switched networks (Kim *et al*., 2005), high throughput NoC architecture (Bouhraoua and Elrabaa, 2006), PnoC (Hilton and Nelson, 2006), CTNOC (Wang *et al*., 2006), low latency on chip network on chip multimedia applications (Lee *et al*., 2006a), NocMaker (Rufas *et al*., 2006), TILEPro64 (Bell *et al*., 2008), UT TRIPS (Gratz *et al*., 2007), Ambric (Butts, 2007), Polaris (Soteriou *et al*., 2007), TTNoC (Paukovits and Kopetz, 2008), ReNoC (Stensgaard and Sparso, 2008), XhiNoC (Samman *et al*., 2009), network on chip in a three dimensional (Feero and Pande, 2009), BiNoC (Lan *et al*., 2011), PMCNOC (Wang *et al*., 2010), WiNoC (Ganguly *et al*., 2011), dAElite (Stefan *et al*., 2014), Aurora (Qouneh *et al*., 2012), RecMIN (Logvinenko *et al*., 2013), SWIFT (Postman *et al*., 2013) and TagNoC (Yaghini *et al*., 2015).

Asynchronous NoC: In asynchronous NoC activities are performed based on the handshake (control) signals shared between routers (Amde *et al*., 2005; Bjerregaard and Mahadevan, 2006; Yaghini *et al*., 2015). Asynchronous NoC are also called self-timed NoC (Bainbridge and Furber, 2002). Asynchronous circuit implementation usually takes more area, delay, power consumption and consumes channel bandwidth as compared to synchronous approach because of explicit sharing of signals (Amde *et al*., 2005). It is not easy to resynchronize the asynchronous communication. The resynchronization introduces error bits and increase the latency and power consumption (Bjerregaard and Mahadevan, 2006). The asynchronous communication is faster as compared to synchronous communication at high traffic loads as it has the least latency (Bjerregaard and Mahadevan, 2006; Itzhak *et al*., 2012). In asynchronous NoC there can be no timing relationship between synchronous clocks (Pes). Asynchronous provides the maximum flexibility in terms of timings (Teehan *et al*., 2007). When interconnects are idle, apart from the leakage, no power is consumed in asynchronous NoC. This solves the problem of increasing power consumption as the chip size is increased (Bjerregaard and Mahadevan, 2006).

CHAIN (Bainbridge and Furber, 2002), ethereal (Rijpkema *et al*., 2003), HERMES (Moraes *et al*., 2004), BIDI-MIN (Pande *et al*., 2003), SoCIN (Zeferino and Susin, 2003), R^2NoC (Samuelsson and Kumar, 2004), Fspider (Evain *et al*., 2004), Spidergon (Coppola *et al*., 2004), asynchronous on chip network router with quality of service (Feliciian and Furber, 2004), Mango (Bjerregaard and Sparso, 2005a, b; Wolkotte *et al*., 2005), ASPIDA (Amde *et al*., 2005), topology adaptive NoC (Bartic *et al*., 2005), asynchronous NoC architecture (Beigne *et al*., 2005), cross road interconnection architecture (Chang *et al*., 2006), SCC (Hoffman *et al*., 2007), a reconfigurable baseband platform based on asynchronous NoC (Paukovits and Kopetz, 2008), EVC (Kumar *et al*., 2008), HT-OCTAGON DRNoC (Krasteva *et al*., 2010), dynamic reconfigurable network on chip (Wu *et al*., 2011), Ramos (Pena and Michel, 2011), BMNoC (Lee *et al*., 2012), Custom Network on Chip architecture (Mishra *et al*., 2012), DANoC (Shu *et al*., 2012), AdNoC (Al Faruque *et al*., 2012) and mesh based NoC (Choudhary and Qureshi, 2012) are asynchronous NoCs.

Globally Asynchronous Locally Synchronous (GALS): In the Globally Asynchronous Locally Synchronous (GALS) approach the NoC is divided among multiple sub systems. Each sub-system has its own clock and they communicate with other system through asynchronous NoC communication. GALS have less power consumption as compared to having a global clock. It avoids the problem of clock synchronization due to clock skew as more and more devices are coming on the chip (Amde *et al*., 2005; Teehan *et al*., 2007; Tortosa *et al*., 2004). Figure 2 shows the GALS architecture where independent synchronous islands of systems are connected with asynchronous NoC through irregular topology.

CLICHE (Kumar *et al*., 2002), PROTEO, Nexus (Lines, 2004), an architecture and compiler for aSoC

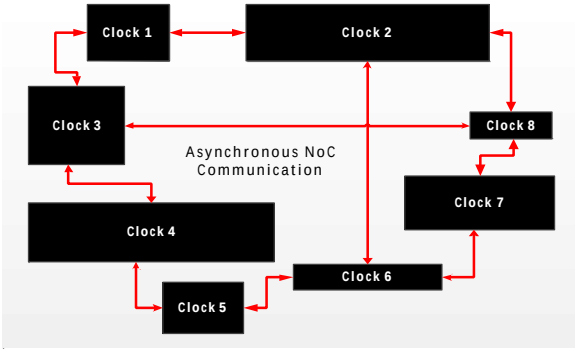

Fig. 2: GALS clocking scheme

(Liang *et al*., 2004), on-chip network for low power heterogeneous SoC platform (Kangmin *et al*., 2004), Arteris, ProtoNoC (Rufas *et al*., 2006), TTNoC (Schoeberl, 2007), MoCRes (Janarthanan *et al*., 2007), CDMA NoC (Wang *et al*., 2007), MoCSYS (Janarthanan and Tomko, 2008), Aelite (Hansson *et al*., 2009), ALPIN (Beigne *et al*., 2009), RAMPSoC (Gohringer *et al*., 2010) and WaveSync (Yang *et al*., 2014) are following GALS approach.

Mesochronous: Due to clock skew concept a new clocking scheme called mesochronous is used. In this scheme all the subsystems have different clocks with the same frequency but the phase is different (Wiklund and Liu, 2003). Ethereal (Rijpkema *et al*., 2003), SoCBUS (Wiklund and Liu, 2003), adaptive network on chip (Lee *et al*., 2005), DSPIN (Panades *et al*., 2006), low-power network on chip (Lee *et al*., 2006b) and Intel TeraFLOPS (Vangal *et al*., 2008) are examples of mesochronous links.

Plesichronous NoC: In plesichronous NoC, the source and destination PE operate at the nominal frequency which may be slightly different and this leads to drifting phase (Teehan *et al*., 2007). The Star Connected OCN (Lee *et al*., 2003) is a plesichronous NoC.

Heterochronous NoC: In a heterochronous NoC, source and destination have totally different clock frequencies (Teehan *et al*., 2007).

Evaluation parameters: The NoC architectures are evaluated based on various parameters. These parameters include latency, throughput, bandwidth utilization, area, power dissipation, energy consumption, etc. Every NoC architecture tries to maximize the throughput and bandwidth utilization while minimize latency, area, power and energy dissipation using varrious techniques. Latency refers to the time taken by a packet or flitlatency is measured in nano seconds (ns). Throughput is the number of bits that can be sent across the NoC interconnect (link) per second. Throughput is measured in bits per second (bps). Bandwidth is the maximum number of bits that can be sent over a interconnect (link) per second. The unit of bandwidth is bits per second (bps). Area refers to the size of NoC after synthesis. Now a days there are also some software tools available which can be used to measure the area and power consumption of the NoC architecture. The unit of area used by most of the architecture is mm^2. The units of power and energy consumption used by the architectures are milli-Watt (mW) and petajoule (pJ), respectively. When packets traverses the router and interconnects it consumes power and energy. These parameters are very important to calculate as more and more heterogeneous devises (PEs) are coming onto chips. They increase the power, energy and area consumption of the chip.

Topology: The topology of the NoC defines how the PEs, routers and links are connected with each other in the network. The selection of the particular topology for any specific NoC depends on the communication usage of the PE's. Other factors in choosing a specific topology for any NoC design include its impact on performance and cost parameters. The performance parameters include latency, fault tolerance, bandwidth and throughput while cost parameters include area and power/energy consumption (Ogras *et al*., 2005). Many different topologies have been proposed (Wang *et al*., 2011). There are broadly two categories of topologies, regular and irregular topologies. In regular topologies routers and PEs are connected according to some pattern, e.g., mesh, torus, fat tree, butterfly fat tree, octagon, star, hierarchical star, crossbar, ring, spidergon, chain, subnets, generalized de bruijin topology. While, there is no common pattern in irregular topology which may include hybridize topologies. Although, regular NoC topologies are simple to implement, at times they have the drawback being non-optimal in terms of network utilization. The low network utilization leads to delayed communication and increased power consumption. In order to overcome these drawbacks scientists come up with the concept of irregular topologies. Irregular or custom NoC topologies are application specific and mostly have heterogeneous PE's, routers as compared to regular NoC topologies (Tatas *et al*., 2014). Regular topologies make the routing decision simple and it is easily replicated on multiple

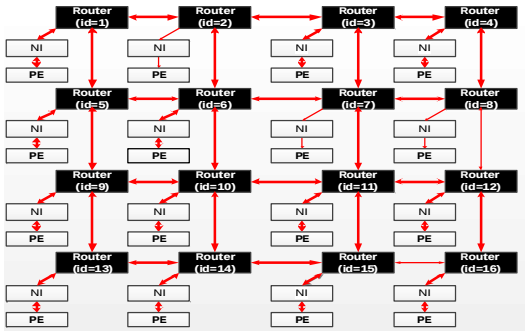

Fig. 3: Mesh topology

nodes while irregular topologies make the routing algorithm more complex (Guerrier and Greiner, 2000).

In the mesh topology, the routers are connected with each other through point to point connection in a mesh structure as shown in Fig. 3. The routers at the first and last column or row of NoC are not connected with any other neighbour routers. Most of the NoC architectures have mesh topology because its communication structure is less complex and it is also similar to 2D silicon surface (Teehan *et al*., 2007; Seifi and Eshghi, 2012). One of the drawbacks of the mesh topology is congestion at the center of the NoC due to the routing algorithm. In mesh topology, routing algorithm should have equal and balance traffic distribution mechanism.

The torus topology is similar to mesh except that the first and last column or row elements are also connected with each other. Torus increases and eases the routing decisions Torus topology solves the excessive round end trip delays as they are connected together. The drawback of the torus topology is more area and links requirement than mesh NoC (Wang *et al*., 2011). In tree structure topologies the routers are connected in a hierarchical design such that the parent's routers have child routers connected with them. The tree topology is hierarchical in structure but becomes complex as more PE's are connected at the leaf routers (Guerrier and Greiner, 2000). In the tree base topology the traffic can be easily disseminated to the desire destination due to hierarchical structure (Bjerregaard and Mahadevan, 2006). In star topology, the routers are connected with the centralized arbiter. The arbiter manages the communication between multiple routers. The arbiter may be a specialized device or it can be a router as well (Lee *et al*., 2003). The capacity of the centralized arbiter/router should be large to manage the traffic received from multiple PE's connected to it. This at times also leads to congestion at the centralized switch.

In the octagon topology, the eight routers are connected in a ring fashion with bidirectional wires (Karim *et al*., 2002). Octagon topology is simple to implement. Fast and efficient routing algorithm can be implemented using this topology. Excessive wiring is required in order to extend the octagon network to more than eight Pes. In crossbar topology the router are connected with a number of wires connected in a crossbar fashion. This topology is simple to implement but the links between PEs become complex and large as more and more PE's are connected through crossbar interconnection (Lines, 2004). Ring topology refers to the nodes connected in a ring (Samuelsson and Kumar, 2004). That is all routers are connected with each other through interconnects in a ring shape. Although, ring topology is simple to implement but it have limited scalability and performance problem as the number of nodes are increased. In the spidergon topology, number of nodes (>2) is connected together in a bidirectional ring in both clockwise and anti-clock wise direction. So, the nodes in spidergon is also connected with the cross connection. Spidergon topology is similar to spider web. This topology is regular, scalable, point-to-point and has good network diameter. The network becomes complex as the number of PEs are increased (Coppola *et al*., 2004). In the subnet topology, there are small groups of PEs connected with the router. This group is called subnet. These subnets are in return connected with each other. The PEs which communicates oftenly are put in the same subnet. This makes the communication between PEs more efficient. The communication between PE in different subnets takes more time for communication which may leads to delayed communication (Hilton and Nelson, 2006). In de bruijin topology the nodes are connected through vertices and it can be an irregular topology (Soteriou *et al*., 2007). It is an efficient topology for parallel processing and is also suitable for VLSI implementation. The two dimensional de bruijin NoC is performing better as compared to two dimensional mesh topology in terms of latency and energy dissipation. At times, in two dimensional de bruijin NoC it takes longer links to connect the neighbour node as compared to two dimensional meshes, this increases the network area.

Open source: The open source software/architecture has a license which allows the end user to have access to the source code, redistribute the software/architecture and modify the original code with the same license. At times, the license may have special provision to be met specifically. For example, the derived

software/architecture should use its own name and version apart from mentioning the original software/architecture name. Open source architectures and codes are usually provided for academic and research purposes. They are mostly not allowed to be used for commercial purpose. Ethereal (Rijpkema *et al*., 2003), Aelite (Hansson *et al*., 2009) and dAElite (Stefan *et al*., 2014) architectures are not open source while Nostrum (Penolazzi and Jantsch, 2006; Millberg *et al*., 2004) is provided on request. Reconfigurable Network on Chip (Ching *et al*., 2005) and NocMaker (Rufas *et al*., 2006) are open source architectures. Other NoC architectures have not mentioned any information regarding it.

Implementation: The NoC architectures are implemented on simulator, Field Programmable Gate Array (FPGA) (Shanthi, 2014) and as Application Specific Integrated Circuits (ASIC). Some of the architectures are synthesized using a cycle accurate simulator. The simulators used are HNOCS (Itzhak *et al*., 2012), OMNET++(Varga and Hornig, 2008), NS-2, OPNET (Modeler, 2009), Noxim (Palesi *et al*., 2010), Nirgam, Simics (River, 2006), Garnet (Agarwal *et al*., 2009b), Orion (Wang *et al*., 2007, 2010, 2011), Spice (Franco *et al*., 2015), Recsim (Logvinenko and Tutsch, 2012) and CACTI (Muralimanohar *et al*., 2007).

NoC size: NoC architectures have used various NoC sizes for implementation purpose. These sizes include 2×2, 3×3, 4×4, 5×5, 6×6, 7×7, 8×8, 5×8, 2×3, 4×3 having two dimensional mesh and torus topologies. Some of the NoC topologies were regular while others were irregular.

Area: Some of the papers mentioned the area of the complete NoC architecture while few specified the router or switch area. The area is usually measured as the total number of look up tables or slices used in FPGA or the number of gates/transistors/flip flops/logic cells used in the NoC architecture. The area of the router and NoC architectures are also mentioned in mm^2, μm^2 units. In embedded systems, area and power consumption of the devices are very much important.

Power dissipation/energy consumption: This is a very important parameter of NoC architectures. Scientists and researchers are finding techniques to efficiently utilize the power and energy consumption of the NoC. The NoC clocking mechanism, buffer management, routing algorithms and switching activities consumes power and energy on a per router and interconnect basis. The units used for power dissipation are μW (micro-Watt), mW (milli-Watt) and MW (Mega-Watt) while the units used for energy consumption is pj (peta-joule) and pj/packet (peta-joule per packet).

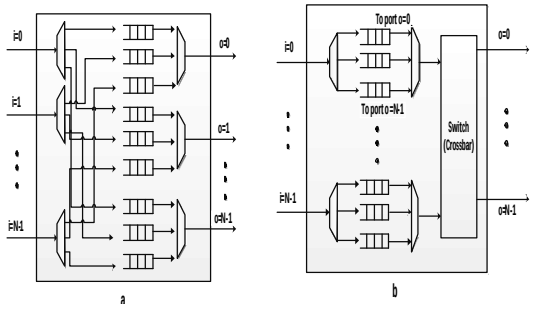

Fig. 4: Output queue and VOQ router architecture

Buffering: Buffer is the integral part of any network router (Bjerregaard and Mahadevan, 2006) but they consume a lot of power in NoC. Therefore, efficient buffer design is very important for optimized NoC performance. The buffer design includes the location and size of the buffer (Bjerregaard and Mahadevan, 2006). To minimize the access latency and implementation cost, it is always preferred to use registers rather than huge memories in the form of SRAM or DRAM (Hu and Marculescu, 2003). The location of the buffers can be at the input or output port of the router. These buffers are called as the input queue and output queue. The performance of the output buffering is the best as compared to other strategies but at the cost of more loads on interconnects. When to read the flits from input or output queue depends on the scheduler which in turns checks the output port that whether it is free. Usually router used to have one queue per port but due the HOL problem now they have more than one queue per port for every connection. The Virtual Output Queue (VOQ) is one type of input buffering which has the combined benefits of input and output queuing (Rijpkema *et al*., 2003). The input queues may have less memory cost as they have fewer queues as compared to VOQ and output buffers techniques (Radulescu and Goossens, 2004). Input queues also solve the problem of HOL as the output queues may be blocked due to congestion or faulty interconnects (Bjerregaard and Mahadevan, 2006). Figure 4 shows the output and virtual output queue architectures of routers.

According to the literature search, 28% of NoC architectures are using input queues while 20% of architectures are using input and output queues together. 5% of architectures are using only output queues while only two architectures are using VOQ's as shown in

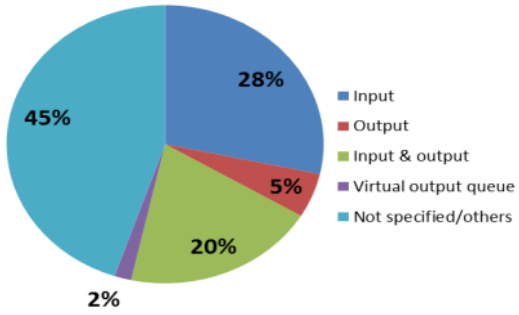

Fig. 5: Buffering

Fig. 5. This shows the trend that most of the scientists preferred input and combination of input and output buffers because of better link utilization and performance.

The area of the NoC increases directly as the size of the input buffers is increased. Ogras *et al.* (2005), it is mentioned that the 4×4 NoC area increases by 30% as the input buffer size are increased from 2-3 words. But at certain times, depending on the network load the network latency is reduced a considerable amount by increasing the buffer size. However, due to heterogeneous traffic generated by PEs in NoC, it is always desirable to allocate more buffers for high traffic channels while small number of buffers can be allocated to low traffic channels.

OCTAGON (Karim *et al.*, 2002), CLICHE (Kumar *et al.*, 2002), ethereal (Rijpkema *et al.*, 2003), HERMES (Moraes *et al.*, 2004), SoCIN (Zeferino and Susin, 2003), µSpider (Evain *et al.*, 2004), RaSoC (Zeferino *et al.*, 2004), QNoC (Bolotin *et al.*, 2004), reconfigurable network on chip (Ching *et al.*, 2005), DyAD (Hu and Marculescu, 2004), a routing switch for on chip interconnection networks (Chi and Chen, 2004), asynchronous on chip network router with quality of service (Feliciian and Furber, 2004; Kavaldjiev *et al.*, 2006), INoC (Neeb and Wehn, 2008), CTNOC (Wang *et al.*, 2006), low latency on chip network (Mullins *et al.*, 2006), low-power network on chip (Lee *et al.*, 2006b), intel teraFLOPS (Vangal *et al.*, 2008), EVC (Kumar *et al.*, 2008), ReNoC (Stensgaard and Sparso, 2008), Aelite (Hansson *et al.*, 2009), XhiNoC (Samman *et al.*, 2009), BiNoC (Lan *et al.*, 2011), DRNoC (Krasteva *et al.*, 2010), PMCNOC (Wang *et al.*, 2010), dynamic reconfigurable network on chip (Wu *et al.*, 2011), Kilo-NoC (Grot *et al.*, 2011), BMNoC (Lee *et al.*, 2012), DANoC (Shu *et al.*, 2012), WaveSync (Yang *et al.*, 2014), RecMIN (Logvinenko *et al.*, 2013), SWIFT (Postman *et al.*, 2013) and BLOCON (Kao and Chao, 2014) have the input queues at the router port.

These are the NoC architectures having output queues at the router port; RAW (Taylor *et al.*, 2002), Eclipse (Forsell, 2002), Xpipes (Bertozzi and Benini, 2004), Mango (Bjerregaard and Sparso, 2005, 2004a, b), topology adaptive NoC (Bartic *et al.*, 2005) and on chip multimedia applications (Lee *et al.*, 2006a).

The NoC architectures which are supporting input and output queues are; SPIN (Guerrier and Greiner, 2000), aSOC (Liang *et al.*, 2000), Dally *et al* (Dally and Towles, 2001), micronetwork (Wingard, 2001), PROTEO, BIDI-MIN (Pande *et al.*, 2003), Nostrum (Penolazzi and Jantsch, 2006; Millberg *et al.*, 2004), A 0.13 µm NoC (Mondinelli *et al.*, 2004), NoCGen (Chan and Parameswaran, 2004), CDMA router for on-chip switched networks (Kim *et al.*, 2005), DSPIN (Panades *et al.*, 2006), XGFT (Kariniemi and Nurmi, 2006), PnoC (Hilton and Nelson, 2006), HIBI (Salminen *et al.*, 2006), TILEPro64 (Bell *et al.*, 2008), UT TRIPS (Gratz *et al.*, 2007), Ambric (Butts, 2007), Generalized de Bruijn Graph NoC (Hosseinabady *et al.*, 2007), HT-OCTAGON, ALPIN (Beigne *et al.*, 2009), dAElite (Stefan *et al.*, 2014), AdNoC (Faruque *et al.*, 2012) and HELIX (Bahirat and Pasricha, 2014). ArtNoC (Schuck *et al.*, 2007) and BLOCON (Kao and Chao, 2014) NoC architectures have VOQ.

NoC routing algorithms: There are five broad categories of routing algorithms which are deterministic, stochastic, fully adaptive, partial adaptive and bio-inspired routing algorithms. Detail about these routing algorithms can be found in Sethi *et al.* (2013a, b, 2014, 2016a, b)

CONCLUSSION

In this study, we are looking and reviewing NoC architectures based on different aspects.

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