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Leakage Current Minimization in Footerless Domino Logic Circuits Using Stalk Technique

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Abstract: IC technology demands high performance, low power consuming, miniature sized devices. Minimizing the device size drastically increases the power consumption and hence the need for innovative techniques to reduce the power consumption are in the bloom. The approach accorded here is the combined implementation of leakage controlled transistors in the path between power supply and ground and stacking of transistors in the pull down network. The above approach is implemented in Domino logic circuits which are often claimed as leaky circuits. Results show reduction in leakage current, total power consumption with an admissible increase in transistor count and overall delay.

Key words: Domino logic circuits, leakage current, stacking, power consumption and leakage controlled transistors

INTRODUCTION

The innovations in CMOS technology have made it superior to other technologies in the field of integrated circuits. CMOS has occupied a vast market space due to its aggressive scaling down of device dimensions, reduced power consumption and scaling up of switching speed. The abrupt scaling down of device dimensions had reached nanometer range, whereas the supply voltage had dropped below one volt (Moore, 1998). This exponential growth has made CMOS technology enter in to microwatt application devices like microsensors, implantable biomedical devices, handheld devices, etc (Wang *et al*., 2015). Power dissipation is a critical factor of concern in nanometer so called ultra deep submicron range devices. Power dissipation is categorized into static power dissipation and dynamic power dissipation. Static power dissipation usually occurs when the device is in idle state. The main contributors to static power dissipation are subthreshold current and various leakage currents (Panda *et al*., 2010). Dynamic power dissipation occurs due to the frequent charging and discharging of parasitic capacitances of the device. In submicron range devices, dynamic power dissipation dominates static power dissipation. In nanometer range technologies, static power dissipation increases more significantly than dynamic power dissipation (Damle *et al*., 2013). Sub threshold leakage occurs due to the flow of current from drain to source when the applied gate source voltage is lesser than the threshold voltage of the device. Subthreshold leakage occurs due to weak inversion, drain induced barrier lowering and drain punch through. (Moore, 1998; Pierret, 1996). Device performance is influenced significantly by the supply voltage and delay metrics. Careful choice of device integration and fabrication is required to reduce the supply voltage below a single volt. Delay should be carefully designed to avoid unwanted errors. Aimed at reducing power consumption, sub threshold leakage and delay, a new work is proposed and simulated with its implication in Domino logic circuits. Domino logic circuits which are generally termed as leaky circuits are classified in to Footed and Footerless domino logic circuits (Mangalam and Gunavathi, 2007). The proposed technique uses Footerless domino logic circuits where the evaluation transistor is eliminated.

Critical paths determine the efficiency of operations in most microprocessors, application specific integrated circuits, microprocessors, system on chips, etc. The critical path is occupied mostly by comparators, adders and multipliers. Binary addition is an elementary level operation of most arithmetic components and adders become the fundamental component of the processors. In addition to adding two numbers, an adder participates in other applications like subtraction, multiplication, division, etc. The conventional 28 transistor full adders occupies significantly more area and consumes more power and produces more delay in the circuit. Trending low power applications require circuits with low power

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consumption as well as dissipation with considerable reduction in occupying space. The proposed technique is implemented in full adder circuit, its performance evaluated and performance up gradation in terms of power consumption and subthreshold leakage current is obtained.

Designs and techniques: Various existing design techniques leading to reduced leakage current are discussed. Integrated circuit based on CMOS technology will be used in almost all fields. Scaling down device dimensions will help device switch faster (Moore, 1998). Leakage current increases exponentially as supply voltage and threshold voltage are scaled down. Multiple supply voltage technique is a technique that uses higher VDD to the circuit in the critical path and lower VDD to the circuit in the non critical path. The slack feature in the circuit is utilized to reduce power consumption (Moore, 1998). Multiple threshold voltage is a technique to reduce subthreshold leakage current. It uses low Devices in the circuit paths with high speed and high devices in other paths (Moore, 1998). Adaptive body biasing is yet another technique to reduce subthreshold leakage current. Power gating is an efficient technique that minimizes leakage current by selectively turning off the device blocks that are not active by using sleep transistors. Domino logic offers higher speed and uses reduced transistor count. Stacked transistor dual threshold voltage is a technique proposed to decrease the power dissipation along with reduced power delay product (Sethi *et al*., 2013). A new leakage tolerant, high speed domino logic circuit with diminished power dissipation and increased speed proposed. This technique uses a small keeper transistor to reduce power dissipation significantly. A comparison between static CMOS logic circuits and domino logic done which proved that domino logic circuits offer better.

Performance in both speed and power consumption than static CMOS circuits. Hence, domino logic circuits are widely used in low power circuit design despite of its leakage current (Govindarajalu and Parasad, 2010).

MATERIALS AND METHODS

A number of techniques have been introduced to reduce subthreshold leakage current and hence power consumption. The device area are being scaled down in regard to technology which in turn shoots up the power consumption. Hence, the need for better leakage reduction techniques are always in demand. Rather than implementing a single technique to reduce the amount of power consumption, combining two or more leakage current reduction techniques to reduce leakage current provides effective power saving (Rahmani *et al*., 2006). With strict adherence to this principle, a novel work is proposed by combining Leakage Controlled Transistors and the traditional stacking technique. As subthreshold leakage current is the dominant one among the various leakage currents, it is in prime focus. Subthreshold leakage occurs when the transistor is in cut off state.

The leakage controlled transistor design is done in such a way that it contains a single NMOS and a single PMOS transistor. The two transistors are connected in such a way that the gate of these two transistors are controlled by the source of the other transistor. Thus, for any input vector combination, one of LCT transistor will be operating around its cutoff region. This inturn shoots up the effective resistance between the power supply and ground rails and hence provide significant reduction in leakage current (Gupta and Khare, 2013). Stacking is yet another efficient technique to reduce leakage current. In stacking, a single transistor is replaced by two transistors of the same kind connected in series with its width made half of the single transistor. The ratios of both of the transistors are adjusted such that there is no area sacrifice. Thus, an intermediary node is formed between the two transistors. When both the transistors are in off-state due to the small drain current, this intermediate node will be positive. Because of the Intermediate node becoming positive, the gate-source voltage of the first transistor will be positive. As the voltage of the intermediary node is greater than zero, body-source potential of the first transistor will be negative and the drain-source potential will decrease. The above three factors lead to the increase in the threshold voltage and decrease in the sub-threshold leakage current. These two techniques are combined together and implemented in footerless domino circuits to reduce leakage and hence power consumption (Wang *et al*., 2004).

The proposed technique which combines both leakage controlled transistors and stacking is hence forth referred as STALK technique. The working of the proposed STALK based domino circuit in non-ideal mode and ideal mode is as follows: When the applied clock pulse is low or during non-ideal mode the dynamic node gets charged high via MP1 and MP4. The charging of dynamic node is almost independent of the previous clock input state. In case, if the input signals are low before the clock sets low then node N2 will be at low potential and transistor MP4 offers the less resistance path for charging of the dynamic node (Fig. 1).

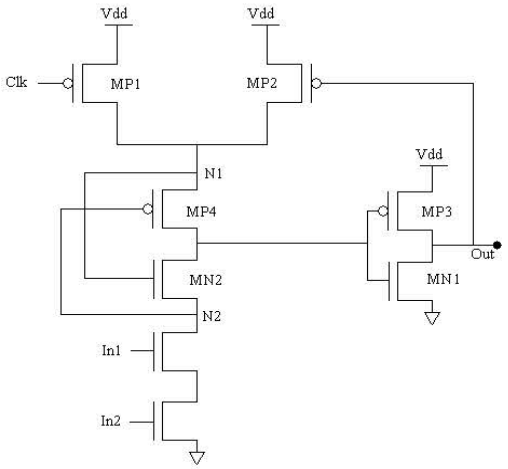

Fig. 1: Proposed technique

Proposed technique: If the inputs are high before the clock sets low, then the voltage at node N2 is not sufficient to turn MP4 completely to OFF state (MP4 is operating near its cut off region). The resistance of MP4 will be lesser than in OFF resistance allowing the dynamic node to get charged high. The charging of the dynamic node is called precharging phase. In this case, the output of the domino logic circuit does not depend on the inputs applied at the evaluation network and the leakage current only is dependent on the input vectors applied as shown in Fig. 1.

Now when the clock turns high or during ideal mode the evaluation phase begins and depending on the inputs the dynamic node will get charged or discharged. If all the inputs are low, then the dynamic node will not get discharged by the evaluation phase transistors and the output at the inverter will be low. This turns ON the transistor MP2, the voltage at node N1 will turn ON the transistor MN1 but the voltage induced at node N2 will not cut off the transistor MP4 and it will be operating around its cutoff region which would increase the effective resistance between and ground, reducing sub-threshold and gate leakage current. If all the applied inputs are high, the dynamic node discharges through the evaluation phase network and the output of the inverter will be high. Transistor MP2 will turn OFF, the voltage at node N1 will operate the transistor MN2 near its cut off region again offering high resistance path. The potential at node N2 will turn ON the transistor MP4. So by introducing the LCTs the resistance between and ground is increased and simultaneously propagation delay of the domino circuit is also increased. The propagation delay can be controlled by sizing of the LCTs.

Implementation of the proposed stalk technique: The proposed STALK technique is implemented in footerless domino logic 4 bit Ripple Carry Adder (Kursun and Friedman, 2003) which consists of four blocks connected to each other. In the first block, the pull up network consists of precharge transistors and the full adder is designed in the pull down network using NMOS transistors only. Between the precharge transistor and the Pull down network, the Leakage Controlled Transistors are implemented. The inputs for the full adder are applied to the transistors implementing the Full adder logic in the Pull down network. Stacking is done in transistors connected to the ground in the pull down network. An inverter is connected to the dynamic node. Dynamic node is the node formed at the connecting point of the pull up transistor and the pull down network. The input to the inverter is applied from the drain of the two LCTs. From the output inverter, the Full Adder outputs are obtained. This design operates with the own individual digital implementation in the domino logic style along with the characteristics of the proposed STALK technique as explained in this study leading to the overall power consumption reduction, delay reduction and the sub-threshold leakage current reduction.

For a better interpretation of the effectiveness of the proposed technique, the comparison of various full adders is done and the results are compared with the Domino Full Adder with the proposed technique. Existing adders namely, conventional 28T cmos full adder, 20T transmission gate full adder, 14T full adder, 10T static energy recovery full adder, 10T full adders realized by gate diffusion input (gdi) structures, adder 9A and 9B are the adders taken for comparative analysis. When the average power consumption , delay and sub-threshold leakage of these circuits are compared with the domino full adder with the proposed technique, results show that domino full Adder with the proposed technique has lesser leakage, power consumption and delay.

RESULTS AND DISCUSSION

The proposed circuit is simulated in 45 nm technology using TSPICE tool with library files downloaded from PTM library. The applied voltage is 0.9 V. The high and low threshold voltages for the nMOS transistors used are 0.466 V and 0.22 V, respectively. Similarly, the high and low threshold voltage for the pMOS transistor used are -0.4118 V and -0.22 V, respectively. Table 1 shows the leakage power measurements are done atC to check it suits at all environmental conditions. Figure 2 depicts the simulated circuit diagram of footerless domino full adder.

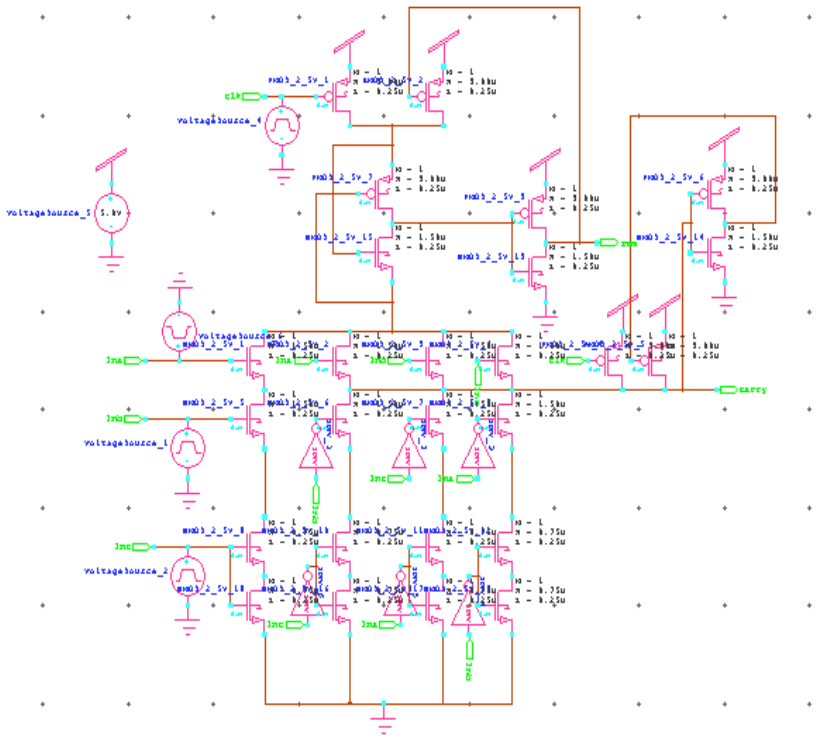

Fig. 2: Footer less domino full adder

Table 1: Comparison of different adders and domino full adder with proposed STALK technique at 1100°C

Techniques	P_{Leak} (µW)	I_{sub}(µA)	NM	Area (µm2)	Active Power (µW)	Delay(ps)	POP(FJ)
Con.28T CMOS Full Adder	43.80	48.76	0.45V	2712.87	83.46	68.18	5.10
2OT Transmission GATE	34.37	38.18	0.49	1854.70	75.56	69.27	4.98
Domino Full Adder	29.80	33.11	0.58	1912.24	78.76	68.72	5.02
Proposed STALK Technique	21.37	23.74	0.62V	2208.9	78.70	73.4	5.24

Table 2: Comparison Of Different Adders And Domino full Adder With Proposed STALK Technique at 250°C

Techniques	P_{Leak} (µW)	I_{sub}(µA)	NM	Area (µm2)	Active power (µW)
Con.28T CMOS Full Adder	36.62	40.68	0.5	2712.87	85.20
2OT Transmission GATE	28.74	31.93	0.54	1854.7	79.74
Domino Full Adder	22.73	25.25	0.60	1912.24	81.42
Proposed STALK Technique	15.87	17.63	0.64	2208.9	80.46

The results of the proposed work is compared with various existing adders. For this, different adders were simulated separately and their performances were studied separately. Results are evaluated based on sub-threshold leakage current, power consumption and delay. The simulation results are illustrated in Table 2.

From, Table 1 and 2, it is clearly evident that the leakage current and leakage power of the proposed STALK technique is significantly lower than the existing techniques. Evaluation of the proposed technique is done both at 25 and at 110°C. The power delay product is comparable with those of the existing ones, whereas we find a slight shoot up in area and delay in the proposed approach. While comparing the leakage current reduction of the proposed technique with those of the existing ones, the delay and area shoot up is negligible and can be given less importance.

From Fig. 3, it is clearly evident that the proposed technique has a significant amount of leakage reduction as compared with those of the existing ones which makes it more superior to the conventional techniques availiable.

From Fig. 4, it is clearly evident that there is only a small shoot up in delay when compared with the existing techniques which provides only a minor impact in the circuit while comparing with power consumption.

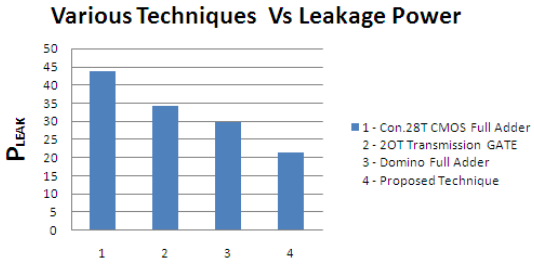

Fig. 3: Graphial representation of leakage power of the proposed technique along with existing techniques

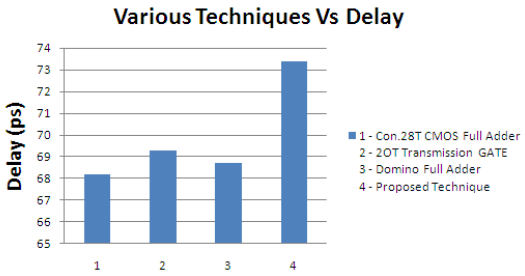

Fig. 4: Graphial representation of delay of the proposed technique along with existing techniques

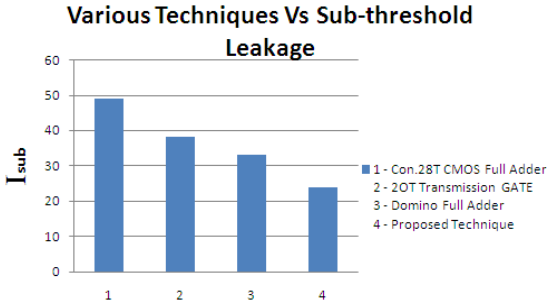

Fig. 5: Graphial representation of subthresholdleakage current of the proposed technique along with existing techniques

Figure 5 shows a flawless reduction in the sub threshold leakage current of the proposed technique with those of the existing ones, which makes it a surpassing technique much suited for low power applications.

Figure 6, it can be concluded that the proposed technique is worthy for varying volages. The proposed technique is fit to temperature variations and its performances evaluated at 25 and at 110°C which shows that the total leakage power obtained is significantly lower than the conventional techniques (Fig. 7).

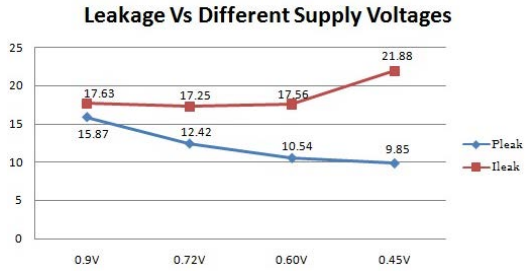

Fig. 6: Graphial representation of leakage current of the proposed technique at different supply volages

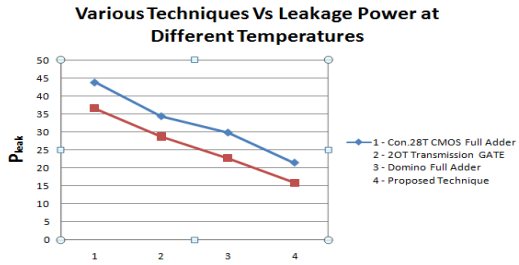

Fig. 7: Graphial representation of leakage power at different temperatures

CONCLUSION

The proposed STALK technique is implemented in footerless domino logic full adder circuit and a significant amount of power saving is achieved. Compared to the existing techniques, the proposed technique shows a greater reduction in both the parameters, power consumption and subthreshold leakage current, with an admissible increase in area and delay. The proposed technique can be implemented in all CMOS circuits to achieve better power savings by reduction in subthreshold leakage current.

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