Asian Journal of Information Technology 15 (2): 277-282, 2016
ISSN: 1682-3915

Performance Analysis of Low Power Port Bandwidth Weight Router Architecture

[1]M. Deivakani and [2]D. Shanthi
[1]Department of Electronics and Communication Engineering,
[2]Department of Computer Science Engineering,
PSNA College of Engineering and Technology, 624622 Dindigul, Tamil Nadu, India

Abstract: Routers are playing crucial role in the field of networking. In this study, the multi port network on-chip router is proposed. The port weight based routing methodology is proposed in this study for low power applications. The proposed network architecture employs a pipelined circuit-switching approach combined with a dynamic path-setup scheme under a multistage network topology. The proposed router does not maintain any routing table to route the packets from source to destination. The performance of the proposed router is analyzed in terms of power and current consumption with conventional methods. The proposed system uses Modelsim software for simulation purposes and Xilinx Project navigator for synthesis purposes.

Key words: Error control, NoC, packetization, router architecture, routing techniques

INTRODUCTION

Network-on-Chip (NoC) is an approach to designing the communication subsystem IP-cores in a System-on-Chip (SoC). NoC applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. Network-on-Chip is spreading rapidly with the development of new architectures and new efficient techniques called 'ROUTING'. Therefore, we define routing as a process of finding the best path for a packet to be forwarded to its destination through a router, based on a routing protocol which is suitable for that particular transmission. Usually, packets are received at an inbound network interface, processed by the processing module and, possibly, stored in the buffering module. Then, they are forwarded through the internal interconnection unit to the outbound interface that transmits them on the next hop to reach their final destination

Implementation of routing in Very Large Scale Integration (VLSI) design proves to be very challenging since, discrete optimization problems occur during its accomplishment. Usually, ICs are being designed with dedicated point-to-point connections, i.e., one wire for every signal. Now with new developments in chip manufacturing technologies several Intellectual Property (IP) blocks such as processor cores, memories, dedicated hardware can be built on single chip with high increase in computation performance. For such rising computation performance the communication bandwidth requirement also increases with same rate. Network-on-Chip (NoC) is an approach to designing the communication subsystem IP-cores in a System-on-Chip (SoC). NoC applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs. Network-on-Chip (NoC) is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip. Network-on-Chip is spreading rapidly with the development of new architectures and new efficient routing techniques. The aim of routing phase is finding a realization of connections offered by the placement phase. In general, routing can be classified into global routing and detailed routing. Global routing finds the approximate interconnections between the blocks whereas detailed routing acquires the output from the global router and delivers the accurate geometric layout of the wires for connecting the blocks.

In this research, we propose a new routing architecture to enhance the energy efficiency of routing systems by means of low power consumption and no performance degradation. The motivation of this study is to design a low power router based on port bandwidth.

Literature review: Roy and Ghosal (2013) proposed a multi-objective global routing technique using fuzzy logic. A set of guiding information is generated from this technique prior to routing phase which helps routing in subsequent steps. During global routing the decision is taken from a fuzzy logic expert system. A GUI is implemented based on the algorithm which is tested for its feasibility study and experimental validation.

Corresponding Author: M. Deivakani, Department of Electronics and Communication Engineering,
PSNA College of Engineering and Technology, 624622 Dindigul, Tamil Nadu, India

Elghazali *et al.* (2009) proposed 6 different architectures for implementing VLSI maze routing algorithm on FPGAs. Their designs utilized a separate hardware accelerator and two processors (MicroBlaze and Power-PC). For maze routing, 2 protocols were designed for data transfer with the hardware accelerator. In terms of seven benchmarks, their proposed architectures were evaluated. Their method was evaluated based on performance and power consumption of the architecture and the best power-delay product was obtained compared to all other conventional routing algorithms.

Mattihalli *et al.* (2012) presented a networking solution for router design used in networking systems using VLSI techniques. Their method was based on hardware coding and reduced the effect of latency issues. Verilog code was used to design a multipurpose networking router to maintain the same switching speed with more security as the packet storage buffer is embedded on chip and the code is generated as a self-independent VLSI based router. Their approach enabled the routers to simultaneously process multiple incoming IP packets through various versions of protocols. The results showed improved switching speed per packet in routing.

Gester *et al.* (2012) presented a novel algorithm which provides high-quality and fast global and detailed routing. Their routing algorithm was based on a shape-based data structure for pin access which used accurate shortest path algorithms and for long-distance connections; they used a two-level track-based data structure. They demonstrated their superiority over traditional approaches by a comparison to an industrial router (32 and 22 nm chips). Their router design was proved to be two times faster than other algorithms and had 5% less net length, 20% less vias and reduced the detours for about 90%.

For the simultaneous estimation of constraints of several routes, a look-ahead method was used in Md-Yusof *et al.* (2009). To minimize the routing search space, the principle of non-dominance was used. Path length method has been employed in selecting the routes contained by predefined constraint bounds. Experimental results showed that their routing methodology might manage constraints of multiple routes. Yet, their technique consumes a longer time for simulation when compared to single-constraint routing with the total time in order of seconds.

Vangal *et al.* (2008) proposed an integrated network-on-chip architecture with 80 tiles arranged as an 8×10 2-D array of floating-point cores and packet-switched routers. The on-chip 2-D mesh network provides a bisection bandwidth of 2 Terabits/s and the fully functional first silicon achieveda performance of 1.0 TFLOPS on a range of benchmarks with a power dissipation of 97W at 4.27GHz and 1.07V supply. Anhybrid microarchitecture was designed for NoCs by combining a broadband photonic circuit-switched network with an electronic overlay packet-switched control network (Shacham *et al.*, 2008). Their design makes use of the strength of each technology and represents a flexible solution for the different types of messages that are exchanged on the chip; large messages are communicated more efficiently through the photonic network while short messages are delivered electronically with minimal power consumption. The average number of Photonic Switching Elements (PSEs) in the ON state is about 86 in a 576-PSE NoC. Hence, the total power consumption was estimated as 860 mW.

Pham *et al.* (2013) proposed a novel on-chip network to support guaranteed traffic permutation for multiprocessor SoCs. They employed a combination of pipelined circuit-switching and approach a dynamic path-setup scheme under a multistage network topology. The circuit-switching approach offers a guarantee of permuted data. Their experimental results showed that their on-chip network achieved 1.9×8.2 reduction of silicon overhead compared to other conventional designs.

Al Faruque *et al.* (2012) presented an adaptive route allocation algorithm to provide a guaranteed QoS combined with an adaptive buffer assignment scheme. Their scheme reduced the area overhead by resource multiplexing due to the on-demand buffer assignment at each output port. An average of 42% buffer saving was reported in their experiment. Banerjee *et al.* (2009) analyzed various designs of a circuit-switched router, a wormhole router, QoS supporting virtual channel router and speculative virtual channel routers. The energy performances of these different routers were accurately evaluated based on their power consumptions.

The router designs in previous methodologies were based on the port bandwidth, not based on port weight. They consumed more hardware utilizations and power consumption. All the above approaches were not effective in dealing with hard-to-predict system behaviour and varying workloads.

MATERIALS AND METHODS

Proposed routing scheme: Generally, the function of a router is to determine the appropriate paths for nets on the chip layout to interconnect the pins on the circuit blocks. The most important objective of routing is to complete all the required connections, i.e., to achieve 100% routability, else causing the operation of the chip to fail. The proposed routing design is shown in Fig. 1. It

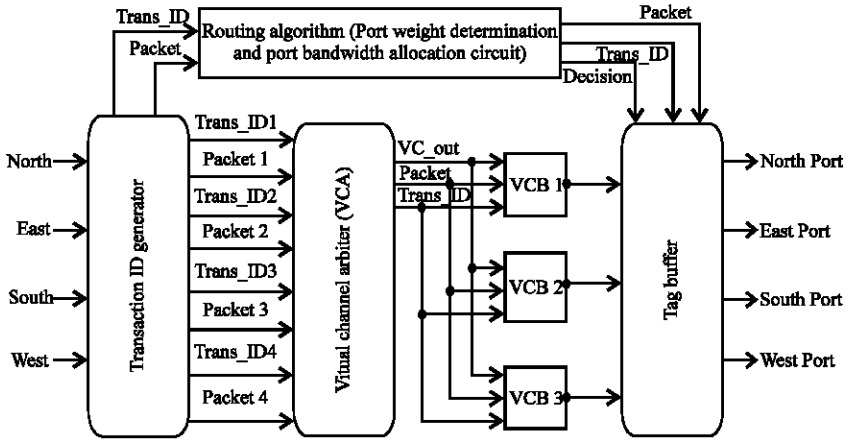

Fig. 1: Architecture of proposed router

consists of transaction ID generator, virtual channel arbiter, virtual channel buffer and a tag buffer. The detailed routing algorithm is explained in upcoming sections. The proposed router generates the 10 bit transaction ID for each input packet in random manner in order to differentiate the input packets.

Port bandwidth allocation circuit: Bandwidth allocation deals with avoiding bandwidth usage overflow and to minimize bandwidth usage under bandwidth-limited constraints at the same time, maintaining the rate-distortion performance stable. The 10bit router address and 10bit destination address are summed up by an adder and right shifted by 2bits. Also, the router address is left shifted by 1bit and subtracted with the destination address and then, again right shifted by 2bits. Both these results are sent to a Multiplexer (MUX 1).

Similarly, MUX 2 receives the router address in one line and shifted bit result in another line. The selection lines S_0 in MUX1 and S_1 in MUX2 determines the selection of bits to be sent to the bandwidth determinator where the bits are represented as integer.

Overflow in bandwidth usage leads to encoding delays, thus causing a failure of real-time constraints and leading to frame dropping, i.e. loss in quality. Figure 2 shows the port bandwidth allocation unit implemented with multiplexers, shifters, comparators, subtractors and adders at low hardware cost. Each port in the router has a port weight and it is based on the destination address (xd, yd) and router address (x, y) of the incoming packet. The packet is always forwarded towards the output port, where the port weight is maximum. The port weights for each direction (North, South, West, East) are given below in Eq. 1-4:

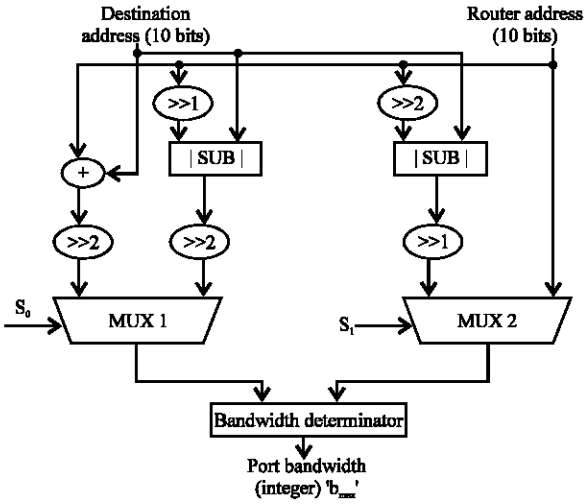

Fig. 2: Bandwidth allocation circuit

$$W_N = \begin{cases} b_N \times |y_d - y| + b_{max}, & y_d - y < 0 \\ 0, & b_N < b_p \\ b_N, & \text{else} \end{cases} \quad (1)$$

$$W_S = \begin{cases} b_S \times (y_d - y) + b_{max}, & y_d - y > 0 \\ 0, & b_S < b_p \\ b_S, & \text{else} \end{cases} \quad (2)$$

$$W_W = \begin{cases} b_W \times |x_d - x| + b_{max}, & x_d - x < 0 \\ 0, & b_W < b_p \\ b_W, & \text{else} \end{cases} \quad (3)$$

$$W_E = \begin{cases} b_E \times |x_d - x| + b_{max}, & x_d - x > 0 \\ 0, & b_E < b_p \\ b_E, & \text{else} \end{cases} \quad (4)$$

Where:

b_N = North port bandwidth
b_S = South port bandwidth
b_E = East port bandwidth
b_W = West port bandwidth
b_{max} = Maximum available bandwidth
W_N = North port weight
W_E = North port weight
W_S = North port weight
W_W = North port weight

The maximum port weight is determined by maximum of $\{W_N, W_S, W_W, W_E\}$. The packet will be transmitted through the output port whose port weight is maximum.

VCA: The Virtual Channel Arbiter (VCA) in Fig. 3 guarantees allocation of the required bandwidth for a single frame. The VCA disregards the short-term variations and holds only the guaranteed allocation for the port unaltered. But, if the bandwidth variation exceeds the guaranteed allocation, the required variation in bandwidth update period will be issued by the VCA. The virtual channel arbiter passes the new allocated data transmission rate and bandwidth update period to the bandwidth controller. After that, the new search range is calculated by the controller based on the proposed method and current block pixels of current macro block have been accessed.

Tag buffer: The implementation of the tag buffer is shown in Fig. 4. It stores the way tag temporarily which arrives from the way-tag arrays. It shares the control signals with L2 cache and possesses the same number of entries of the write buffer. The line size of way-tag array is n, such that all the entries of the way-tag buffer have (n+1) bits. To indicate the write miss operation in the current entry, an additional status bit is used. During the occurrence of write miss, all the ways in the L2 cache will get activated due to unavailability of way information, else, only the desired way gets activated.

A single clock cycle is needed for updating the status bit. The stored operation in write buffer is sent along with its way tag to the L2 cache which requires the data in write buffer and its way tag to be sent simultaneously. Otherwise, write/read conflicts may occur in the way-tag buffer. However, this problem may be fixed by inserting a cycle delay to the write buffer using a bypass multiplexer (MUX in Fig. 4) between the L2 cache and way-tag array.

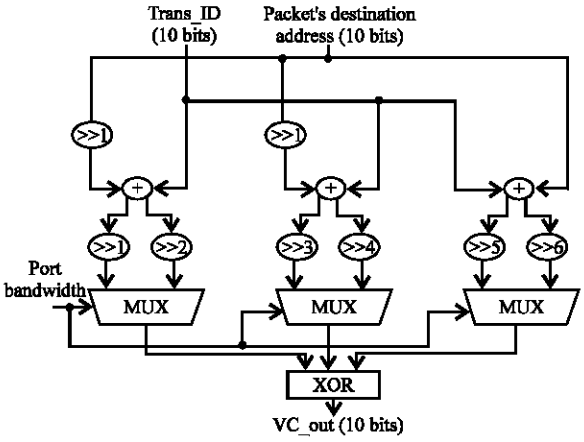

Fig. 3: Architecture of proposed virtual channel arbiter

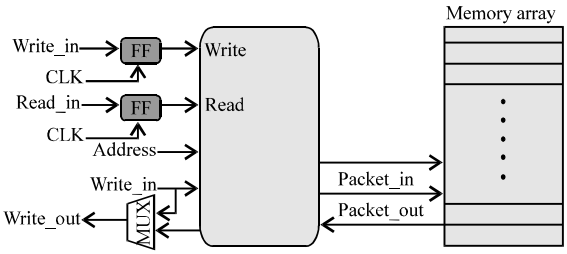

Fig. 4: Tag buffer design

RESULTS AND DISCUSSION

For appraising the performance of the proposed architectures, each scheme is synthesized by Xilinx Project navigator tool using the 90 nm CMOS technology and modelsim for simulation. The performance of the proposed routing algorithm is evaluated and the results of simulation are illustrated in Fig. 5. Figure 5a depicts the designed router IC using Xilinx project navigator design tool which illustrates the main ports of the router. Figure 5b represents the RTL schematic representation of the proposed routing methodology which consist of Look Up Tables (LUTs) and comparators. The packets are forwarded to any one of the output port (EAST, NORTH and SOUTH) based on the maximum weight as shown in Fig. 5a. The packets are entered into the router through the WEST port of the router.

The hardware utilizations and its specifications are clearly shown in Table 1. Table 2 describes the power and current utilization of different devices of Spartan family. The junction temperatures of various Spartan family devices are listed in Table 3. The proposed method is also compared with other existing routing algorithms and shown in Table 4. The comparison shown in Table 4 is in

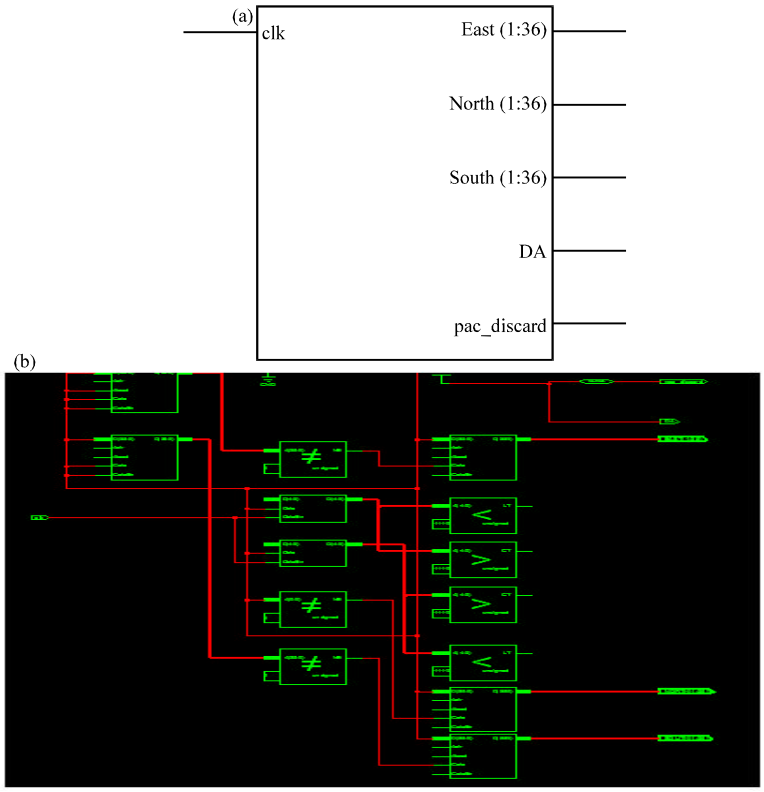

Fig. 5: a) Designed IC view; b) RTL schematic representation

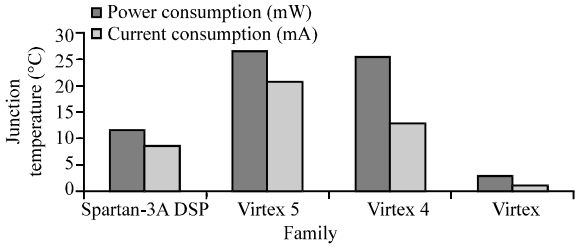

Fig. 6: Graphical plot of power and current utilizations

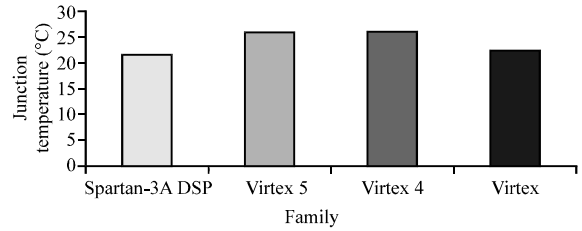

Fig. 7: Graphical illustration of junction temperatures

terms of power consumption. Figure 6-8 graphically represent the data in Table 2-4, respectively. Table 2 represents the power consumption and current consumption of the proposed methodology (with respect to the condition of Eq. 1-4) using Xilinx project

Table 1: Device specifications

Family	Device	Package
Spartan-3A DSP	XC3SD1800A	CS484
Virtex 5	XC5VLX30	FF324
Virtex 4	XC4VLX15	SF363
Virtex	XCV50	BG256

Table 2: Results on power and current consumption on various devices

Family	Power consumption (mW)	Current Consumption (mA)
Spartan-3A DSP	115.00	82
Virtex 5	267.00	208
Virtex 4	253.00	127
Virtex	26.79	10

Table 3: Results on junction temperature which affects the performance

Family	Junction temperature (°C)
Spartan-3A DSP	25.00
Virtex 5	29.94
Virtex 4	30.26
Virtex	25.81

Table 4: Performance comparison of different methodologies

Methodology	Power consumption (mW)	CMOS echnology	Frequency (MHz)
Proposed work	27.0	65	200
Vangal *et al.* (2008)	670.0	180	350
Shacham *et al.* (2008)	227.0	90	400
Pham *et al.* (2013)	110.8	90	350
Al Faruque *et al.* (2012)	725.0	180	350
Banerjee *et al.* (2009)	92.0	90	350

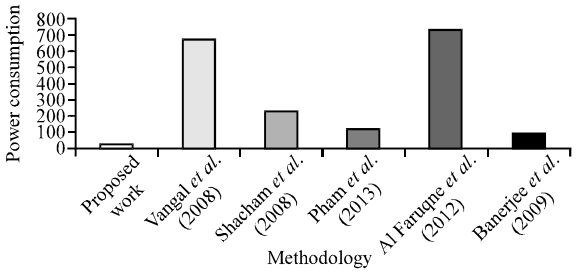

Fig. 8: Graphical illustration of comparison of power consumptions

navigator synthesis tool by implementing the proposed routing method on different FPGA processors. The power consumption of the proposed methodology and conventional methodology (Vangal *et al*., 2008; Shacham *et al*., 2008; Pham *et al*., 2013; Al Faruque *et al*., 2012; Banerjee *et al*., 2009) are measured using Xilinx Project Navigator 12.1 (power prime) tool.

CONCLUSION

This study has presented an efficient port bandwidth weight based routing architecture to route the packets from source to destination. The proposed router does not maintain any routing table to route the packets from source to destination. The performance of the proposed router is analyzed in terms of power and current consumption with conventional methods. The presented approach can be combined with other low-power approaches to further reduce the overall power. The proposed port bandwidth weight computation router architecture consumed 26.79 mW of power and 10 mA of current.

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