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Analysis and Performance Evaluation of Maximum Step up Ratio DC to DC Resonant Converter

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Abstract: The HVDC and wind turbine interfaces were attain the researchers interest by its megawatt ratings over the dc-dc convertors ration with high setup. In this stusy, we have produced a regular multi-stage dc-dc resonant converter enhanced with topology of ideal boost converter. In this mechanism the traditionally used single switches were replaced instead of that number of clamped capacitor sub-modules are implemented. In which the converter is implemented with some resonance betweenthe arm inductor and sub-module clamped capacitors in a resonant mode. To provide a constant number the switching arrangement ofa phase-shifting operation is provided and supported by N of sub-capacitor modules at very high voltage. On this operation mode the count of sub-capacitor modules and the inductor charging ratio play a vital role which supports the step-up ratio. This converter has the capacity of bidirectional power flow and even without transformer it exhibits scalability. A wind turbine interface as an application example is shown with the conversion ratio 10:1 which is shown on simulation results. The proposed concept is experimentally verified with a laboratory-scaleprototype.

Key words: HVDC converters, DC transformers, dc-dc conversion, regular multi-stage converters, resonant conversion

INTRODUCTION

In general multilevel converters are mainly employed for medium and high voltage real time applications, so that it minimize the output voltage harmonic content as better than the traditional converters as shown in (Zhang and Green, 2015; Solas *et al*., 2013; Perez *et al*., 2012). These usages of dc-dc conversion with multilevel converters have raised its popularity among renewal energy based on the frequency success in dc-ac conversion (Ferreira, 2013). In the past there are various types of multilevel converters were developed by implementing the step-up dc-dc converters directly or in-directly (Perez *et al*., 2015). In which considers to the others regular Multilevel Converter (MMC) is most popular and designed with more attractive features. The diode clamped converters are practically not possible to implement due to the requirement of multiple number of diodes to be present on clamped converters. Next is Conventional flying capacitor converters but it requires series of capacitor connections (Meynard and Foch, 1992). Which means the requirement of capacitor volume is huge. To improvise the system a step-up dc-dc conversion with generalized multilevel converters is designed (Peng, 2001; Todorcevic *et al*., 2013; Monge *et al*., 2011). It results in large topology size with high step ratio. The IPOS converters (input-parallel output-series) and switch converters built up for step-up operation of dc-dc conversion (Khan and Tolbert, 2007; Kouro *et al*., 2010; Leon *et al*., 2011). In order to get efficiency and maximum power conversion the IPOS uses resonant sub-modules but to balance the differences between the windings it requires more number of isolating transformers (Ortiz *et al*., 2013). The series-parallel topologies are increasing the voltage switch at the module capacitor/module switch. Stress difference between the peak voltage and output dc voltage is very close. The switched capacitor converters were used to control the high charge losses and overshoot currents. This drawback is balanced by high switching frequency with driving MOSFETs. This shows that the switched capacitor converters can applicable at low voltage conditions. Young *et al*. (2013) Cockcroft-Walton multiplier using power electronics explains gives an effective solution for high voltage dc on the requirement of unidirectional step-up. Next a ladder shaped bidirectional medium voltage dc converter is discussed at

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(Kasper *et al*., 2013) that have the capacity to gain high step ratio. The best thing in this set up is does not need for switching synchronization between the sub-modules.

In the emerging new technology growth regarding the medium and high voltage applications uses regular multilevel converters for dc-dc conversion which based on conventional MMCs (Zhang *et al*., 2015; Antonopoulos *et al*., 2014; Kasper *et al*., 2013; Luth *et al*., 2014). Generally MMCs balance the voltage level by control scheme as they provide a fine quality waveform between more than two levels. The fault cells are bypassed by operational systems with redundancy and high regularity.

The MMCs has no direct and simple solution for dc-dc conversion operated at large step-up ratio. In this study, we present an enhanced topology with control scheme for those multi-stage bidirectional dc-dc converters using maximum step-up ratio. The PWM (pulse-width-modulation) with Phase-shifted increases the operating frequency in those subs-module switching frequency. Compared to the traditional converters our proposed converters enhanced their step ratio; as they are bidirectional can effectively manage the low power dc-dc applications by means of regularity, elasticity and simplicity. The below prototype explains the circuit configuration and the principle of operation which are also validated by the simulation results.

MATERIALS AND METHODS

Bidirectional regular multistage dc-dc converters: The conversion of regular multistage format from simple standard switched mode requires multiple clamped sub-modules. Figure 1 clearly shows the configuration of half-bridge clamped single switches in which the IGBT is replaced by anti-parallel diode. On MMC topologies it is complex in forming series of stack of switches with off-state voltage across. This concept is implemented with regular multilevel inverter topology by series of arrangement on IGBT. It implies good voltage and sharing between sub-modules with active clamping.

The concept of active clamping is also applicable for dc-dc converters in which the upper and lower IGBT's are termed as clamping IGBT and clamped IGBT, respectively. Figure 2 (i) shows the definitive bidirectional two-stage dc-dc converter which low voltage with inductor along with a pair of IGBTs withInput/output capacitor sandanti-parallel diodes. On Fig. 2 (ii) it is shown a regular

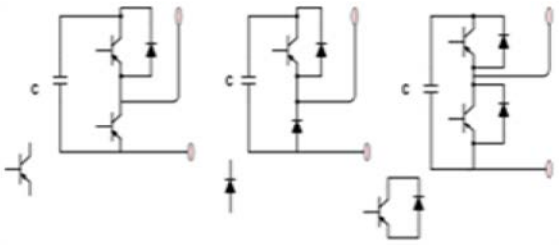

Fig. 1: Active clamping of sub-capacitor modules and single switches

multistage dc-dc converter by replacing serially connected sub-modules on switch with active clamping. Here some special operation techniques are needed instead of compensating upper sub-modules with lower upper sub-modules.

Maximum step-up ratio regular multistage dc-dc conversion: The proposed operationalmechanism of dc-dc converter is discussed in this section which shows the step by step analysis of step up operation of dc-dc conversion. By theoretical is explained by the following assumptions:

- The sub-modules and switches were identical and ideal
- A lossless converter
- A balanced steady-state dc voltage capacitor

System configuration: As shown in Fig. 3 (i) a diode andanindividual IGBT is configured with boost converter technology in which the lower position of IGBT is recharging the input inductor (L). The circuit diode on upper part is communicated mechanically by passing the discharging circuit current to the peak voltage capacitor (CH). Figure 3 (ii) shows the regular multistage unidirectional operation of step up dc-dc conversion with active clamping by means of half-bridge sub-modules on lower position M. The upper position N is denoted by the arrangement of chopper (clamped diode) sub-modules. There is an equal arrangement of output (high-side) voltage with sum of capacitor voltages on sub-modules stack. A little difference is shown between the instantaneous voltage across the

Stack to the voltage across CH along with small inductor LS. The CL is the large capacitor placed at input side and the Fig. 4 demonstrates the proposed circuit of step-down operation converter.

Mechanism of phase-shift controller: The proposedmultistage converter results in several operating characteristics and step-up ratios under the examination of multiple operation modes. In this study, we focused on

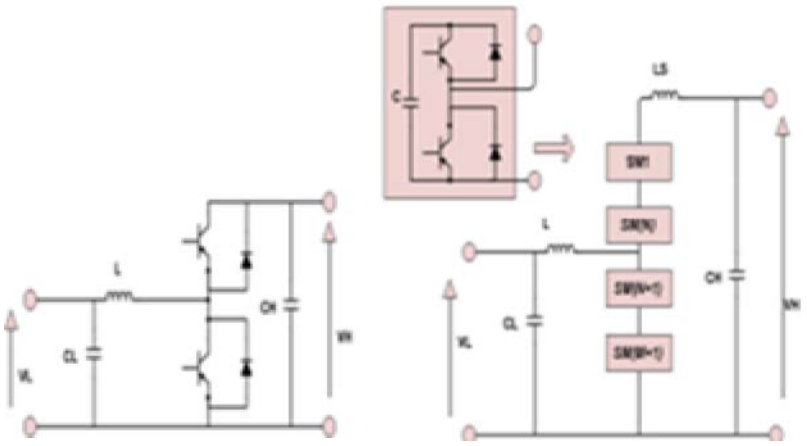

Fig. 2: Bidirectional operations ofdc-dc conversion (i) Traditional two-stage dc-dc conversion (ii) Newregular multi-stage dc-dc conversion

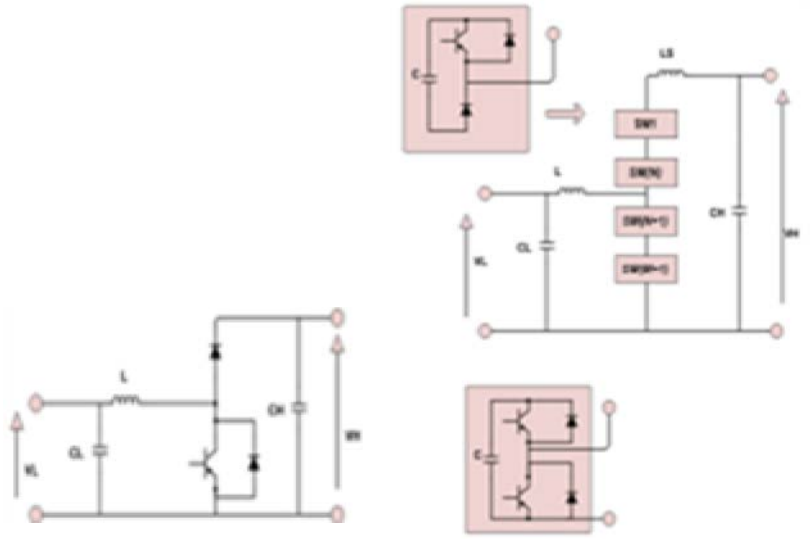

Fig. 3: Unidirectionalstep-up operation of dc-dc conversion (i) Traditional boost conversion (ii) Proposed regular multi-stage step-up dc-dc conversion

maximum step-up ratio operational mode on this mode a regular conversion is used for maximum step-down ratio of dc-dc converter results the medium voltage systems with auxiliary electronic circuit. The converter is also applicable for minimum step ratio, high-voltage dc-dc converter with sub-modules in both upper and lower stacks. The proposed regular multistage step-up dc-dc converter is controlled by Phase-shifted PWM (PS-PWM) converter. It is formatted in the order of high duty-cycle with a single sub-module capacitor per time, so that the step-up ratio is depends on count of upper circuit cells N. Then the excitation frequency is maximum than the switching frequency of a single cell.

The principle of PWM states in diode position a step-up converter is placed with four sub-modules. It shown in Fig. 3 (ii) It is proved by injecting three/four sub-modules at sometime under duty-cycle of above 75%. Here, for example, 90% is employed in which lower position operation with one module that is four times of upper module switching frequency. Here the system with lower position operation under two sub-modules was illustrated by step-up converter and step-down.

It is demonstrated on Fig. 5 and 6 the clamped circuit diode cells are synchronously switched using Clamped IGBTs by which the entire voltage of both upper and lower cells are describe as v_n and v_m. Son the operational

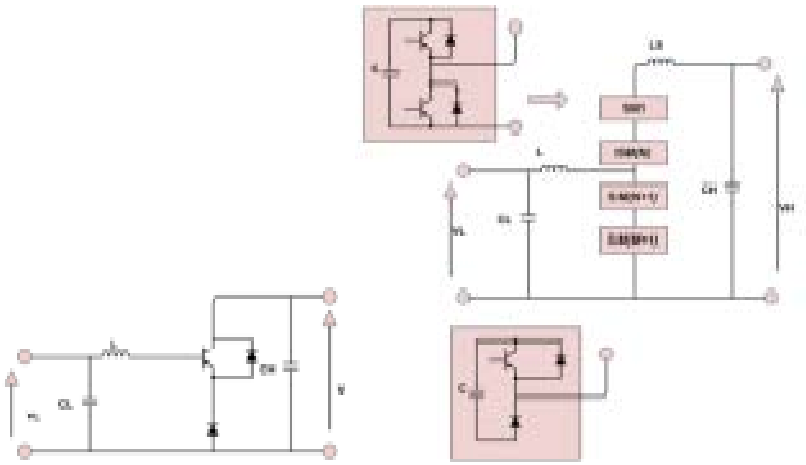

Fig. 4: Unidirectional step-down operation of dc-dc converters (i) Traditional buck converter. (ii) Proposed regular multistage dc-dc converter

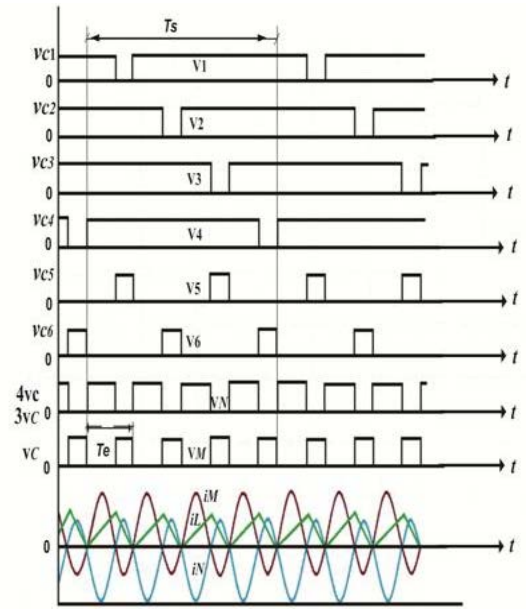

Fig. 5: The proposed multistage dc-dc converter waveforms

frequency is equivalent to the switching frequency four times of the upper cells and the switching frequencytwo times of the lower cells. According to the Fig. 6 the step-down operation is executed under same stack voltage waveforms with step-up dc conversion. Here theresults of voltage sub-modules are not shown instead the time domain proposed step-up converter key waveforms are shown.

Maximum conversion ratio: The proposedmultistage dc-dc converter is targeted for maximum step-up ratio of

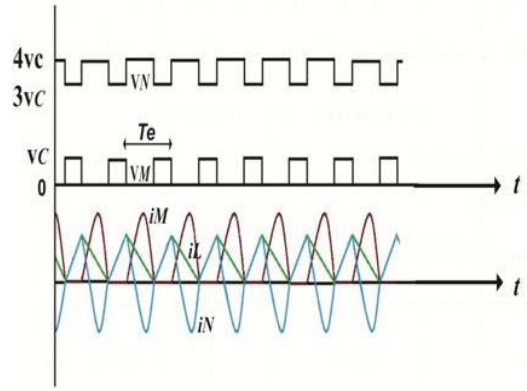

Fig. 6: The proposed multistage step-down dc-dc converter waveforms

dc-dc conversion by which the operation as well as conversion ratio are examine at one equivalent cycle Te which is shown in Fig. 5. Figure 7 highlights the two modes of the circuit with a circuit diagram. As per Fig. 7 (i) the mode 1 is begins with switched on at IGBT present in Cell 4 and finishesat IGBT in Cell 1in the state of switched off. The mode 2 is begins with IGBT present in Cell 1 at switched off state and the Cell 5 switched off at minimum IGBT. Finally, the mode 2 is ends with Cell 1-IGBT are switched on as shown in Fig. 7 (ii). It shows that mode 1 and 2 are equivalent to each other with on- as well as off-states of ordinary boost converter. The circuit current flowing between upper and lower cells andinput inductor are determined, respectively as i_L, i_M and i_N. On mode 1 the inductor L with currentis charged directly with input voltage v_L through Cell 5 and 6 of IGBT. The serially connected capacitors such as C1-C4 are connected with inductor L_s and capacitor

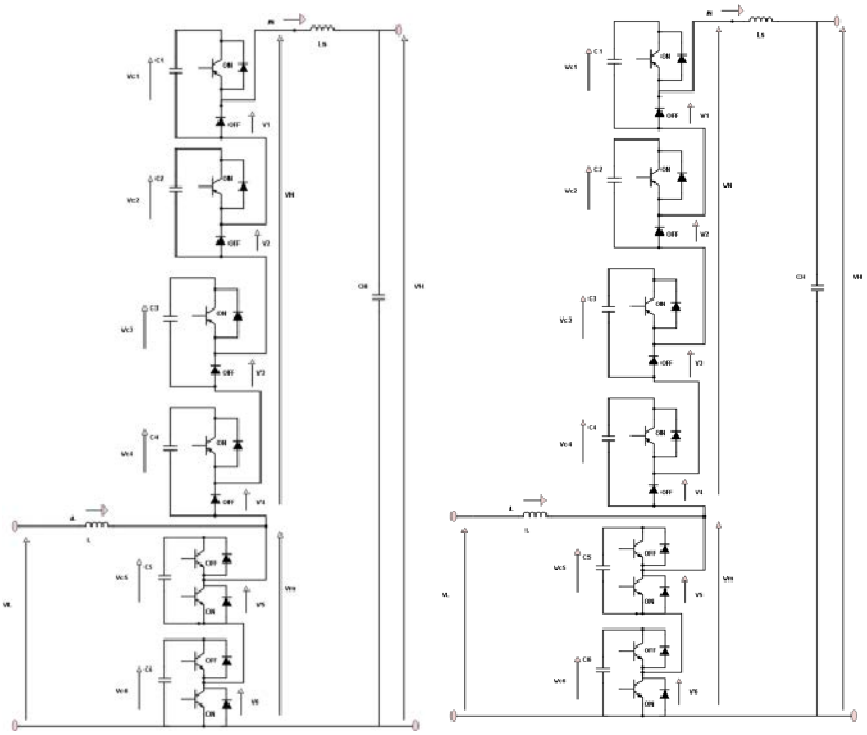

Fig. 7: Step-up operational modes in the initial equivalent controlling cycle: i) Mode1 operation; ii) Mode 2 operation

forming a resonant tank. On this series the C_H is large compared to the cell capacitors. So the cell capacitor dominates the resonant by eliminating. C_H The resonant frequency is states by:

$$f_r = \frac{1}{2\pi\sqrt{\frac{L_S C}{N}}} \tag{1}$$

By this case if N = 4, $f_r = 1/\pi\sqrt{L_s C}$ during the entry of converter from mode 2 to 1 on the circuit C5 is connected to C1 in a series connection with other capacitors C2-C5 at resonant tank L_s and C_H, respectively. In which the mode 2 resonant frequency is depend on series inductor L_s along with four series connected capacitors. There is a possibility of equal resonant frequency at mode 1 and 2 only at which clamped IGBT and clamped diode uses same capacitors. In any condition the original resonant frequency is more than f_e and mode 2 ends with i_N which is less than zero under circuit functions at Discontinuous Conduction Mode (DCM).

When, the mode 1 operation starts the current i_L immediately charged at low voltage side in this stage the resonant starts at current i_N with frequency f_r. At the stage of current through the mode 1 to mode 2 vC5 is higher than v_L with reduced inductor current i_L. In DCM the circuit operates before equivalent operating cycle ends, so that i_N falls to zero with i_M equals to i_L still the new cycle begins. The voltage conversion ratio is obtained by charging the ratio with model time duration relative to the equivalent operating cycle at T_e. In this steady state is increased and decreased respectively to the i_L over T_e which is states by:

$$\frac{v_L T_e d}{L} = \frac{(vCj - v_L) T_e (1-d)}{L} \tag{2}$$

If j = 5 or 6 then the lower sub-modules of capacitor voltages can be stated by:

$$vcj = \frac{v_L}{1-d} \tag{3}$$

The average stacks voltages v_n and v_m is equal with high-side voltage v_H:

$$v_H = \frac{N-1+d}{N}\sum_{j=1}^{N} vCj + \frac{1-d}{M}\sum_{j=N+1}^{N+M} vCj \tag{4}$$

The capacitor voltages were balanced equal at some ideal conditions which are equal to v_C. By derivation the Eq. 3 and 4, we get the voltage conversion ratio:

$$\frac{v_H}{v_L} = \frac{N}{1-d} \quad (5)$$

Here the d is not increasing and the conversion ratio is increased higher numbers of upper sub-modules N. If the N value is 4 then the conversion ratio v_H/v_L = 4/1-d. In this stage the converter's current stress is estimated to determine the power losses and device ratings. The average current of i_L is noticed by high voltage side power consumed with the load dc current l_0. Hence, it is stated by:

$$I_L = \frac{v_H}{v_L} I_o \quad (6)$$

The charging time of inductor L is obtained from peak-to-peak ripple $\Delta/_L$:

$$\Delta I_L = \frac{v_L T_e d}{L} \quad (7)$$

The i_N gives the current stress on the clamped-diode by means the load can feed and the ac components circulate within the resonant tank. Then the current flow dc current by the power of clamped-diode (upper) stack is given by:

$$P_1 = (N-1+d)vCI_o \quad (8)$$

The resonant current sinusoidal waveformwith the square-wave element of the stack circuit voltage is described by:

$$P_2 = \frac{vC}{2} I_{N1} \lambda \quad (9)$$

From Eq. 9 λ describes the current combination and voltage power factor which can be obtained from numerical solutions. If the maximum value λ = 1 is gained then the charging ratio (d) is 0.6. Therefore the proposedconverter is lossless and the upper stack between the ac and dc power are equal:

$$I_{N1}\lambda = \frac{N-1+d}{\lambda} I_o \quad (10)$$

The proposed multistage dc-dc converter is model for both maximum step-up ratiosof dc-dc conversion and step-down dc-dc conversion which is depicted in Fig. 8 with detailed circuit diagram in which two modes of the circuit along with current paths were highlighted. Figure 8 (i) gives mode 1 initiates with clamped IGBT present in Cell 1 which is switch on and terminates at switched off. In the same manner Fig. 8 (ii) shows mode 2 with clamping IGBT present in Cell 6 is at the state switch off that shows opposite direction on step-up operations. The inductor L in the voltage for mode 1 resultsmore than mode 2 then the input current charged at mode 1 and then discharged at mode 2. Then, the Inductor along with C2-C4 were also charged which shows that the clamped diodes are reverse biased. The capacitors C1-C4 are attached in series with inductor L_s to form the energy stored resonant tank from the mode 1. Therefore f_r is the resonance frequency for the step-down and step-up circuit operation with current flowing at lower stack i_M is stated by:

$$i_M = i_L - i_N \quad (11)$$

The current waveform for step-down circuit operation is presented in Fig. 6 which gives sawtooth wave shape for inductor current and zero lower stacks current at mode 1. Then the upper stack current for mode 1 is same but the upper stack current for mode 2 resembles discharging of a resonant wave shape and the step-down output voltage derivation is compute by, v_L high voltage v_H and inductor currentv$_L$. Here v_H =NvCJ and the conversion ration described as:

$$\frac{v_H}{v_L} = \frac{N}{1-d} \quad (12)$$

By which the step-down operation and step-up operation causes same step up ratio which clearly gives that the proposed regular multilevel dc-dc converter and conventional bidirectional dc-dc converter are similar in the aspect of step ratio. The bidirectional power conversion on converter is gained by changing the direction without changing the switching arrangements.

Mechanism of clamped capacitor voltage: The proposed converter with cell clamped capacitor voltage mechanism is demonstrated using step-up circuit operation as depicted in Fig. 7 (i). It has capacitors Cell 1-4 with low voltage side inductor supported by high-side dc voltage. The cell capacitors and inductor L_s forms resonant tank to zero at resonance frequency with negligible resonant components. The output voltage is equal to: vo = vC1+vC2+vC3+vC4 which is expressed as vo = vC2+ vC3+ vC4+vC5, these two equations were compared and stated as: vC1 = vC5. The same method is used for next operating cycle by which one state is vC2 = vC6 followed by the remaining operation on sequences such as vC1 = vC3 = vC5 and vC2 = vC4 = vC6. The capacitor voltages of the upper cells and the lower cells are balanced by clamp and it is equal at steady-state.

The converter in lower position with one cell will inherit the balancing capacity by which it gains the additional balancing control. Figure 9 shows the balancing control of lower cells. The average capacitor

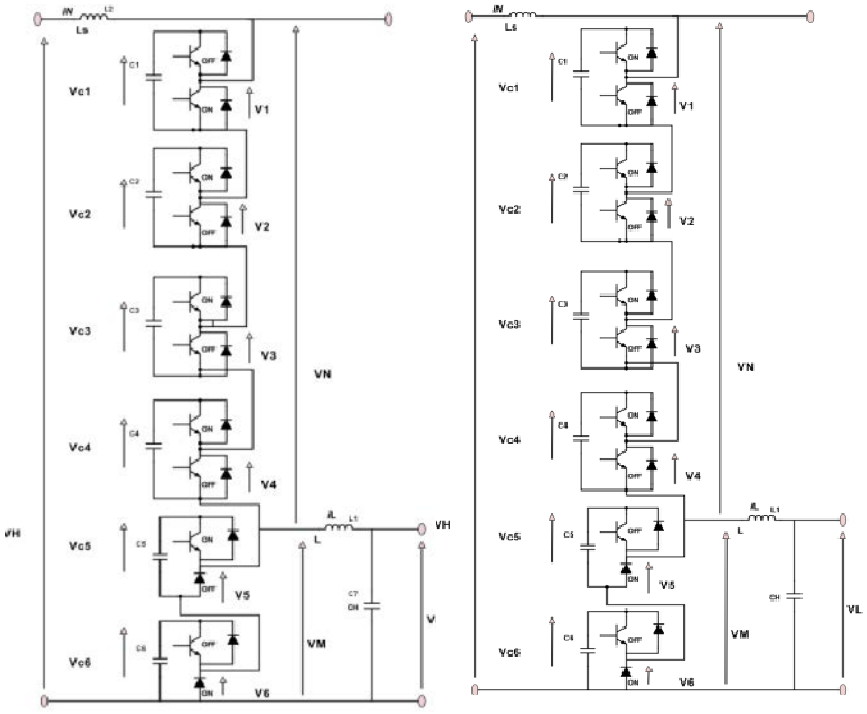

Fig. 8: Step-down operational modes in the equivalent controlling cycle (i) Mode 1 operation (ii) Mode 2 operation

voltages in half bridge cells are used to calculate the reference cell voltage which is derived by:

$$v_{ref} = \frac{1}{M}\sum_{j=N+1}^{N+M} v^{*}Cj \qquad (13)$$

From Eq. 13, vCj it is a sampled capacitor voltage which has considerable ac components that has first order low-pass filters. The each cell in the dc voltage is compared by reference voltage and regulated by proportional feedback control. To adjust the voltage imbalance a dead cell zone is produced with minimum tolerance. Here the limit is adjusted by saturation function and the capacitor voltage is charged by linearly increasing the duty-cycle of a cell (Table 1).

Parameters of the application example: Fig. 10 shows the all sub modules with output voltage feedback control and the voltage regulator is expressed by $H_{v(z)}$. The controller may be phase lead controller or anti-windup. Proportional-Integral (PI) controller which doubled the sub-modules present in lower side when compared to upper side due to the deviationsin the duty-cycle that demonstrated in Fig. 5. The upper sub-modules pulses are complementary by the lower sub-modules.

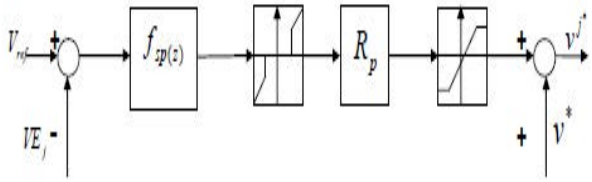

Fig. 9: Voltage control operation of half-bridge circuit

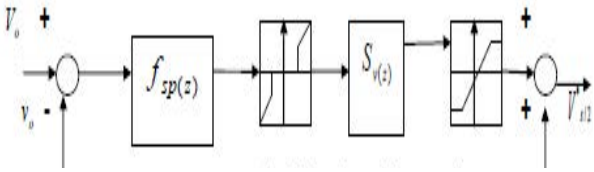

Fig. 10: Common control for output voltage

RESULTS AND DISCUSSION

Experimental results: By means of Fig. 2 (ii) it is clear that the proposed work is constructed with two and four lower and upper cells respectively, in addition to it capacitors with a nominal capacitance is used in

Table I: Parameters of the application example

Symbol	Quantity	Value
P	Power rating	1 MW
VL	Nominal low dc voltage	2 kV
VH	Nominal high dc voltage	25 kV
Ipk	Maximum device current	650 A
Vpk	Maximum device voltage	7 kV
fs	Switching frequency	1 kHz
Te	Equivalent operating cycle	200 μs

Table 2: Circuit parameters

Symbol	Quantity	Value
VL	Nominal low dc voltage	25 V
VH	Nominal high dc voltage	200 V
Ipk	Maximum switch current	30μA
Tb	Sampling period	100 μs
Te	Equivalent operating cycle	250 μs
L	Low voltage side inductor	800μH
Ls	Series inductor	130 μH
C	Cell capacitor	60 μF
CL	Low voltage side capacitor	480 μF
CH	High voltage side capacitor	190 μF
RL	Low voltage side load	19 Ω
RH	High voltage side load	1080 Ω

the sub-modules with the value of 50 μF. By the result the expected resonant frequency is about 5:2 kHz with switching frequency of upper cells is about 1 kHz and lower cell is 2 kHz. The operation frequency is 4 kHz and it is less than resonant frequency. Table 2 shows the complete circuit parameters.

Open-loop tests: In open-loop tests the constantratio of charging is 0.7 and the step-up circuit operation is fixed with input and output voltages are 30 and 300 V, respectively. These switches were not ideal hence the expected value is higher than high voltage and the experimental parameters were simulated at converters for comparison purposes. The wave form with simulated currents and voltages is shown in which voltage is dropped gradually until the switch set to 1 V. Figure 11 (i) and (ii) presents the stimulated value and Fig. 11 (iii) and (iv) demonstrates current and voltage waveforms experimentally. In mode 1 current i_N changes into zero from negative with dramatically damped current resonance. The mode 1 with negative current i_N is dropped voltage to positive by v_N. If the current i_N is changed to positive then the IGBT becomes negative with voltage drop compared to v_N.

In mode 1 the inductor L is in charging state and capacitor C_H is raised with i_N at the terminal of this mode. Then the mode 2 is starts with inductor current i_L and current i_N is resonating till touches zero. From Fig. 11 (ii) the stack voltage waveforms is measured and close to that of Fig. (iv). The result shows the conversion ratio which is minimal than 10:1 than the lower and upper stack voltage with sum under 300 V. Then the required level is achieved by closed-loop control with output voltage. Then for step-down circuit operation 300 V will be the input peak voltage with expected output low voltage of 30V. In the actual switches the voltage drops with minimal output voltage as presented in Fig. 12 (iii) and (iv). In this stage the mode 1 with zero lower stack current then the currentsi_L and i_N is increased linearly. But in mode 2 current i_L is decreased linearly with upper stack capacitors in series by inductor L_s. The operation analysis verifies the proposed converter with around 25 V output high voltages and v_H = 300 V under open loop control. Across IGBT the expected value is more than the output voltage. Figure 13 show sub-modules with step-up operation current and voltage waveforms, in which cell 1 represents upper cells and the cell 6 represents lower cells. Then the resonant frequency is 4 kHz with 1 kHz of upper cells switching frequency. The upper cell has the clamped switch with switch-on and switch-off currents are at low. The operationalmechanism of the interleaved PWM control is verified by current flowing at equivalent circuit frequency of 4.5 kHz.

The step-downcircuit operation results are shown at Fig. 14 with cell 1 and 6 wave forms. The resonant current frequency is 4.1 kHz is shown on Fig. 14 (i) with 1 kHz upper cells switching frequencies. By the interleaved PWM the operating frequencies is increased and consider to resonance frequency it is four times higher as switching frequencies. At cell 6 under lower stack the cell current is 4 kHz which shown in Fig. 14 (ii). At cell 6 on switched off state the current value is zero with clamping IGBT. On cell 6 cell capacitor voltage is higher to the voltage with clamped diode which remains still at 2.5 kHz.

Linearity tests: Linearity test for step-up operation is tested with output voltage versus input voltage at constant charging ratio of d = 0:7 which explained in the Fig. 15. On this the circuit shows the output and input voltages linear relationships by comparing an offset with ideal cases. On the downscaled prototype results the noticeable relative error shows the low input voltage and other step up operations on for linearity is shown in Fig. 16. From this Fig. 16 the relative errors for step-down ratio can be minimized by increasing the input voltage with ideal values.

Closed-loop tests: The regulation properties of the converter is tested by applying closed-loop control and Fig. 17 shows the experimental wave forms for step-up conversion with input voltage v_L = 30 V.

On open loop control the value of d = 0.6 which is seen in Fig. 11 by which the value of d in closed loop is

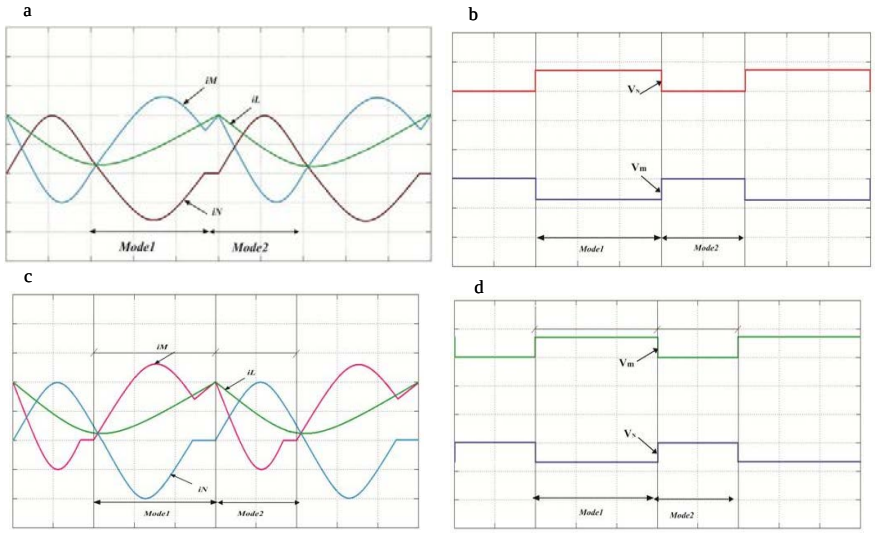

Fig. 11: Simulated and Experimental results of the proposed regular multi-stage step-up dc-dc converter (X-axis: Time, 60 μs/div). Simulated Output:(i) Currents (Y: Current magnitude, 3 A/div). (ii) Voltages (Y: Voltage magnitude, 150 V/div). Experimental Output: (iii) Currents (Y: Current magnitude, 2 A/div). (iv) Voltages (Y: Voltage magnitude, 150 V/div

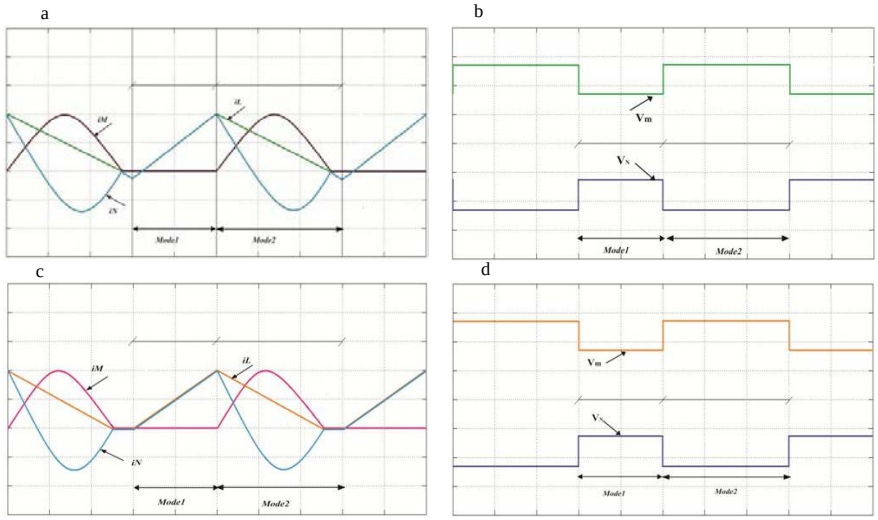

Fig. 12: Simulated and experimental results of the proposed regular multi-stage step-down dc-dc converter (X: Time, 100 μs/div) Simulated Output: (i) Currents (Y: Current magnitude, 3 A/div). (ii) Voltages (Y: Voltage magnitude, 150 V/div) Experimental Output:(iii) Currents (Y: Current magnitude, 3 A/div). (iv) Voltages (Y: Voltage magnitude, 150 V/div)

higher that is rose by the controller. By the output step-up conversion ratio is 10:2 with high voltage v_H at almost 300 V. The observation shows that by the effective closed loop control the peak voltage rated across the value 300 V. The step-down conversion with closed loop control results, such as experimentally obtained waveforms of current and voltage are demonstrated in Fig. 19. It has the fixed input voltage with: v_H = 300 V compared the open loop control at d = 0.7 by which the closed controller is reduced and the closed loop control's experimentally measured output voltage observation is shown on Fig. 20. The performances of the closed loop controller are effective when the low voltage values are at 30 V. The capacitor voltages are also calculated with input

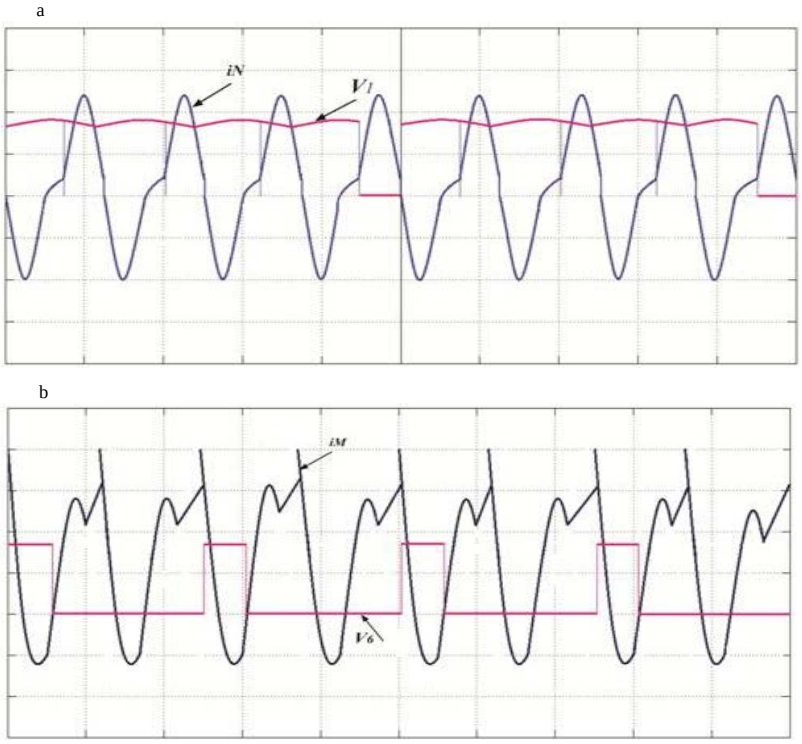

Fig. 13: Experimental results of step-upcurrent and voltage of the clamped switchsub-module (X: Time, 100 μs/div)at (i) Cell 1(Y: Current magnitude, 3 A/div) (ii) Cell 6 (Y: Voltage magnitude, 70 V/div)

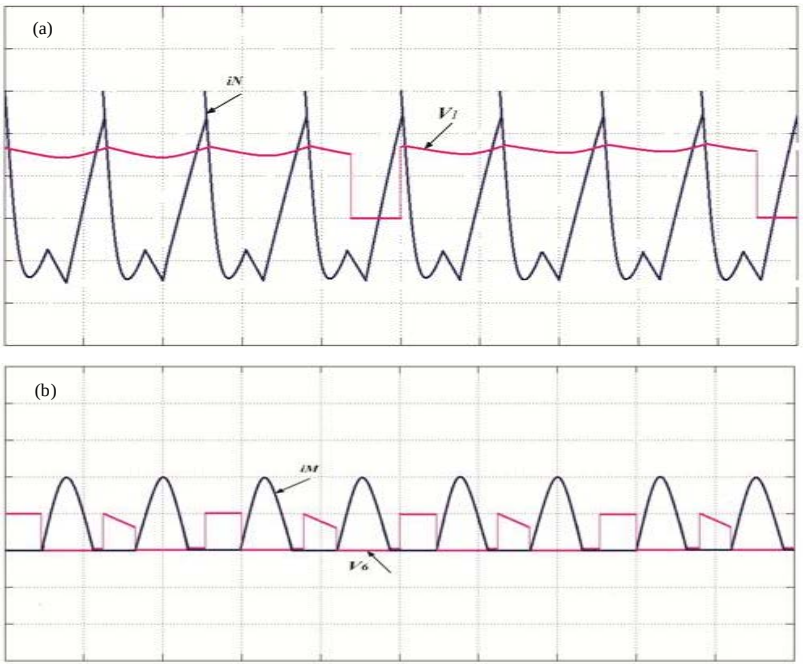

Fig. 14: Experimental results of step-downcurrent and voltage measure of theclamped switch sub-module (X-axis: Time, 300 μs/div)at (a) Cell 1(Y-axis: Current magnitude, 3 A/div) (b) Cell 6 (Y-axis: Voltage magnitude, 100 V/div)

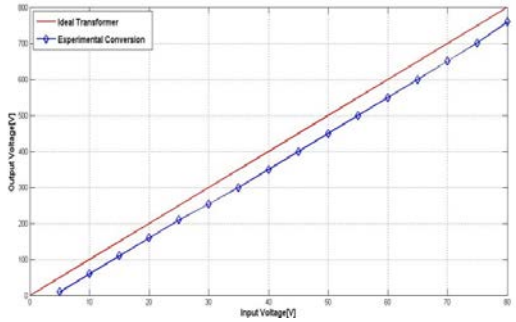

Fig.15: Experimentally evaluated step-up operation withpeak voltages versus various input low voltages

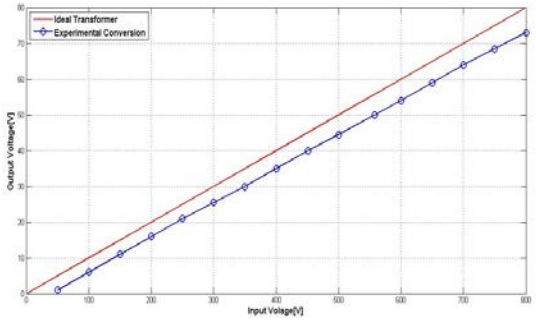

Fig. 16: Experimentally evaluated step-down operation with low voltages versus various input peak voltages

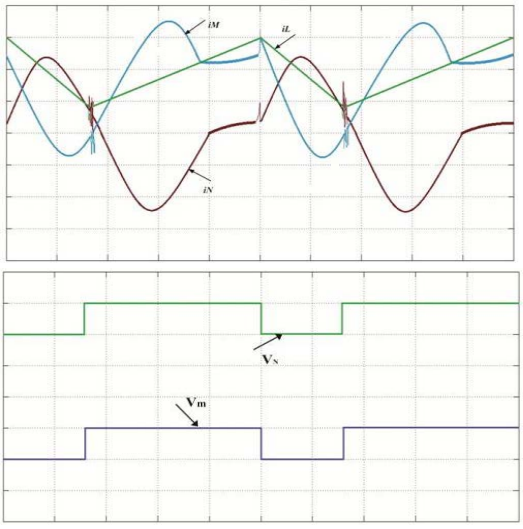

Fig.17: Experimental results of the closed-loop operation of step-up converter (X: Time, 100 μs/div) (i) Currents (Y: Current magnitude, 3 A/div) (ii) Voltages (Y: Voltage magnitude, 150 V/div)

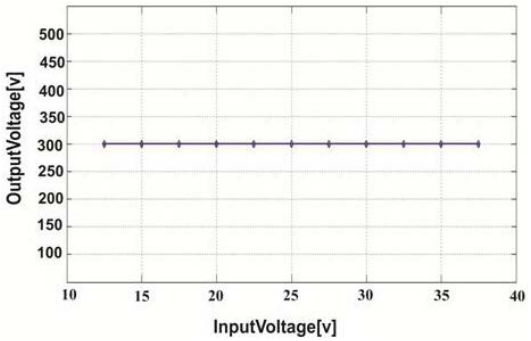

Fig.18: Experimentally evaluated closed-loop control step-up voltages

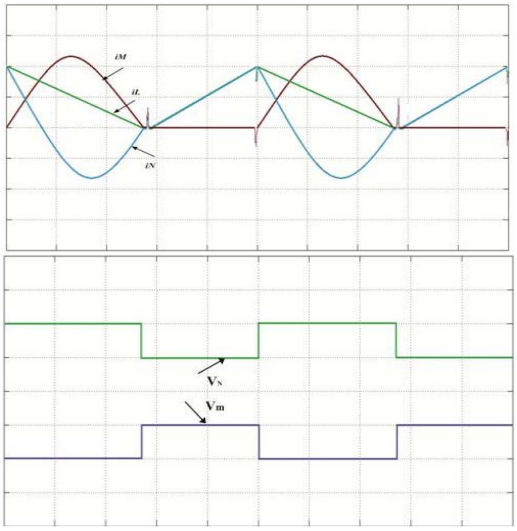

Fig. 19: Experimental result of the closed-loop control operation of step-down converter (X: Time, 100 μs/div). (i) Currents (Y: Current magnitude, 3 A/div) (ii) Voltages (Y: Voltage magnitude, 150 V/div).

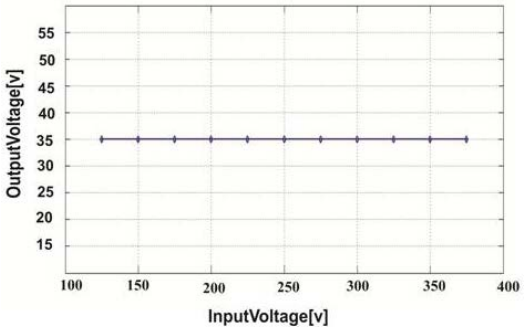

Fig. 20: Experimentally evaluatedvoltages ofclosed-loop controlduring step-down operation

voltage conditions which are balanced with upper sub-modules voltages as well as the lower sub-modules voltages.

CONCLUSION

In this study we examined and presented the efficiency of new transformer less MMC dc-dc converter. It is arranged in series with two stacks of sub modules supported by high voltage. The sub modules with dc capacitors were also used for resonant operation in which the proposedregular multistage dc-dc converter proves the ability of bidirectional conversion. To demonstrate the performance of the proposed work step-up and the step-down operations were implemented under various stages. In which under open loop the converter with dc transformer shows better linearity and at closed loop control is implemented for trimming the resultant voltage. The operational principle of the proposed system is examined under bench scale experimental prototype which has high losses. This is due to high current in sub-modules but it is proved effective for high voltage applications.

RECOMMENDATIONS

The future work can be carried to enhance the performance by lowering the switching frequency on the case were the cell capacitors requires high volumes. Thus proved that the proposed work is has the capacity of regularity, scalability and simplicity that works effectively on some special applications.

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