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Hard Switching Versus Soft Switching-Case Study on Positive Output Elementary Super Lift Luo Converter

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Abstract: Luo converter is a developed converter which transfers the voltage based on lifting and achieves a high voltage gain in geometric progressive law. Researchers show more interest on control of Luo family converters while their procedural steps involved in design is not detailed to gratify the beginner in the field. In regulated power supply applications, Luo converters are more preferred if they operated in soft switching mode. Soft switching techniques like Zero Voltage Switching (ZVS) has reduced switching losses and hence improved efficiency and life of power semiconductor switches. This study takes up and provides complete design of Positive Output Elementary Super Lift Luo Converter (POESLLC) for the 25.92 W rating, firstly. Secondly, the performance evaluation of ZVS based POESLLC over hard switched POESLLC is aimed. Proportional Integral (PI) control of POESLLC for hard switched and ZVS switching are compared in MATLAB-simulink platform.

Key words: Luo converter, POESLLC, soft switching, voltage lift, ZVS

INTRODUCTION

Switched-mode dc-to-dc converters are used to convert the unregulated dc input into a controlled dc output at a desired voltage level. dc-dc converters are widely used for traction drives in electric automobiles, trolley cars, marine hoists, forklift trucks, mine haulers, communication devices etc. Switching converters have been in existence since 1950 s for the applications varying their ranges from power supplies to DC motor drives. Switching power supplies demand higher energy efficiency, a higher power packing density and reduced Electromagnetic Interference (EMI). To consider the ever increasing requirements for smaller size, lighter weight, higher voltage transfer gain and higher efficiency power supplies, switched-mode power conversion technologies have evolved from basic Pulse-Width-Modulated (PWM) converters to resonant converters, quasi-resonant converters (QRCs), Multi-Resonant Converters (MRCs) converters etc (Luo and Hong, 2006; Luo and Fang, 2004). Even though the performance parameters of the converter can only be improved by control techniques, higher voltage transfer gain is inherent characteristics of topology of the converter. A higher voltage transfer ratio with reduced ripple content is achieved in Luo converter in simple structure (Luo and Ye, 2003a, b). Luo converter is a developed converter, introduced by Fang Lin Luo in 1977. In Positive Output Elementary Super Lift Luo Converter (POESLLC), the voltage increases in geometric progression (Luo and Ye, 2003).

For the simplicity of analysis, converters are operated under continuous conduction mode. However PWM POESLLC converter under discontinuous conduction mode, a detailed analysis has been presented (Zhu and Luo, 2004). Increasing switching frequency or size of energy storing elements will make the converter in continuous conduction mode and reduced ripple content at the output. With increased frequency hard switching operation, semiconductor switches experience high switching losses (Mohan *et al*., 2006). This will restrict the converters from operating at a higher frequency and hence, the mission towards size/weight reduction and performance improvement is impeded. Soft switching technique has improved the switching frequency of the same converter with reduced switching losses (Marian and Czarkowski, 2011). The design procedure for very high frequency resonant boost converters has been given (Burkhart *et al*., 2013). The POESLLC is a new series of

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dc-to-dc converters having high voltage transfer gain, high power density, high efficiency, reduced ripple voltage and current. These converters effectively enhance the voltage gain in power-law terms (Luo and Ye, 2003ab).

Having reviewed the literature exhaustively it is understood that the progressive converters like POESLLC has not been treated well to enable the researchers to commence their study. The basic operation, performance indices (voltage ripple etc.,) application specific designs etc. may enlighten their study further. This study provides a detailed design procedure for POESLLC after detailing the mode diagrams based working. The design is followed by a development of Proportional-Integral (PI) controller based POESLLC system implemented in MATLAB-Simulink. The performance difference between ZVS and hard switched systems are well demonstrated using the results such as ripple voltage and transient start-up etc.

MATERIALS AND METHODS

Proposed PI controller based system: The proposed PI controller based system consists of a resonant switch added in the converter as shown in Fig. 1 so the working is under soft switching. The resonant inductor L_r and C_r form a series resonant circuit. When observing from switch terminal due to resonance the voltage across the circuit including switch, resonant circuit and source will swing to obtain a zero crossing instant.

POESLLC under PWM switching: The Pulse-With-Modulation (PWM) is the simplest triggering method for attaining different voltage levels for different duty ratio. It has frequency limitations in the converters due to increased switching losses. The abrupt discharges of energy stored in semiconductor switches are the cause of this limitation. A small signal energy factor and mathematical model for dc-dc converter is given (Luo and Ye, 2007). The two basic modes of operation of the converter under PWM operation is shown in Fig. 2ab. Super-lift luo-converters with capacitor voltage drop is given (Luo, 2008).

The voltage lift technique opens a good way to improve circuit characteristics (Luo, 1999). After long-term research this technique has been successfully applied for dc-to-dc converters. Positive output Luo converters are a host of relatively recent dc-to-dc step-up (boost) converters which were developed from prototypes using voltage lift technique by Luo. In simple structure the Luo converters will give an output voltage with fewer ripples. The other similar category of Luo converters are called Negative Output Super Lift Luo Converters (NOSLLCs). Its output voltage is negative with respect to input voltage. NOSLLC and reduced-order sliding mode controller plus proportional double integral controller for negative output elementary super-lift Luo-converter are given (Luo and Ye, 2003ab; Kumar and Jeevananthan, 2010, 2013).

The POESLLC consists of dc supply voltage V_{in}, capacitors C_1 and C_2, inductor L_1, power switch (n-channel MOSFET) S, freewheeling diodes D1 and D2 and load resistance R is shown in Fig. 2. When the switch S is closed, voltage across the capacitor C_1 is charged to V_{in}. The current i_{L1} flowing through inductor L_1 increases with voltage V_{in} as indicated in Fig. 3. When the switch S is opened, current decreases with voltage (V_o -2V_m) as shown in Fig. 3. The ripple in inductor current i_{L1}.

$$\Delta_{iL1} = \left(\frac{V_{in}}{L_1}\right)dT = \left(\frac{V_o - 2V_{in}}{L_1}\right)dT \quad (1)$$

$$V_o = \left(\frac{2-d}{1-d}\right)V_{in} \quad (2)$$

Voltage transfer gain is:

$$G = \left(\frac{V_o}{V_{in}}\right) = \left(\frac{2-d}{1-d}\right) \quad (3)$$

In steady state, the average charges across capacitor C_1 should not change. We have the following relations:

$$i_{in-off} = i_{L1-off} = i_{C1-off}, i_{in-on} = i_{L1-on} + i_{C1-on} \quad (4)$$

When inductance L_1 is large, i_{L1} is nearly equal to average current i_{L1}. Therefore:

$$i_{in-off} = i_{L1} = i_{C1-off}, i_{in-on} = i_{L1} + \frac{1-d}{d}\frac{i_{L1}}{d} \quad (5)$$

$$i_{C1-on} = \frac{1-d}{d}i_{L1} \quad (6)$$

Average input current:

$$I_{in} = di_{in-on} + (1-d)i_{in-off} = i_{L1} + (1-d)i_{L1} = (2-d)i_{L1} \quad (7)$$

Considering:

$$T = \frac{1}{f} \quad (8)$$

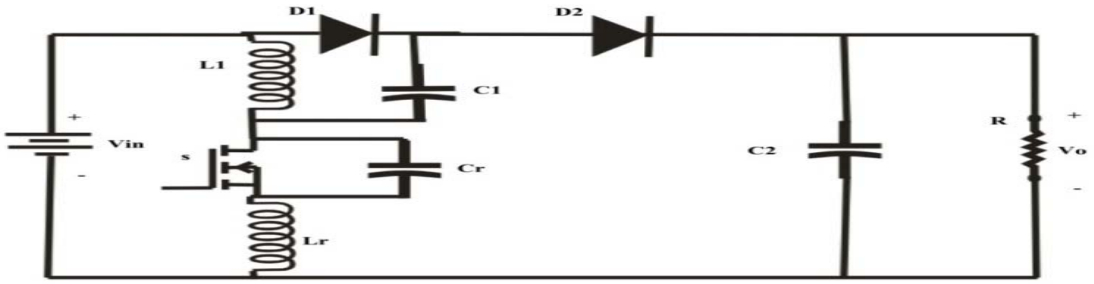

Fig.1: Circuit diagram of ZVS POESLLC

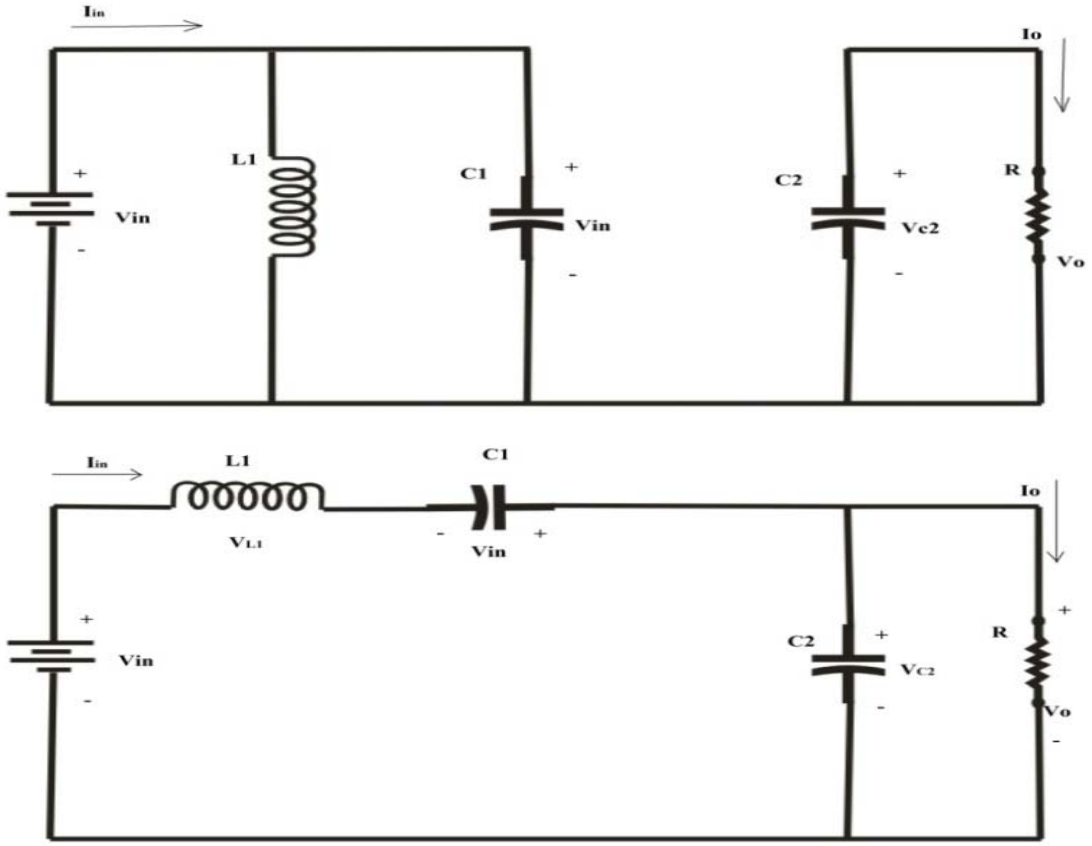

Fig. 2: POESLLC modes of operation

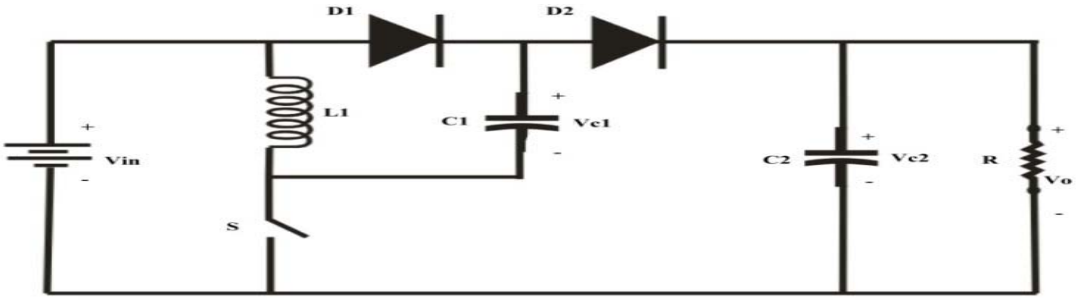

Fig. 3: Circuit diagram of POESLLC

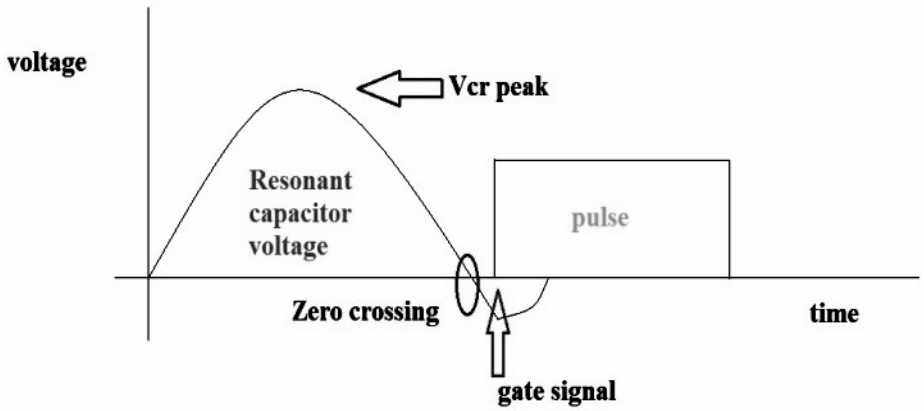

Fig. 4: Theoretical waveform showing ZVS operation

$$\frac{V_{in}}{I_{in}} = \left(\frac{(1-d)}{(2-d)}\right)^2 \frac{V_o}{I_o} = \left(\frac{(1-d)}{(2-d)}\right)^2 R \qquad (9)$$

The variation ratio of inductor current i_{L1} is:

$$\xi = \frac{\Delta_{iL1/2}}{i_{L1}} = \frac{d(2-d)TV_{in}}{2L_1I_{in}} = \frac{d(1-d)^2}{2(2-d)}\frac{R}{fL_1} \qquad (10)$$

The ripple voltage of output voltage Vo is:

$$\Delta_{Vo} = \frac{\Delta Q}{C_2} = \frac{I_o(1-d)T}{C_2} = \frac{(1-d)}{fC_2}\frac{V_o}{R} \qquad (11)$$

Therefore, the variation ratio of output voltage V_o is:

$$\xi = \frac{\Delta_{VO}/2}{V_o} = \frac{(1-d)}{2RfC_2} \qquad (12)$$

POESLLC Under ZVS switching: The Zero Voltage Switching (ZVS) is one of the soft switching methods implemented to improve the switching efficiency. The converter can be operated at a high switching frequency using ZVS. In ZVS the voltage across the switch is shaped and it is operated to near zero voltage to minimize the losses (Jayashree and Uma, 2011abc). The voltage across switch is shaped as shown in the Fig. 4. The successful operation of ZVS in Luo and Ultra Lift Luo converters is given in study (Jayashree and Uma, 2011abc).

The closed loop operation of dc-dc converter with a VCO is shown in Fig. 5 for ZVS operation. The PI-ZVS POESLLC circuit is shown in Fig. 1 and four basic modes of operation with appropriate current direction is shown in Fig. 6.

In ZVS quasi resonant converters, the transistor peak current is identical to that of PWM converters. However, the transistor peak voltage is much higher than that of PWM converters which requires a MOSFET with a higher breakdown voltage. Such MOSFETs have a higher on-resistance, causing a higher conduction loss (Kazimierczuk, 2008).

$$P_{rDS} = r_{DS}I_{Srms} \qquad (13)$$

Design of proposed converter

Design: Commercial controllers can operate each phase at a switching frequency in the MHz range, resulting in effective size reduction. The Luo converter is designed for 12 V input voltage, 100 KHz. For 50% duty cycle the output voltage of the POSLLC is shown in Fig. 7-9

$$V_o = \left(\frac{2-d}{1-d}\right)V_{in} \qquad d = 0.5 \qquad (14)$$

The V_o= 36 V, Let Load resistance, R = 50 Ω, Output Current, I_o= 0.720 A, Output Power, $P_o = V_oI_o$= 25.920 W, Let the efficiency be 91.79%. So:

$$\text{Input Power } P_{in} = \left(\frac{P_0}{\eta}\right)28.238W \qquad (15)$$

Input Current, I_{in}= 2.353A, Inductor ripple current is 25% of input current, so ΔI_{L1}=0.6A

$$L_1 = \left(\frac{V_{in}}{f\Delta i_{L1}}\right)d = 100uH \qquad (16$$

Capacitor ripple voltage is Δv_o = 0.16 V

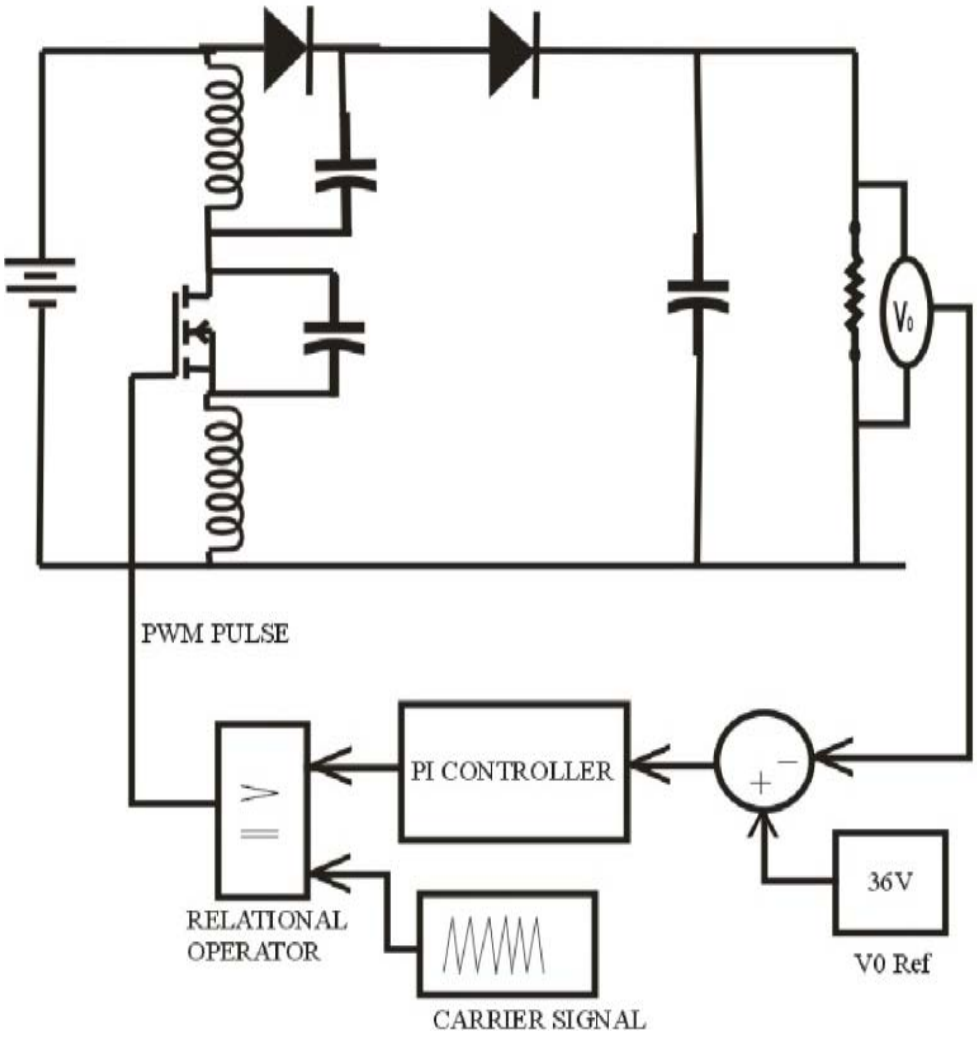

Fig. 5: Block diagram for closed loop operation of ZVS-POESLLC

$$C_o = \left(\frac{1-d}{f\Delta V_o R}\right)V_o = 22.5uF \quad (17)$$

Co= C1 = 22.5 uF. ence the design parameters are tabulated (Table 1).

PI control: The design and analysis of a PI control for POESLLC is given. PI controller is modeled using operational amplifier. The values of proportional gain, Kp and integral time, T_I of the controller are determined using Ziegler-Nichol's tuning method. For triggering the converter, variable pulse generator is used:

$$\text{Resonant frequency} = f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (18)$$

Table 1: Design parameters for POESLLC

Parameter name	Symbol	Value
Input voltage	V_{in}	12 V
Output voltage	V_o	36 V
Inductor	L_1	100 µH
Capacitors	C_1, C_2	30 µF
Nominal switching frequency	f_s	100 KHz
Load resistance	R	50 Ω
Output power	P_o	25.92 W
Input power	P_{in}	28.32 W
Average input current	I_{in}	2.361 A
Efficiency	η	91.56%
Average output current	I_o	0.72 A
Duty ratio	d	0.5
Peak-to-peak inductor current	Δi_{L1}	0.6 A
ripple	ΔV_o	0.16 V
Peak too peak capacitor ripple		

$$\text{Characteristic impedance } Z_o = \sqrt{\frac{L_r}{C_r}} \quad (19)$$

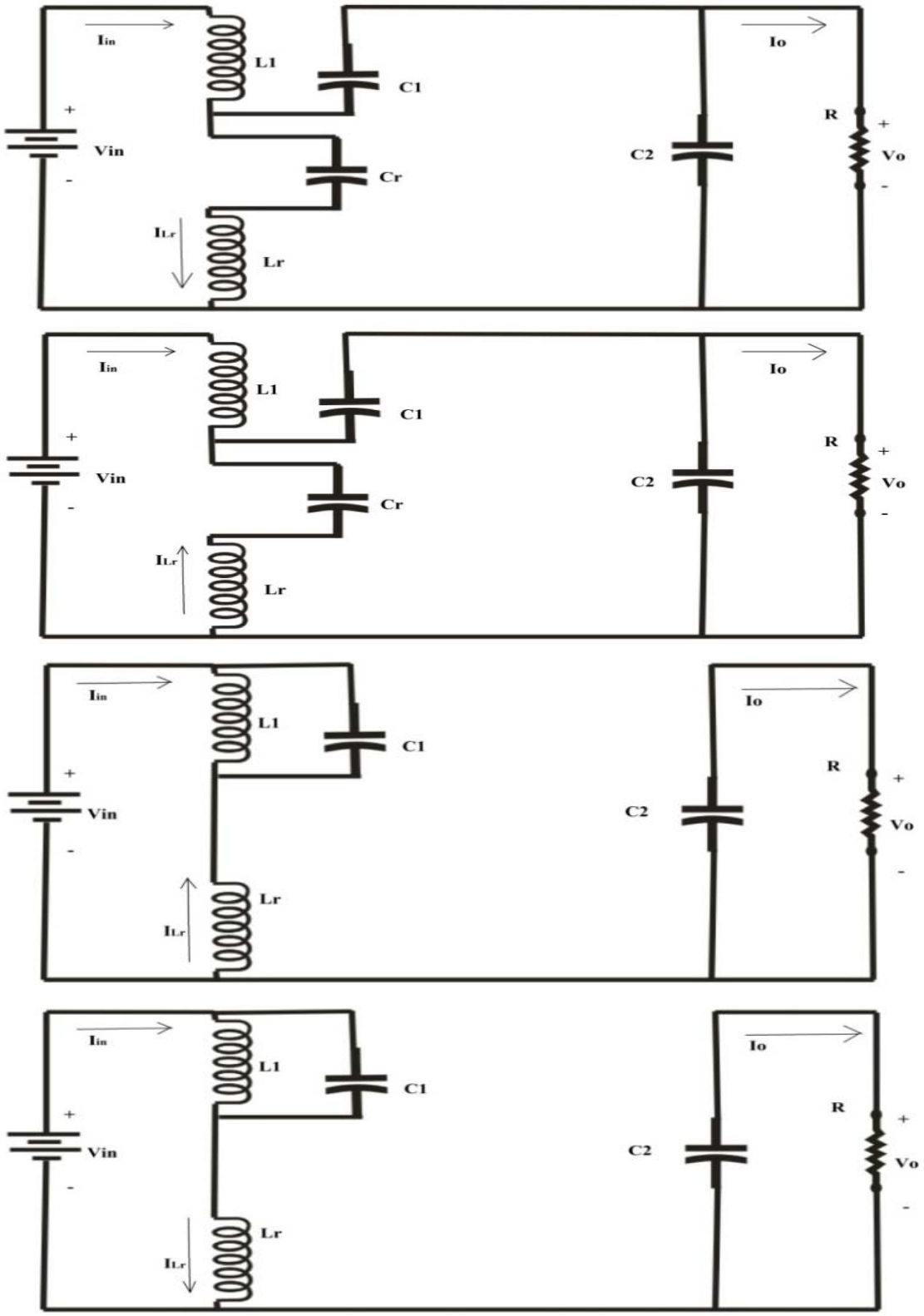

Fig. 6: ZVS-POESLLC modes of operation

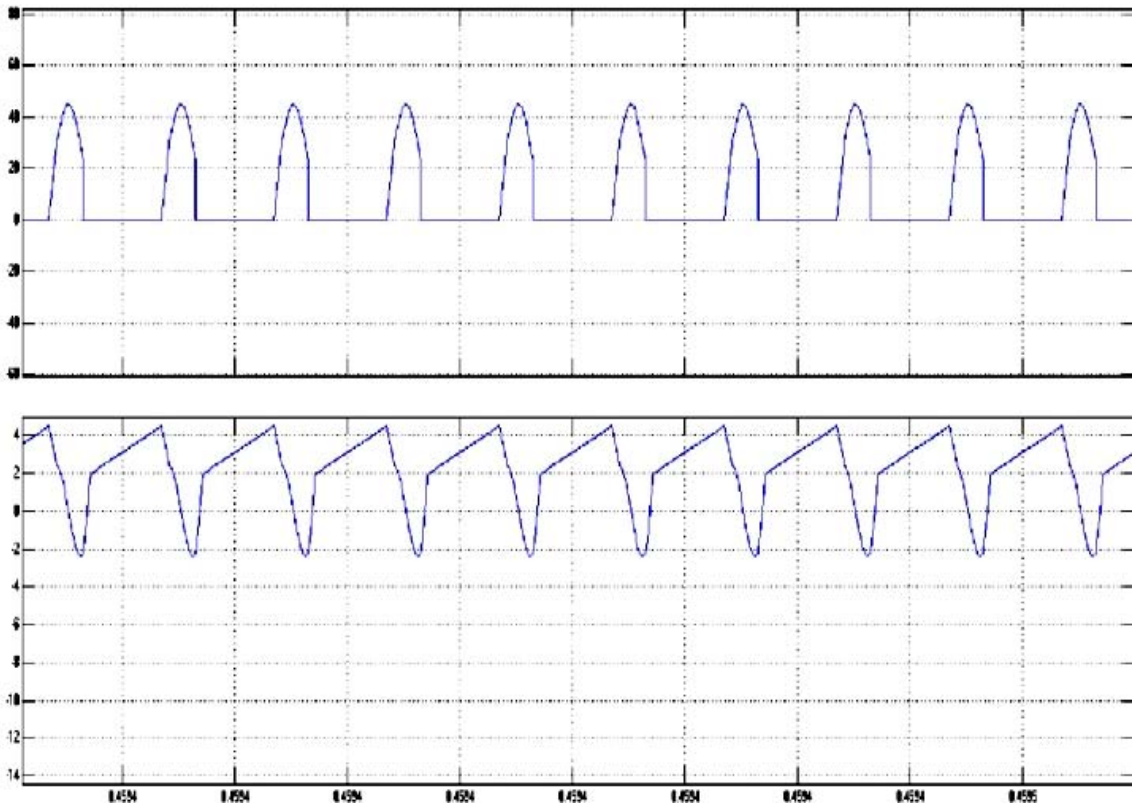

Fig.7: Simulated resonant capacitor voltage and resonant inductor current of ZVS-POESLLC

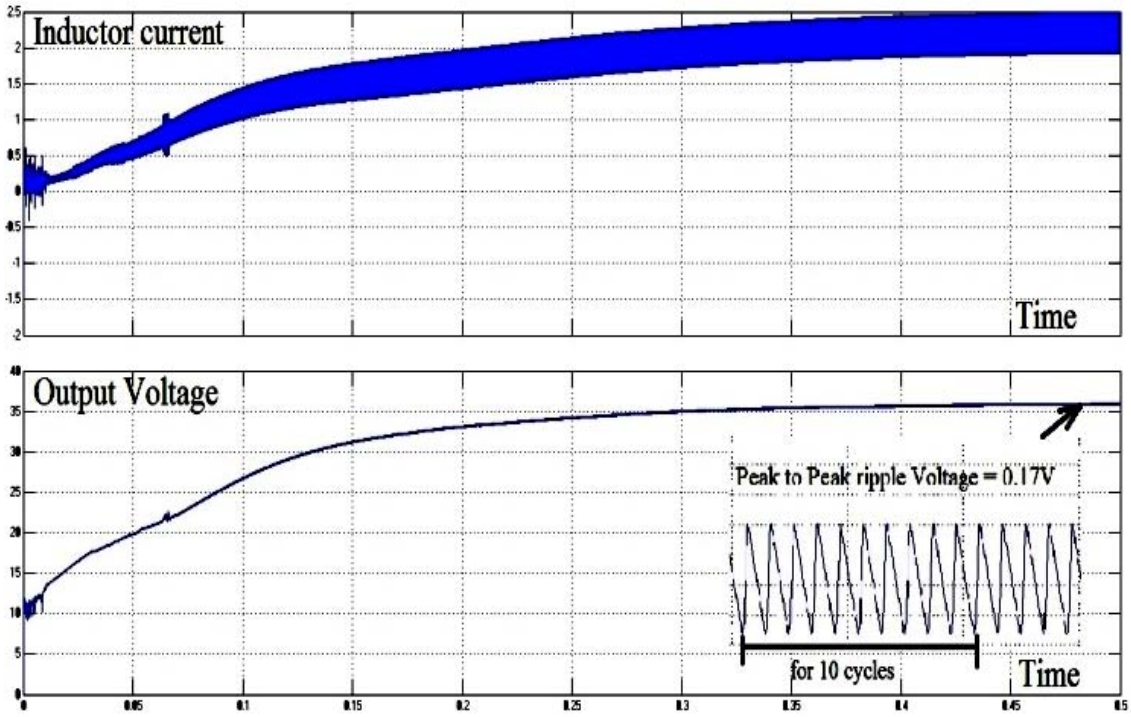

Fig. 8: Output voltage and inductor current for start-up transient of ZVS-POESLLC

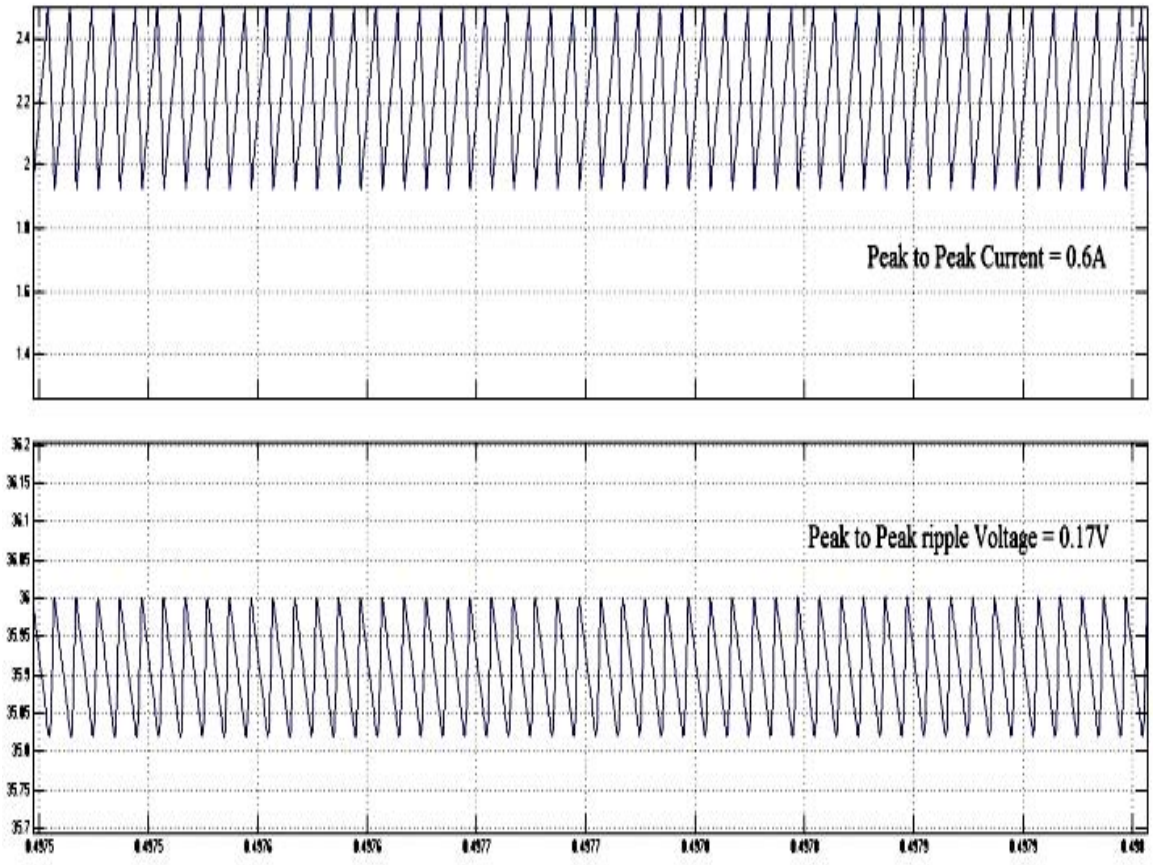

Fig. 9: Output voltage and inductor current in steady state region of ZVS-POESLLC

Condition for ZVS is:

$$I_M Z_o \geq V_{in} \quad (20)$$

DC voltage transfer function is:

$$M_{VDC} = \frac{V_O}{V_{in}} = 3 \quad (21)$$

Let $Q = M_{VDC} = 3$

$$M_{VDC} = \frac{1.1}{f_s / f_o} \quad (22)$$

f_o = 272.727 Khz Characteristic impedance, $Z_0 = R_L/Q = 16.666$:

$$L_r = \frac{R_L}{\omega_o Q} = 9.726\text{uH} \quad (23)$$

$$C_r = \frac{Q}{\omega_O R_L} = 35.014\text{nF} \quad (24)$$

Peak switch current, ISM = MVDCIO = 2.16A (25)

RESULTS AND DISCUSSION

The designed converter is simulated in MATLAB-simulink platform. Simulink is graphical multi-domain simulation and Model-Based Design for dynamic and embedded systems shown in Table 2. The output voltage for PI-ZVS POESLLC is shown in Fig.10. For an input voltage of 10 V the PI controller regulates the output voltage to reference voltage of 36 V. This is achieved under zero voltage soft switching condition.

Table 2: Ripple voltage for a range of load variation

Load current, i_l	Theoretical ripple voltage	Simulated ripple voltage for hard switching	Simulated ripple voltage for soft switching
0.90	0.15	0.20	0.23
0.80	0.13	0.18	0.20
0.72	0.12	0.15	0.18
0.65	0.11	0.14	0.17
0.60	0.10	0.12	0.15

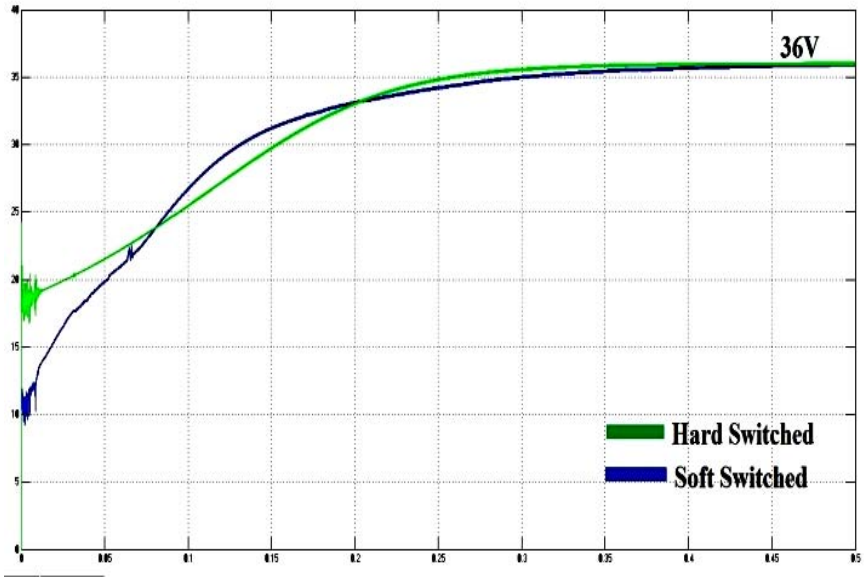

Fig. 10: Output voltage comparison of hard and soft switched POESLLC

CONCLUSION

In this study, the ZVS-POESLLC is compared with POESLLC analyzed and designed. The proposed topology and control technique may be used in industrial applications requiring regulated output voltage. The Positive Output Elementary Super Lift Luo Converter (POESLLC) performs the voltage conversion from positive source voltage to positive load voltage. Due to the time variations and switching nature of the power converters, their dynamic behavior becomes highly non-linear. This studyr has successfully demonstrated the design, analysis and suitability of PI-ZVS controlled positive output elementary super lift Luo converter for much efficient operation and high frequency. The positive output elementary super lift Luo converter with PI-ZVS control thus claims its use in applications such as computer peripheral equipment, switch mode power supply, medical equipments and industrial applications, especially for high voltage application etc.

REFERENCES

Burkhart, J.M., R. Korsunsky and D.J. Perreault, 2013. Design methodology for a very high frequency resonant boost converter. IEEE. Transac. Power Electron., 28: 1929-1937.

Jayashree, E. and G. Uma, 2011a. Analysis, design and control of zero-voltage switching quasi-resonant -positive output super lift Luo converter. IET. Power Electron., 4: 21-28.

Jayashree, E. and G. Uma, 2011b. Design and implementation of zero-voltageswitching quasi-resonant positive-output Luo converter using analog resonant controller UC3861. IET. Power Electron., 4: 81-88.

Jayashree, E. and G. Uma, 2011c. Soft-switched-controlled-ultra lift Luo converter. IET. Power Electron., 4: 151-158.

Kazimierczuk, M.K., 2008. Pulse-Width Modulated DC-DC Power Converters. John Wiley and Sons, New Delhi, India, ISBN: 9780470694657, Pages: 808.

Kumar, K.R. and S. Jeevananthan, 2010. PI control for positive output elementary super lift Luo converter. Int. J. Electr. Electron. Eng., 4: 440-445.

Kumar, K.R. and S. Jeevananthan, 2013. Design and implementation of reduced-order sliding mode controller plus proportional double integral controller for negative output elementary super-lift Luo-converter. IET. Power Elec., 6: 974-989.

Luo, F.L. and H. Ye, 2003b. Negative output super-lift converters. IEEE. Transac. Power Electronics, 18: 1113-1121.

Luo, F.L. and H. Ye, 2003a. Positive output super-lift converters. IEEE. Transac. Power Electron., 18: 105-113.

Luo, F.L. and H. Ye, 2007. Small signal analysis of energy factor and mathematical modeling for power dc-dc converters. IEEE. Transac. Power Electron., 22: 69-79.

Luo, F.L. and L.L. Fang, 2004. Advanced DC/DC Converters. CRC Press, New York, USA.,.

Luo, F.L. and Y. Hong, 2006. Essential Dc-Dc Converters. Taylor and Francis Group, New York, USA., ISBN: 9780849372384, Pages: 420.

Luo, F.L., 1999. Positive output Luo converters: Voltage lift technique. IEEE. Proc. Electr. Power Appl., 146: 415-432.

Luo, F.L., 2008. Analysis of super-lift Luo-converters with capacitor voltage drop. Proceedings of the 2008 3rd IEEE Conference on Industrial Electronics and Applications, June 3-5, 2008, IEEE, Singapore, ISBN: 978-1-4244-1718-6, pp: 417-422.

Marian, K.K. and D. Czarkowski, 2011. Resonant Power Converters. John Wiley and Sons, Hoboken, New Jersey, USA.,.

Mohan, N. and U.M. Tore, W.P. Robbins, 2006. Power Electronics: Converters, Applications, and Design. John Wiley and Sons, Hoboken, New Jersey, USA.,.

Zhu, M. and F.L. Luo, 2004. Analysis of positive output super-lift converter in discontinuous conduction mode. Proceedings of the International Conference on Power System Technology, November 21-24, 2004, IEEE, New York, USA., ISBN: 0-7803-8610-8, pp: 828-833.