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Area and Power Optimized Hardware Design of Bi-Phase Space Coding/Phase Coding Technique for Wireless Sensor Applications

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Abstract: Wireless sensor nodes are used in wide range of applications. Most of them require short range communication. Phase Code (PC) or Bi-Phase Space Code (BPSC) can be used for this communication. Wireless sensor nodes has to be compact and should require less power. Half duplex communication can be used for the Wireless Sensor Network (WSN). In this study, Phase/Bi-Phase Space Code Generation and Degeneration technique is designed in a single system. Based on the control inputs, the operation of the system can be selected. Both systems are using the same hardware. Number of transistors is reduced from 66-55 (reduced by 16.66%). This system was designed and analyzed using Cadence 180 nm technology. Power consumption is reduced around 15% and it depends on the operating frequency and operation of the system. This system occupies 22.94×65.705 μm^2 (reduced by 61.93%).

Key words: Phase Code (PC), Bi-Phase Space Code (BPSC), VLSI, low power, WSN

INTRODUCTION

Now a days, Wireless Sensor Networks are used in wide range of applications. Lot of Issues are present in Wireless Sensor Networks (Gowrishankar and Basavaraju, 2008). Sensor networks are modified ad-hoc networks. This article distinguish the WSN from ad-hoc network. Distance between each nodes will be less. So short range communication is enough for most of the WSN. Phase/Bi-phase space coding can be used for this short range communication. Bi-Phase Space code generator/Phase code generator can be designed with full hardware utilization (Lee and Pan, 2015) code generation for both coding techniques can be done through this system. This system was designed in 180 nm technology. Reference (Lee *et al*., 2015) deals with the FM0/Manchester Codec with fully utilized hardware. The Encoder and Decoder parts have been discussed in this research.

Motivation of our proposed system is as follows. Nodes of WSN has to be compact and should consume less power. Because they are powered with battery supply. The life time of the sensor node depends on the battery life time. Miniaturization in chip area and power reduction are the required tasks to be carried out in this system. Sensor nodes will be having a transceiver to communicate with the central unit. Sensor nodes can use RF communication for this purpose. Code Generation and Degeneration has to be carried out at the transmitter and receptor. PC technique or BPSC technique can be used for coding operation. In general, sensor nodes will be enabled with a single coding technique. If the user wants to use another coding, the system will fail to fulfill the requirement. The entire system has to be replaced. The complexity and cost of the design of miniaturized system is quite high. Replacement causes much loss due to this.

Code Generation and Degeneration operations aren't separable. Many designs have been proposed for Generation and Degeneration operations. Most of them deal with encoder or decoder as discussed in research (Lee *et al*., 2015). In general, WSN uses Half-Duplex communication. Transmission or Reception will be present in the transceiver. Because of this nature, PC and BPSC can be combined in a single system. A single Coding system is capable of doing Generation and Degeneration operations for both coding techniques. The existing system has 2-1 Multiplexer, Latch, XNOR logic, Inverter, D-Flip Flop in its architecture design and makes use of 66 transistors. Area requirement is33 X 120 μm^2. In the proposed system, all designs are optimized to get an optimized system as shown in the reference (Jeslin and Rajakumar, 2015). Pass Transistor Logic (PTL), Transmission Gate Logic (TGL) and other MOS configurations can be used to design each modules

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(Mishra *et al*., 2010, Markovic *et al*., 2000; Heo *et al*., 2007). The proposed system is designed with 55 transistors and requires 22.94×65.705 μm^2. Transistor count is reduced by 16.66%. Area requirement is reduced by 61.93%. Power consumption is also 15% lower than the existing system. Quantum dot Cellular Automata (QCA) is a new paradigm in nanotechnology. It can be used to increase the speed, reduce the area and power consumption (Lakshmi *et al*. 2015). Flip Flops and Shift Registers can be designed with QCA. This can be applied in the future.

Background of pc and BPSC: BPSC generation has separate representations for binary '1' and '0'. Binary '1' is represented by a constant voltage in a clock cycle and binary '0' is represented by a transition in the middle of the bit window. i.e., to represent binary '0' there is a transition in each half clock cycle and to represent binary '1' there is a single transition at the end of each full clock cycle. If the input has large number of high bit values, the output will be having less number of transitions. Bi-Phase Space code degeneration is done by inversing the operation. If the input has transitions within a clock cycle, the output will be binary '0' and if there is no transition within a clock cycle the output will be binary '1'. PC Generation has at least one transition per clock cycle. In phase code generation, the input data will be XORed with the input clock signal. Since there is a transition per clock cycle, clock synchronization at the receiver side is easy. But, phase code consumes wider bandwidth than BPSC. Phase code degeneration is done by XORing the encoded data with the clock signal.

MATERIALS AND METHODS

Proposed schematic: The proposed schematic is designed using 2-1 selector, match finder logic, positive level D-Latch, Positive Edge D Flip-Flop and Inverter. Selector logic can be designed using Transmission gates. About 2 to 1 selector design using transmission gates require 6 transistors. Pass Transistor logic can be used to reduce this transistors from 6-4 with voltage degradation in the output. The previous design makes use of 10 transistors for the Latch design. D-Latch can be designed using 7 transistors. D-Flip Flops are designed using 22 transistors which can be reduced to 16 transistors. Overall, our proposed system is designed with 55 transistors. Transistors are optimized in width to reduce area requirement.

Optimized selector: Selector can be designed using multiple logics. CMOS design of 2 to 1 selector requires 10 MOS devices to design the circuit. The usage of Transmission Gate Logic (TGL) reduces the transistor count from 10 to 6. TG logic for 2 to 1 selector is shown in Fig. 1. The response of the 2-1 selector shows that, when the select input(s) is high, 'A' input will be selected and when the select input(s) is low, 'B' input will be selected.

The transistors required for the design of 2-1 Selector can be reduced to 4 using the Pass Transistor Logic (PTL) as shown in the Fig. 2. While using pass logic, the threshold voltage of the MOS device will be dropped. This can be understood from the response of the selector using pass transistor. The input signal has 1.8V as Vmax and the output signal has 1.2V as Vmax. A Buffer or an inverter is required at the output stage to compensate the degradation. TG logic is used for selector design. PT logic is used where the next stage of the circuit has inverter at the entry.

Optimized positive level D-Latch: In previous papers, about Phase/Bi-Phase space coding, the Latch was designed using 10 transistors. Proposed system require 7 transistors for the Latch design as shown in Fig. 3. So, 3 transistors can be reduced here. D (Data), clk (Clock) and Q (Latch output) are the three pins used here. The operation of the positive level D-Latch is as follows. The latch is transparent, when the clock input is high and it acts as memory when the clock input is low.

Optimized match finder schematic: In general, two input Match Finder will be designed using 8 transistors, proposed system uses PT logic with pull up and pull down devices to get match finder logic with 6 transistors as shown in Fig. 4. So, 2 transistors can be reduced by this design. The output is high, when both the inputs are same and the output is low when both the inputs are different. D-Flip Flop will be designed using 22 transistors (Mohideen and Perinbam, 2006). In the resesrch, D-Flip Flop with 16 transistors is used as shown in Fig. 5. Optimized D Flip Flop reduces 6 transistors from the previous design.

Positive edge triggered D-Flip Flop is used in our paper. In our design, it has two inputs. Data input (D) and clock input (clk) are provided as inputs and the output (Q) is obtained from the circuit. Inverted clock input has to be provided to clkb terminal. The operation of the circuit is as follows. If the input is high during the positive edge of the clock, the output will be high during that clock period. If the input is low during the positive edge of the clock, the output will be low during that clock period. Inverter schematic is simply designed using PMOS at the pull up side and NMOS at pull down side. The width of the PMOS is set as twice as that of the NMOS to compensate the speed difference.

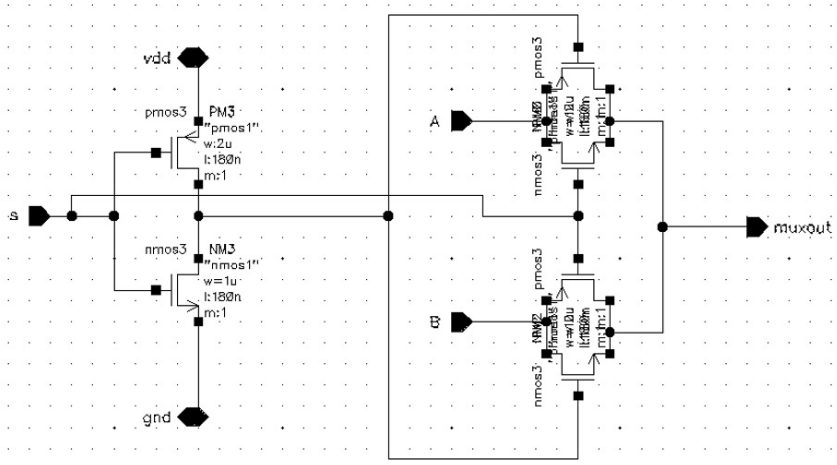

Fig. 1: Optimized selector using transmission gates

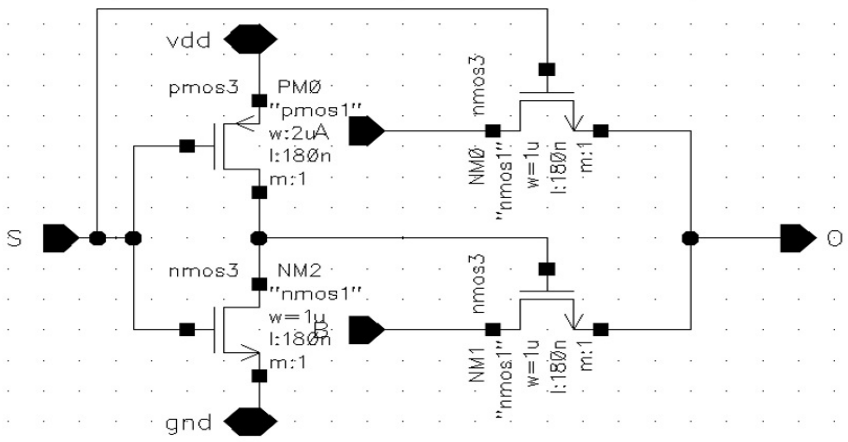

Fig. 2. Optimized selector using pass logic

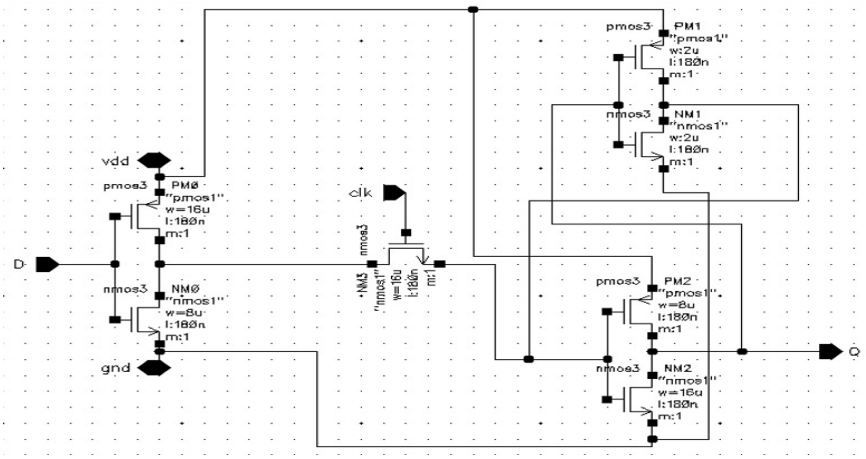

Fig. 3: Schematic of optimized positive level D-latch

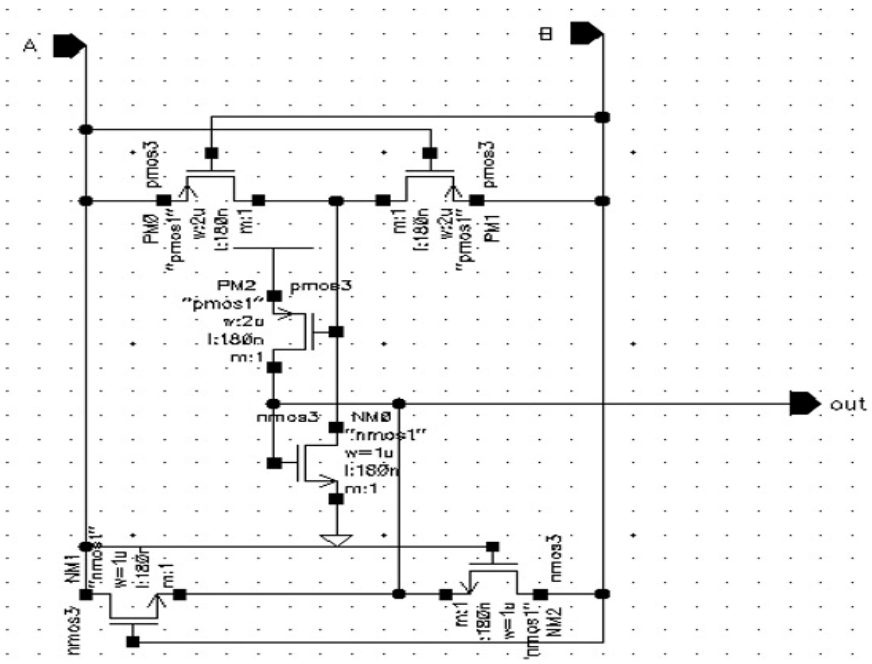

Fig. 4: Schematic of optimized match finder

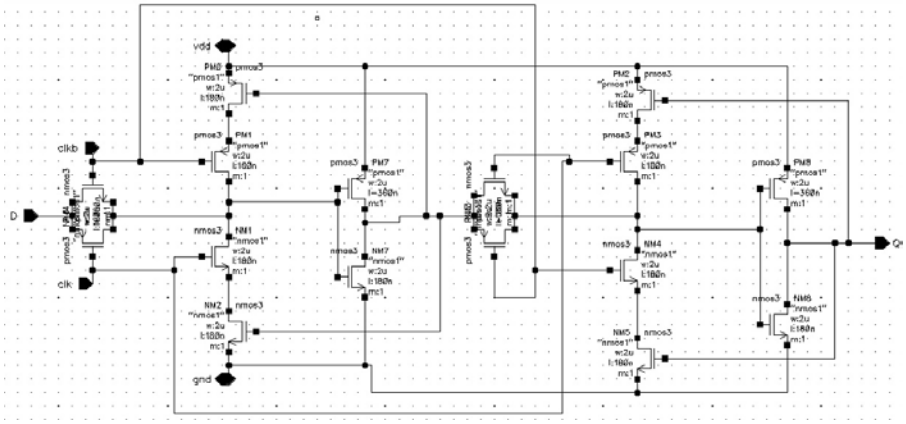

Fig. 5: Schematic of optimized positive edge triggere

Proposed system schematic: Proposed system schematic is designed by combining all of the above mentioned designs as shown in Fig.6. Optimized PTL (Block 5) and TGL (Blocks 2,3 and 6), Match Finder (Block 4), D-Latch (Block 7), Inverter (Blocks 1 an 8) and D-Flip Flop (Block 9) are used in the proposed schematic. The generated code is obtained from the path before it enters into the DFF. The degenerated data can be obtained from the output of the DFF. As discussed earlier, this schematic is capable of doing multiple operations based on the control inputs Ca, Cb, Cc and Cd. The control inputs and their corresponding operation are tabulated in Table 1.

Table 1: Table for scheme selection

Scheme	Ca	Cb	Cc	Cd
BPSC generation	1	0	0	1
BPSC degeneration	0	0	1	0
Phase code generation	0	1	0	1
Phase code degeneration	0	0	1	1

To understand the operation of the BPSC, two systems can be coupled in series. The first system is provided with the control inputs to operate as a code generator and another system is provided with the control inputs to perform the Code degeneration. The input data (in) and the clock (clk) signal are provided as the inputs to

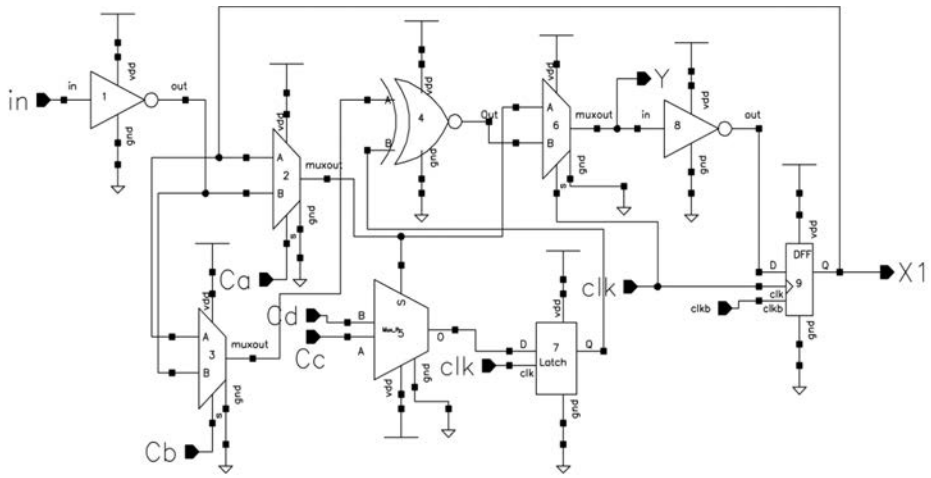

Fig. 6: Proposed schematic system

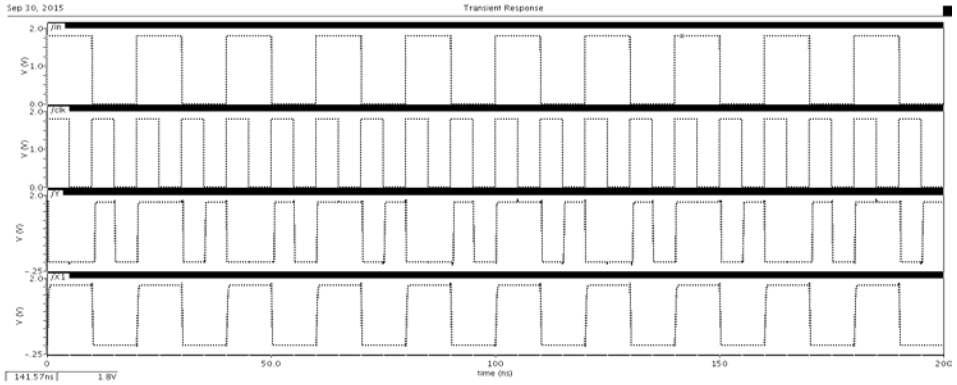

Fig. 7: Response of Bi-Phase space coding scheme

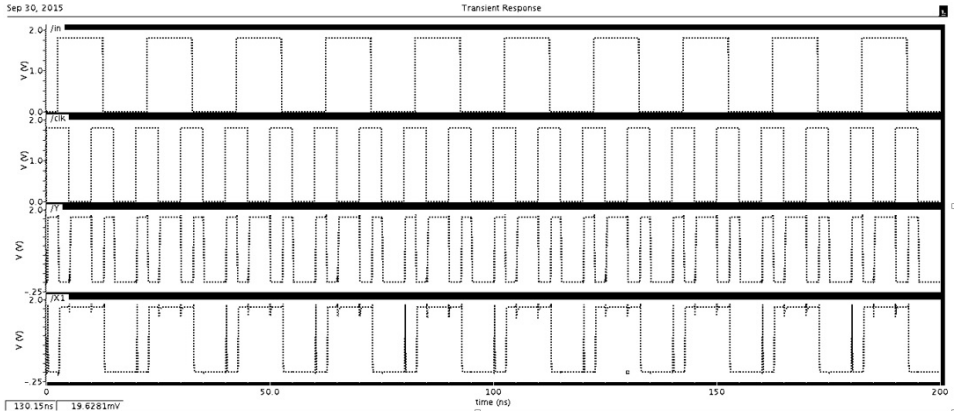

Fig. 8: Response of phase coding scheme

the first system. The generated code (Y) is provided to the second system. The Degenerated data (X1) is obtained from the coupled system. Waveforms obtained for BPSC scheme from Cadence Virtuoso ADE L are shown in Fig. 7. This waveform adopts with the background of BPSC. PC generation and degeneration can be performed by applying different set of control inputs as specified in the Table 1.

RESULTS AND DISCUSSION

Power analysis: To know the efficiency of the circuit based on the power consumption, power analysis is required. Average power consumption, Peak power at a point, Static power consumption, Dynamic power consumption of the both schemes are analyzed. The analysis was done for the duration of 200 ns at three different frequencies i.e., 100, 250 and 500 MHz for both schemes. The power analysis was performed for code generation and degeneration operations separately. Following notations are used in Table 2. AV-Average Power, PP-Peak Power, SP -Static Power, DP-Dynamic Power. The tabulated results in Table 2 and the corresponding power analysis chart shown in Fig. 9 shows that, the Phase Coding scheme consumes less power than that of Bi-Phase Space Coding scheme. Both schemes are utilizing the same hardware. But, based on the control inputs, the switching activity of the transistors differ. The power consumption of our proposed system is less than the existing systems. For example, in the existing system the BPSC run at 500 MHz frequency consuming 890 μW. But, our system consumes 745.2 μW only for that case. Gate capacitance of a MOS device is as in Eq. 1:

$$C_g = \varepsilon \frac{WL}{t_{ox}}$$

Dynamic power consumption is expressed as in Eq. 2:

$$P_d \propto C V_{dd}^2 f$$

Power consumption and capacitance are related with each other as in Eq. 2. The gate capacitance is reduced by reducing the width of the device and the power consumption is reduced by reducing the capacitance. The power consumption is reduced around 15%. The power consumption depends on the frequency also (2). This can be observed in Table 2.

Area analysis: The layout was designed using Cadence Virtuoso Layout Suite XL to analyze about area minimization. This system requires the area of 22.94×65.705 μm^2 as shown in Fig. 10. The previous system requires 33×120 μm^2 with the same 180 nm technology. Required area is reduced by 61.93%. This is achieved by reducing the width of the devices and maintaining the ratio of pull-up and pull down side as 2:1.

Table 2: Table for power analysis

Frequency	100 MHz	250 MHz	500 MHz
Bi-Phase code degeneration			
AP	245.1 μW	454.5 μW	745.2 μW
PP	6.223 mW	6.646 mW	8.332 mW
SP	366.1 pW	366.1 pW	366.1 pW
DP	245.09 μW	454.49 μW	745.19 μW
Bi-Phase code degeneration			
AP	326.0 μW	590.1 μW	977.2 μW
PP	5.944 mW	5.951 mW	7.43 mW
SP	1.6293 μW	1.6293 μW	1.6293 μW
DP	324.37 μW	588.47 μW	975.57 μW
Phase code generation			
AP	233 μW	350.11 μW	640.7 μW
PP	6.356 mW	6.309 mW	10.16 mW
SP	356.89 pW	356.89 pW	356.89 pW
DP	232.99 μW	350.1 μW	640.69 μW
Phase code degeneration			
AP	287.9 μW	476.42 μW	981.42 μW
PP	7.450 mW	10.72 mW	13.95 mW
SP	1.254 nW	1.254 nW	1.254 nW
DP	287.89 μW	476.41 μW	981.41 μW

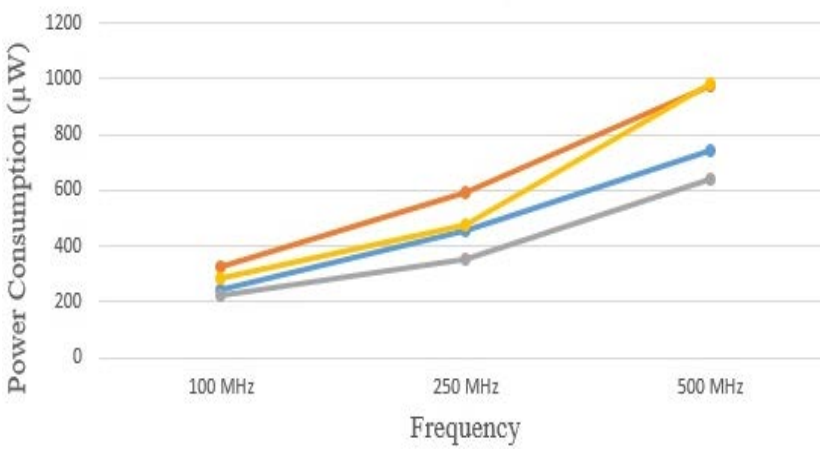

Fig. 9: Power analysis chart

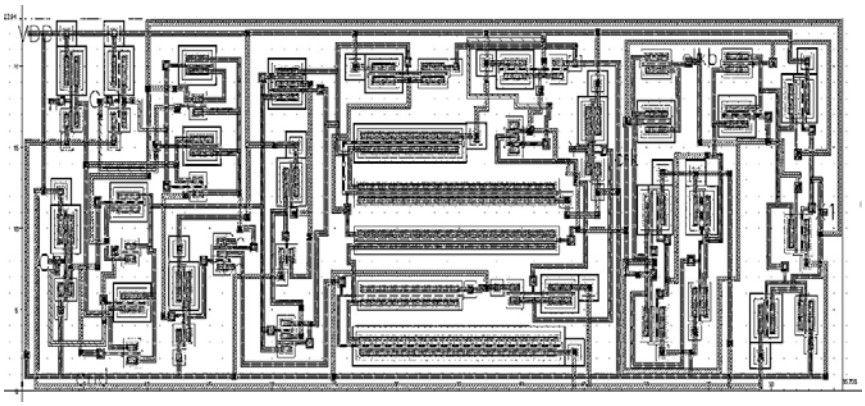

Fig. 10: Layout of the proposed system

CONCLUSION

This study deals with the system design of Phase/Bi-Phase Space Coding scheme for Wireless Sensor Network applications. The system was designed using 55 transistors with full hardware utilization. The design was analyzed in Cadence 180 nm technology. It occupies 22.94=×65.705 μm^2. The simulation was done at 100, 250 and 500MHz frequencies. Frequency of operation can be increased by concentrating on device modelling in the future.

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