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BISR Strategy for Compression Based Bench Mark Testing Sequential Circuit

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Abstract: In this compression based bench mark testing sequential circuit is tested by using Built In Self Repair (BISR) strategy. This strategy describes the testing method for generation on chip broadside tests. The generation of hardware is based on the function of initial input from a specified primary state therefore using the sequential circuit to generate additional states can be reached. Primary random sequences are entered to change the repeated function and this can be validated the pair of comparable states. This strategy comprises of the primary contribution vectors and the corresponding vectors can be verified. This test is useful to achieve a maximum rate of demonstrated faults in bench mark testing sequential circuits and also their bench mark testing circuit S27 era is the fundamental objective for this technique. Often, functional input vectors are verified as verification based vectors, these are used to confirm if the function characters matches its requirement. In the automatic test equipment world any one vectors application are taken to be fault coverage of functional generation of vectors given during the developing repair strategy, then the fault coverage area easily detected. This study shows S27 circuit is used in multiplier circuit for testing application and it is done by verilog programming and simulated by modelsim 6.5version and synthesis by xilinx tool.

Key words: Built in Self Repair (BISR), Built in Self Testing (BIST), Linear Feedback Shift Register (LFSR), Benchmark testing, sequential circuit S27

INTRODUCTION

Built in self Repair strategy was proposed by compression based bench mark testing sequential circuit S27.It can be describes the on chip function generation method for functional on chip test. Functional vectors are taken as clarification vectors. As bench mark testing compression based circuits methodology those breaking points of Moore's law and the area specification has taken a edge on increments in clock recurrence, stacking dies to structure a 3-D die-stack have been recommended as one of the method that will give satisfaction on improvement in the execution about the system. Increase the system performance are expected to rise the high gain from the input sequence that the vectors routes the middle of dies on a stack are much less than the chip towards chip continue to table or routes starting with one end of a chip to in turn. Unfortunately, high gain volume manufacturing has been difficult (Whetsel, 2000). One of the most cause prevention the large-scale manufacturing of 3-D integrated circuits there are Testing dies and getting great earnings are difficult. The inclusion of Through-Silicon Vias (TSVs) can destroy the concept is during the compression based bench mark testing strategy then the silicon is grounded to explicit the TSV connection something like that can be compared to the multi core comparator. Through silicon via are efficient to probe without damaging the making of testing the individual dies are difficult in manufacture. Fortunately, a 3-D stack additionally gives new chances for replacement strategy. Specifically, whether a die have benchmark testing sequential circuit is include to the 3D die stack, this multi core functions comparator destroy to sidestep faulty segments about another dies. Many case of granularity for testing are possible from replacing the validate quality can be reschedule by a compression based testing architecture of functional unit to compression based testing architecture. particularly repair strategy was well defined to the repair of clarification units in out of order processors because the multi core processors can be explained to split data can be evaluate multiple RAM functional units with different architecture (Sankaralingam *et al*., 2000). In case, testing is achieved when the critical comparator of a discriminating part will be found to be faulty. However, when the defective component are lacking even the performance cause automatic test pattern generation, substitution cost of the faulty majority data might be alluring. This study enhances the idea for BISR digital logic compression based testing architecture in 3-D stacks. They are declare two separate comparator dies in the 3-D stack the original compression based circuit used in an Application Specific Integrated Circuit process and a separate FPGA die which can be computed can be

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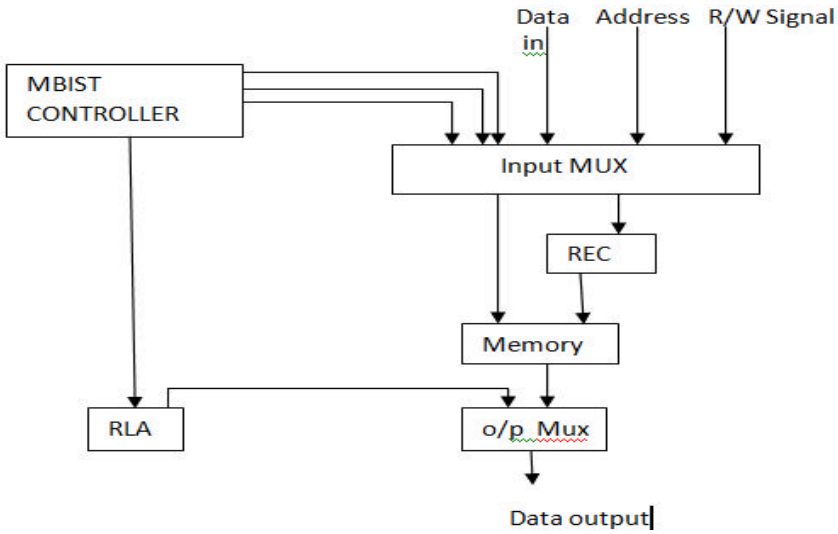

Fig. 1: Block diagram of compression based testing architecture

needed to design extra practical modules (Fig. 1). This approach destroy the merits given by 3-D architectures including number of large Through-Silicon Vias strategy and capability are created between dies to increase the flexibility and increase the performance of repair. To the best of our knowledge, this proposed work such a bench mark testing compression based method achieved. Similarly, multipliers, adders, subtractors are compared to the comparator. The output of the compression based testing sequence being reconstructed and the part of the circuit to detect to the compression based circuitry will be rest of the driven comparator by the MBIST (Memory BIST) instead of the defective partition shown in Fig. 1, each of the inputs has the fault detection to the adder multiplier architectures are compared the comparator architecture.

The tristated driving buffers are analyzed to minimize the area and delay can be taken to the multicore circuit. Most of the TSVs are linked to the FPGA such that it turns into a primary input given to the FPGA. ASIC and FPGA both will taken to be automatic test pattern generation programmed the majority data. The result of the simulation given the sign conversion of test data will then travel through other predefined TSVs until they arrive at the level of the ASIC being repaired (Lee *et al*., 2000). Comparators are evaluated to give the input values to the comparator architecture of the circuit is in repair mode as shown by the quality of the select line on the MUX.

MATERIALS AND METHODS

Built In self repair strategy was used to related module in matching the compression testing method like logic blocks or routing resources to displace those faulty comparator modules. One more way is to utilize the automatic test generation functional units on FPGA such as alternative ALUs. These methodologies execute both the original and alternative modules on a single comparator testing architecture. The same alternative die in a Silicon on Chip (SoC) to give capacity for validating the design of S27. Then the design comparator architecture are specifications (such as compression test data) change in Fig. 2.

On chip test generation method: On-chip ROM memory architecture and analyze the performance, area compression and temperature tradeoffs of 3D CMPs. Runtime of compression matching factor to improve performance while maintaining power and area constraints. 3D stacking ROM memory architecture for CMPs behavior and selects among low-power and turbo operating modes accordingly. Under the fixed voltage-frequency (V-F), the IPC of runtime optimization policy increase a multi core 3D CMP with stacked DRAM compared with measurable optimal 3D system to Energy-Delay Product (EDP) is decrease the multi core comparator to a 3D system managed by a temperature triggered dynamic scaling split data policy. Complex matching factors of performance, area compression and power of 3D die stack bench mark circuit S27 with stacked SRAM main memories (Ikar *et al*., 1998).

The BISR concept for bench mark testing sequential circuit was specify an acceptable and reliable strategy for each matching factors, core or application. Technology scaling has high gain volume to determine the effect on multicore split data accuracy with improved changeability

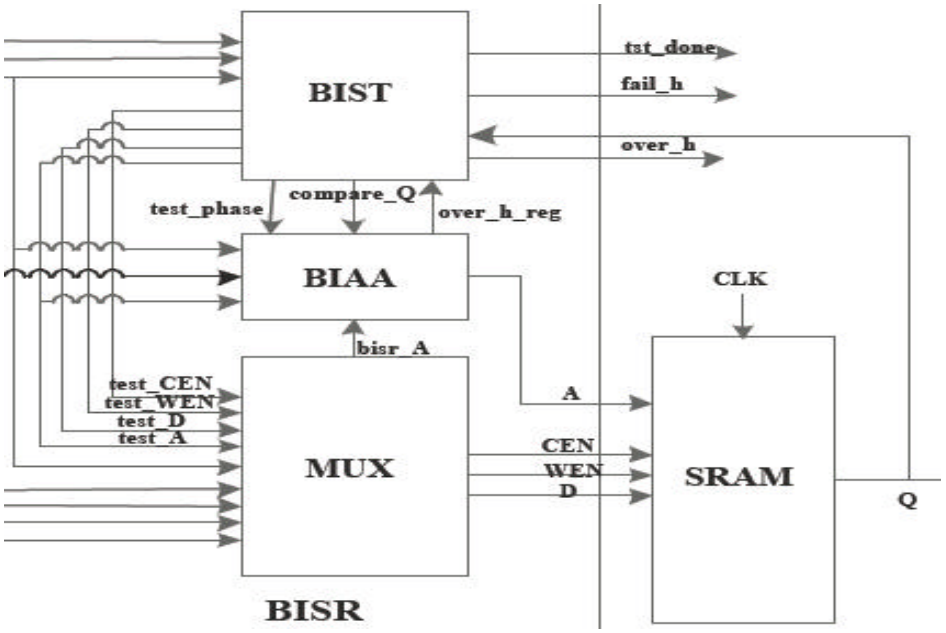

Fig. 2: BISR architecture

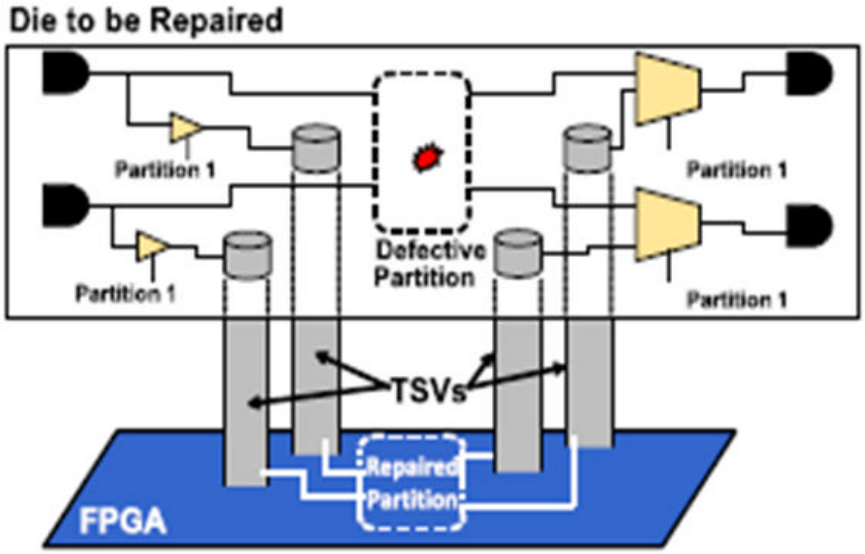

Fig. 3: Application Specific Integrated Circuit (ASIC) partition repair using the Field Programmable Gate Array (FPGA) layer

and higher perceptivity to mistakes. Architecture and redundancy method to develop the yield of 3-D-stacked memories. The new fuse architecture have the Built In Address Analysis (BIAA) and SRAM memory management cause the repair working area which is shown in Fig. 2. There is a way to declare the compression based matching a fuse architecture provides prebond and postbond repairs. Stacking multiple memory dies vertically using TSVs can reduce the interconnect length shown in Fig. 3. This not only reduces the latency but also provides high bandwidth and low power consumption. In 3-D-stacked memory, capacity extension is implemented by increasing the number of stacked memories. However as the number of stacked memories increases, the yield loss of 3-D-stacked memories becomes more serious due to one of irreparable stacked memories.

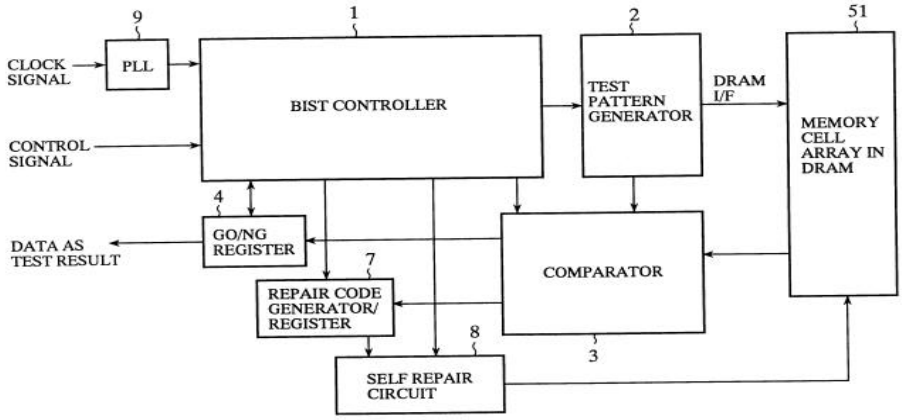

Fig. 4: Self repair circuit

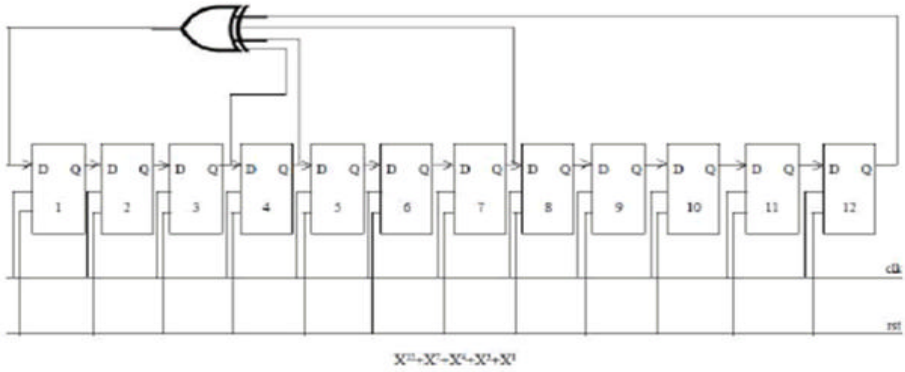

Fig. 5: Linear Feedback Shift Register (LFSR) 12 Bit circuit

Fault correction technique: Error correction code and built-in self-repair schemes are used to improve the compression of matching factors memories. Many built-in redundancy-analysis algorithms and ECC schemes are used to report before. However, most of them taken this BISR strategy for ECC schemes. In this study, we propose compression based matching factors in the field of bench mark testing sequential circuit S27 for yield improvement. Many comparators are partition to addition or subtract or comparator architecture.

Linear Feedback shift register values initially at given to primary input of the built in self repair circuit. We note the unnamed in the two unscanned state variable this involves which can be utilized as a scan in state of this test and the first two patterns of the test can be neglected, suppose that is stated to functions and broadside vectors. It is due to the result in which all the states are fully specified.

Built in self repair strategy: Self repair of a comparator on the ASIC using test pattern generation that may be replaceable and by passable by FPGA functionality has the valid verification vectors are Through Silicon Vias that are directly connected to the FPGA (Lee *et al*., 2000). Note that such TSVs are needed to be used for repair. When the condition for correctable partition corresponding to a functional unit in an out of order processor, the alternative TSVs can be compared to the matching factors of comparator also be used for performance of BIST controller acceleration. Specifically, the repair code generation can be used to permit the execution of memory cell array in DRAM instructions on the self repair of memory cell array. Effectively this would allow a hardware implementation of function that taken multi core instructions if it were implemented with the original instruction set shown in Fig. 4.

Proposed work: Linear Feedback Shift Register (LFSR) can be treated as a 12 bit circuit. LFSR is one of the best testing circuit. The goal of this brief is to derive skewed-load test cubes from functional broadside tests and use them for the generation of low-power skewed-load tests.when generating a low-power skew loaded test set. The procedure can also be extended to generate a mixed low-power test set which consist of both broadside and skewed-load tests shown in Fig. 5.

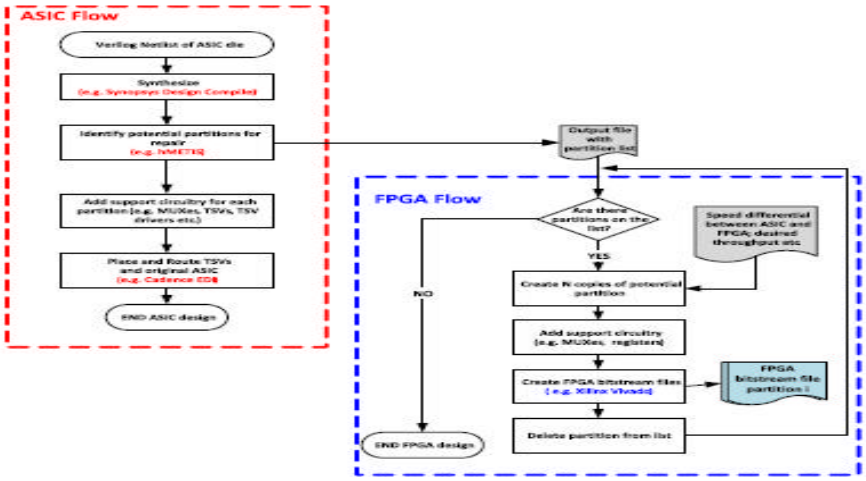

Fig. 6: Repair flow diagram for CAD Design

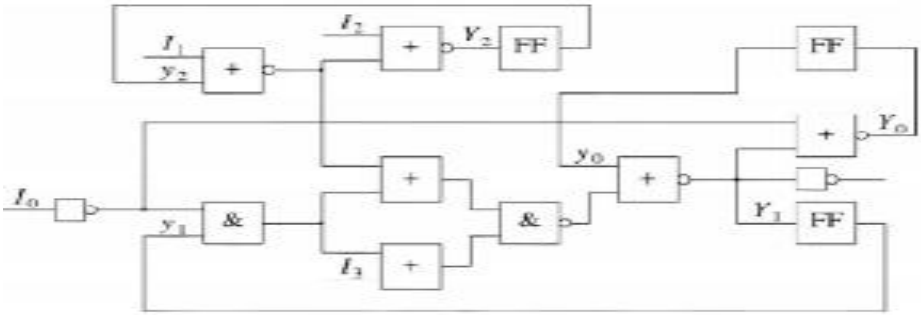

Fig. 7: Benchmark testing circuit of S27

In CAD Design flow we select to induce our programmable repair approach using both a bench mark circuit S27 and a super scalar processor as examples (Kajihara *et al*., 2002). However, the compression based matching factor approach is generally applicable to other types of circuits at various comparator levels of granularity. The design flow of our strategy is shown in Fig. 6 and includes the following steps. Provide a Verilog coding for synthesis software. For this study, we used XILINX.

The repair of the defective partition can take place toward user defined level about granularity. For the multiplier architecture, a partition resolve match to the combinational logic in a pipeline stage. Once the circuit partitions include identified, the ASIC flow continues with the placement of the synthesized cells and the inclusion and placing of the TSVs, drivers and MUX required to shift data between the ASIC level and the FPGA during repair.

The FPGA flow consists of the following steps. A repairable partition is selected from the list and a new circuit net list with multiple copies of the partition is created. In the simplest implementation, the number of copies that are needed is determined by the speed differential between the FPGA and ASIC clock signals of the design however, other utilization such as the aspects of the element for a typical application can also affect the ideal number of copies.

Additional support registers, multiplexers, etc., are added to the FPGA design to allow data from the ASIC layer to multiplex to the suitable copy and to return data to the ASIC layer when execution completes. The FPGA design is replicated and then the bench mark testing sequential circuit S27 was implemented that can be loaded when repair of the desired partition is necessary. Steps 1-3 are repeated until a bit stream for repair of each of the partitions that are recognized as potential components for repair is generated.

Figure 7, shows the S27 bench mark testing sequential circuit is the ordinary circuit. Here, we used S27 bench mark as a testing circuit. Apply the test vectors as input to the S27 bench mark sequential circuit generation for efficient and simulated practical scan based tests were generate the external tester under the test generation of

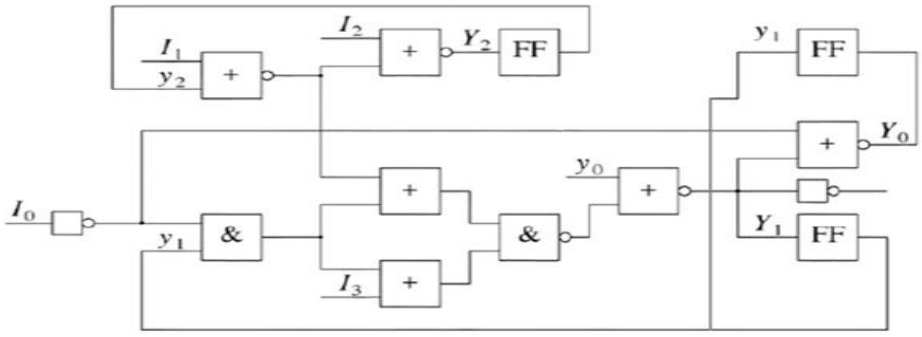

Fig. 8: S27 faulty circuit

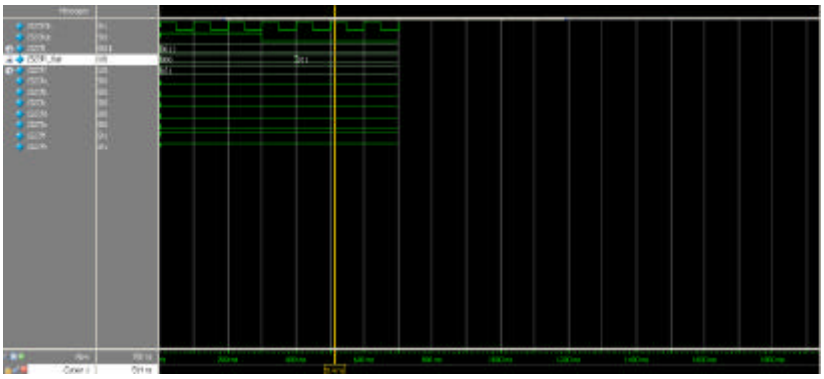

Fig. 9: Output waveform of standard sequential testing circuit S27

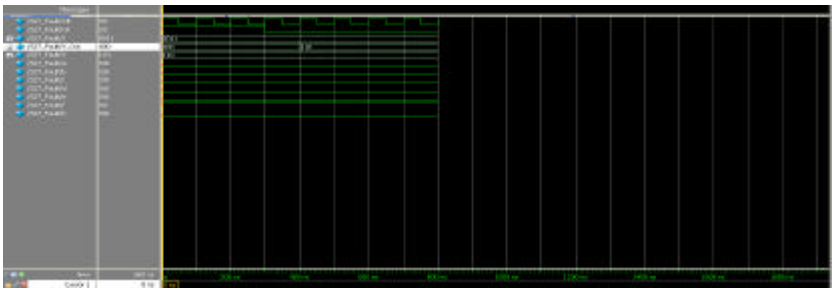

Fig. 10: Output waveform of faulty sequential testing circuit S27

on chip vectors noted that the holdup error reporting achievable using efficient broadside tests. Bench mark sequential circuit is compare to faulty S27 circuit depends on the specification functional vectors that can be used to detect the faults on the circuit easily shown in Fig 8. Then the presence of delay including defects is causing increasing concern in the semi conductor industry today.

RESULTS AND DISCUSSION

In this Ckt Logic, ScanIn, Clk, Rst, Scan are the given inputs and the outputs are ScanOut. Here normal peration means give an input scan = 0, scan operation means give a input scan = 1. MUX D Flip Flop. Scan Repair, Test Repair, Clk, Rst are given inputs and the outputs are scan out here the normal operation means scan = 1, test mode = 1, repair operation means scan = 0, test mode = 1,these conditions and simulation output shown in Fig. 9.

Pseudo random test generation has the primary goals to develop a battery of statistical tests to detect non random in binary sequence. Compare all the specifications then detect the fault coverage area easily detected by this BISR scheme, due to the comparision of faulty and original S27 testing sequential circuit shown in Fig 9-13. We find the fault on defected area. The above Register

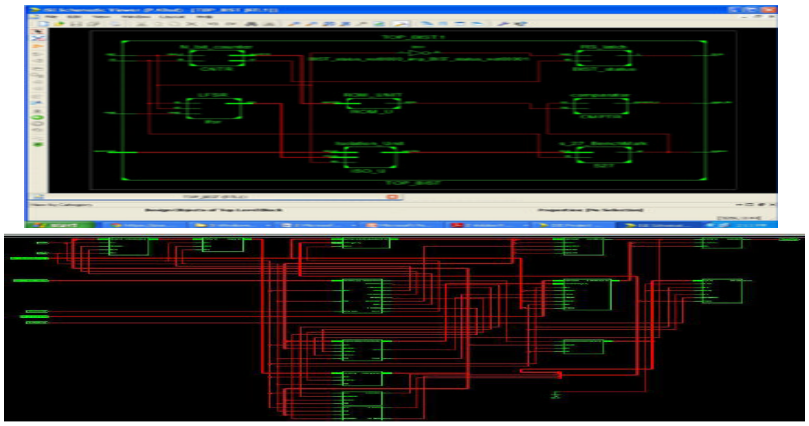

Fig. 11: RTL view

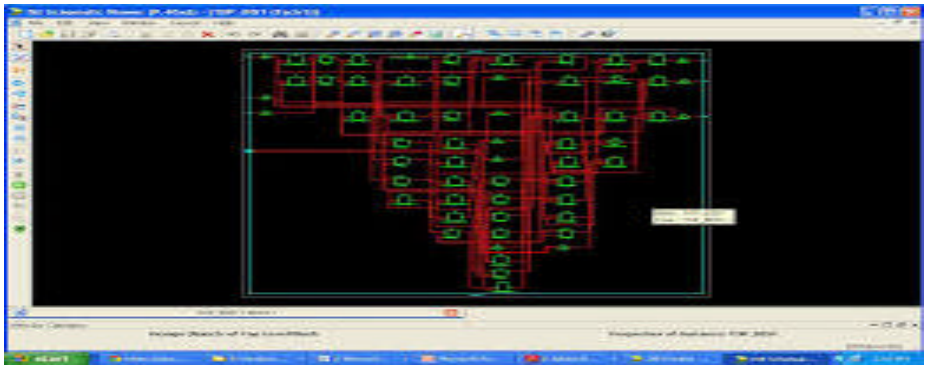

Fig. 12: RTL schematic view

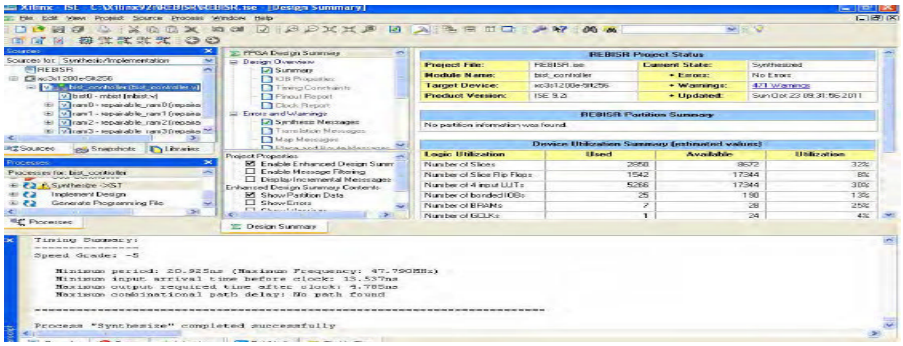

Fig. 13: Synthesis report for device utilization summary

Transfer Logic (RTL) is nothing but graphical representation of the built in self repair using bench mark circuit of sequential circuit S27 design was verified and faulty area can be detected easily. RTL graphical representation of circuit design generated by the synthesis tool. The goal of the RTL Schematic view is to be nearly close of the functions represented the internal blocks and specifications of possible to detect the area of fault coverage. The number of Look Up Table (LUT), flipflops, Gated CLK (GCLK), delays are noted in the above mentioned device utilization report (Fig. 13).

CONCLUSION

In this method we make use of BISR Scheme for Bench mark testing sequential circuit S27 to access the deep submicron technology allow the multiple memories on a single chip. On chip test generation has the built in

self repair a bench mark sequential testing circuits S27 has the merits like reduces the test data volume,and testing complexity can be reduced, facilitates at speed test application, then it achieves high fault coverage. Future work related to reduce the time overhead.

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