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Design of CMOS RF Front-End of Low Noise Amplifier for LTE System Applications

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Abstract: This study describes a CMOS RF front end for long term evolution system applications in a TSMC 0.18im process, this work use Receiver Architecture including Source Inductive Degeneration LNA in according with LTE system standard for the center frequency of 2.4GHz. The challenges of circuit design are based on low power, low noise figure and high gain. The most important parameters of receiver front-end circuit are Gain, noise figure and linearity. The circuit exhibits a good trade off among low noise, high gain and provides more reverse isolation which is crucial in LNA design.Complete simulation analysis of the circuit results in center frequency of 2.4 GHz with 38.5 dB Voltage Gain, 2.2dB Noise Figure (NF), IIP_3 of -6.063dBm, 1-dB Compression Point of -17.13dBm, 50 Ω input impedance, 3dB Power Bandwidth of 450MHz, 11.2dB Power Gain (S_{21}), High Reverse Isolation (S_{12}) = 60 dB, Input Return Loss (S_{11}) =11dB, Power Dissipation of 2.7mW at 1.2V power supply.

Key words: CMOS RF, front-end receiver architecture, low noise amplifier, long term, evolution specification

INTRODUCTION

Radio Frequency (RF) devices transmit and receive signals from 3 kHz-300 GHz, covering a variety of wireless standard applications. For example, new generations of cellular phones 4G (LTE) have just been available for a couple of years. Moreover, wireless local area network (Wi-Fi) is gaining popularity for laptop, tablet and Smartphone, since Wi-Fi can provide access to the Internet via an access point (hotspot). Campus-wide Wi-Fi and city-wide Wi-Fi are further providing convenience for these users. Since wireless communication enables voice, data, image and video to be transferred to anywhere almost instantaneously, the impact of RF on people's daily lives has become significant. The receiver's front-end circuits play very important role in faithfully recovering the information transmitted through the wireless channel. The Low Noise Amplifier (LNA) is used in communication systems to amplify very weak signals captured by an antenna. It is located very nearer to the antenna, as shown in Fig. 1, so that losses in the feed line become less critical.

According to Friis's noise figure relationship, the first few stages dominate the overall noise figure of the receiver front-end. LNA reduces the noise of all the subsequent stages by the gain of the LNA while injecting the noise of the LNA directly into the received signal Thus, LNA should boost the desired signal power while adding as little noise and distortion as possible so that the retrieval of this signal is possible in subsequent stages in the system.

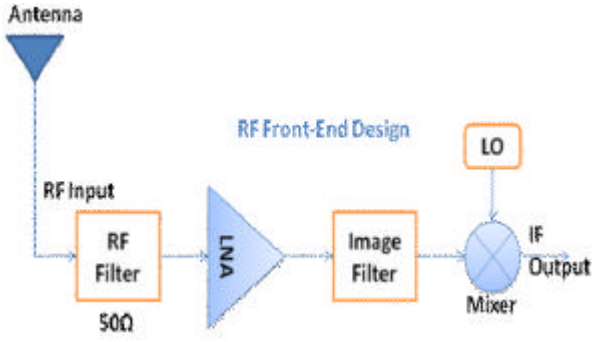

Fig. 1: Radio frequency front-end receiver block diagram

The LNA must have high amplification in its first stage to achieve low noise. A low LNA noise figure (typically NF < 3 dB) means a minimum degradation of the Signal to Noise Ratio (SNR) of the wanted signal resulting in high sensitivity. The gain of the LNA relaxes the Noise Figure requirements for the subsequent stages (Mixers, IF Stage). The design of LNA is very crucial because of its position in the receiver path; so anything wrong in the LNA circuits cannot be compensated in subsequent stages. The realization of LNA circuits in CMOS technology is very challenging.

Communication IC is target to a small size and low power circuit in the future. Along with increasing of mixed circuits, reliability requirements of CMOS become more important (Leung, 2011). Front-end circuit of RF is the most popular research topics in recent years. In sum, the

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Table 1: LTE receiver specifications

Receiver items	Specification
Input power (dBm)	-95 to -25dBm
Noise figure (dB)	<7
P_{1dB}	>-25
$IIP_{3\,(dBm)}$	<-15

target of CMOS communication circuit's integration is to build a RF front-end and base-band processing receivers.

Recent works in designing of LNA shows that it's very difficult to achieve low noise figure and low power consumption. This study gives comparative analysis of different LNA designed in past few years so that we can try to improve the different parameters of LNA.

LTE specifications: LTE, an abbreviation for long term evolution, commonly marketed as 4G LTE, is a standard for wireless communication of high-speed data for mobile phones and data terminals. It is based on the GSM/EDGE and UMTS/HSPA network technologies, increasing the capacity and speed using a different radio interface together with core network improvements (Lin *et al*., 2014). The standard is developed by the 3GPP (3rd Generation Partnership Project) and is specified in its Release 8 document series, with minor enhancements described in Release 9 and 10. The utilized band is mainly allocated based on Evolved Universal Terrestrial Radio Access (E-UTRA) which is part of 3GPP LTE air interface. E-TURA is a whole new system belonging to 3GPP 8 editions not incompatible with wideband Code Division Multiple Access (W-CDMA). For data transfer, download uses Orthogonal Frequency Division Multiple Access (OFDMA) and upload uses Single-carrier Frequency-Division Multiple Access (SC-FDMA). Operating bands of proposed architecture is from 2400-2490 MHz within Band7 of E-UTRA. Flexible bandwidths are 5MHz, 10MHz, 15MHz and 20MHz.Transferring speed based on 20MHz frequency can reach to 100Mbps for downlink and 50Mbps for uplink. Chip is designed in 0.18μm CMOS process.

LTE is the natural upgrade path for carriers with both GSM/UMTS networks and CDMA2000 networks. The different LTE Frequencies and bands used in different countries will mean that only multi-band phones will be able to use LTE in all countries where it is supported. Table 1 describes the receiver specification of LTE including the input power, the noise figure, input third-intercept point and input 1dB compression point. The requirements can be calculated from the 3GPP TS 36.101 V8.9.0 [10] standard's specification.

LNA topologies: There are lots of methods to adjust the input impedance of the amplifiers (Toofan *et al*., 2007). Four distinct methods are:

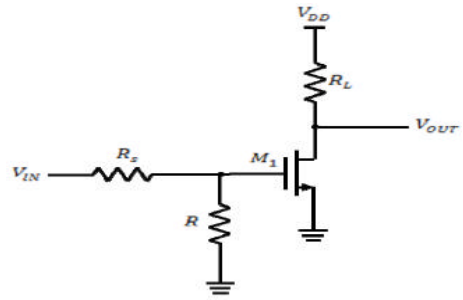

Fig. 2: Resistive termination

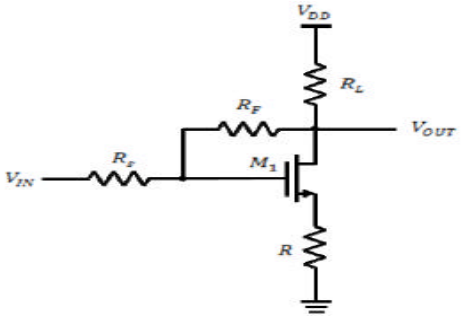

Fig. 3: Shunt-series feedback

- Resistive termination
- Shunt-series feedback
- Common gate amplifier or ($1/g_m$) termination
- Inductive degeneration

Resistive termination: In Resistive Termination Topology, a 50Ω Resistor (R) is simply placed across the input terminals of a common-source amplifier (Fig. 2) with a source resistance (R_S) and an output resistance (R_L).

However, this additional resistor introduces thermal noise that increases the amplifier's NF and attenuates the signal before the transistor, resulting in unacceptably high noise. This method utilizes a resistor at the input terminal of the LNA to provide a 50Ω input resistance.

Shunt-series feedback: In a shunt-series feedback topology (Fig. 3), before amplification the resistor R does not cause attenuation of signals. It is expected that the noise figure in shunt-series feedback amplifier is improve than that of a resistive termination amplifier. On the other hand, the resistor feedback network remains a source of thermal noise. However this method generally has high power dissipation compared to others with similar noise performance and requires accurate on-chip resistors that actually are not available in existing CMOS Technologies.

Common gate amplifier or ($1/g_m$) termination: The common gate topology is another circuit implementing resistive input impedance (Fig. 4). Characteristics of

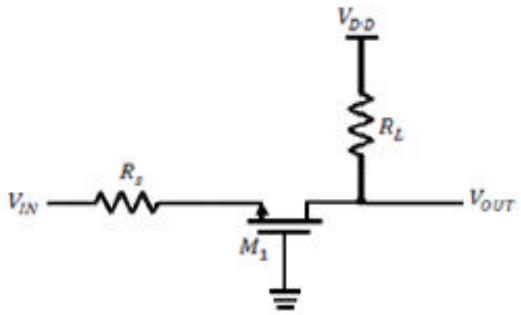

Fig. 4: The $1/g_m$ termination

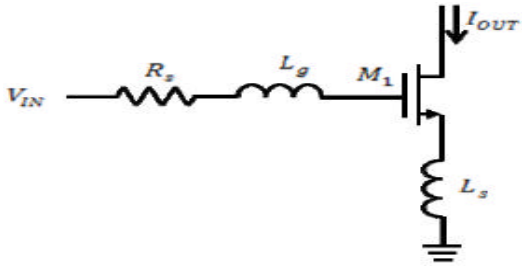

Fig. 5: Inductive degeneration

the common-gate topology are that the resistance looking into the source terminal equals ($1/g_m$). The major drawback of CG topology is high input-referred noise.

Inductive degeneration: An inductive source degeneration topology (Chang and Lin, 2007) (Fig. 5) is commonly used to create resistive input impedance without the noise of real resistors. This topology provides resistive input impedance at the resonant frequency without the thermal noise of an ordinary resistor and degrading the noise performance of the amplifier. So we have used this in our design.

This study focuses on LNA (Low Noise Amplifier) of RF Front-End. To meet the design requirement, it needs to make a balance between noise figure and linearity. This proposed architecture includes source inductive degeneration LNA. And also it must meet the requirements of common design features for the receiver front-end like Noise Figure (NF), input-referred third-order intercept point (IIP_3) and input power 1-dB compression point (CP_{1dB}) and Conversion Gain. Low power consumption as well as good noise performance is a great challenge to design.

MATERIALS AND METHODS

Design conciderations: The low gain LNA cannot amplify the incoming weak signal to a desired value and high gain LNA can degrade the linearity. Linearity is typically measured in terms of Input Intercept Point (IIP3) that is required to be maximized (Behzad Razavi). To achieve higher linearity in RF receivers, IIP3 must be >10dBm. There is trade-off among Gain, Noise Figure, Linearity and Power Consumption etc. in the design process of these circuits. The main function of LNA is to provide sufficient transconductance (g_m) gain with acceptable linearity and power consumption to overcome the noise of subsequent stages with addition of little inherent noise. Moreover, the stability conditions, if and only if k>1 and $|\Delta|<1$, presented by stability factor k must be satisfied where:

$$k = \left(1 - |S_{11}|^2 - |S_{22}|^2 |\Delta|^2\right) / \left(|S_{12} \times S_{21}|\right) \quad (1)$$

$$\Delta = \left(S_{11} \times S_{22} - S_{12} \times S_{21}\right) \quad (2)$$

For CMOS LNAs, the power gain (S_{21}) should be in the range of 10–20 dB. The input return loss (S_{11}) and output return loss (S_{22}) of less than -10 dB are desirable. Also to avoid unwanted signals to reach the LNA input from the following stages, reverse isolation (S_{12}) must be <-20 dB (Razavi, 1998, 1999).

The input to LNA is coming either directly from the antenna or from the output of the band pass filter (the Duplexer). Since the antenna has a characteristic impedance of 50Ω, the BPF needs to have both its input and output impedance of 50Ω for unidirectional power flow and maximum power transfer from the antenna to the BPF and from BPF to the LNA. So the main requirement of the LNA is to provide thepower matching so that maximum amount of power will be transferred from the source and to allow the flow of power unidirectional i.e., with no reflections which is called as Impedance Matching (Desouki *et al*., 2015). The matching achieved at the input of the LNA to achieve the minimum NF is called as Noise Matching. In practical cases, the input signal to the LNA usually comes from antennas connected to LNA circuit by an unknown length of transmission line. This requires an amplifier with a reasonably stable input impedance of approximately 50Ω.

The major advantage of the proposed Source Inductive Degeneration method is that it does not degrade the amplifier's noise performance and it easily matches the input impedance. Neglecting parasitic effects, its input impedance can be expressed by Toofan *et al*. (2007):

$$\begin{aligned} Z_m &= R_g \left| R_{Ls} \right| \left| R_{Lg} \right| s\left(L_s \left| L_g \right.\right) \left| \frac{1}{sC_{gst}} \right| \frac{gm}{C_{gst}} L_s \\ &\approx s\left(L_s + L_g\right) + \frac{1}{sC_{gst}} + \frac{gm}{C_{gst}} L_s \end{aligned} \quad (3)$$

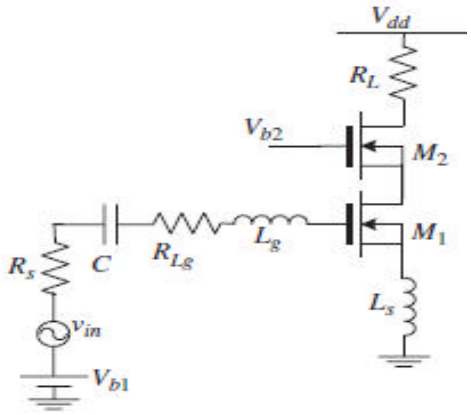

Fig. 6: Common LNA circuit schematic

Where:

C_{gst} = The total gate–source capacitance,
g_m = The tranconductance and
R_g = Gate resistance of the transistor
R_{Lg} and R_{Ls} = Series resistances of the inductors L_g and Ls

At the desired frequency, the imaginary part of (Eq.3) must be equal to zero and then the input impedance becomes:

$$\text{Image}(Z_n) = 0 \Rightarrow Z_m = \frac{g_m}{C_{gst}} L_2 \tag{4}$$

Receiver rf front end design: To have proper impedance matching and increased isolation, a good configuration for LNA is the cascade topology with inductive degeneration (Toofan *et al*., 2007) as depicted in Fig. 6.

The first design step is calculation of the optimum width of the input transistor M_1 to obtain the best noise performance. The channel width of the input transistor M_1 is calculated by the following equation:

$$W_1 = W_{optIFmin} \cong \frac{1}{3wLcoxR_S} \tag{5}$$

where, C_{ox}, R_s, ω and L are the oxide capacitance, source resistance, operating frequency and length of the transistor, respectively. The dimensions of the cascading transistor M_2 should be similar to that of M_1. This requires a trade-off in order to suppress the noise magnitude of M_2 and the Miller effect of M1 (Chen *et al*., 2014). In Fig. 7 the reference current I_{ref} is determined based on the power consumption of the circuit. Total gate-source capacitance (C_{gst}) of transistor M_1 can be found using:

$$C_{gst} \cong \frac{2}{3} W_1 L C_{ox} \tag{6}$$

Transistor M_3 is used as LNA biasing network which forms a current mirror along with M_1. To minimize the noise and power consumption the width of transistor M_3 must be set to a small fraction of M1's. A good assumption is $W_1 = 20W_3$:

$$\omega_0 = \sqrt{\frac{1}{(L_s + L_g)Cgst}}$$
$$\frac{gm}{C_{gst}} L_s - 50 \tag{7}$$

From Eq. 7 we found that the source inductor is used for impedance matching and the gate inductor sets the input resonance frequency. A suitable resistance (R_b) is used to lessen the effect of gate–source capacitance in transistor M_3 and, its value is arbitrarily chosen to be 2-4 kΩ in 0.18μm technology. Generally, C_1 is assumed to be 5-10 times $>C_{gst}$. At the output, an inductor is placed at the drain primarily for two reasons. Firstly to achieve desired frequency the drain inductor should resonate with the total drain capacitance. Secondly, it should provide a high enough impedance to obtain a good gain. The LNA voltage gain is approximately calculated by:

$$A_v \cong Q_{in} g_{m_1} Z_L, Q_{in} = \frac{1}{2\omega_0 R_s C_{gst}}$$
$$= \frac{\omega_0 (L_g + L_s)}{2R_s} \tag{8}$$

where, g_{m1} is the transconductance of M_1, Z_L is the load impedance and Q_{in} is the input matching network quality factor.

RESULTS AND DISCUSSION

In this design work, we had used Tanner EDA and Cadence Tools to build the schematic for the circuit shown in Fig. 7 and then simulated the circuit within analog design environment using T-Spice Simulator and Spectre RF Simulator.

The detailed schematic diagram is drawn in Schematic-Editor (S-Edit) and corresponding simulation waveforms for different parameters are generated by Tanner Spice simulator shown below. Circuits are realized and simulated using TSMC 0.18μm CMOS technology for 2.4GHz frequency range.

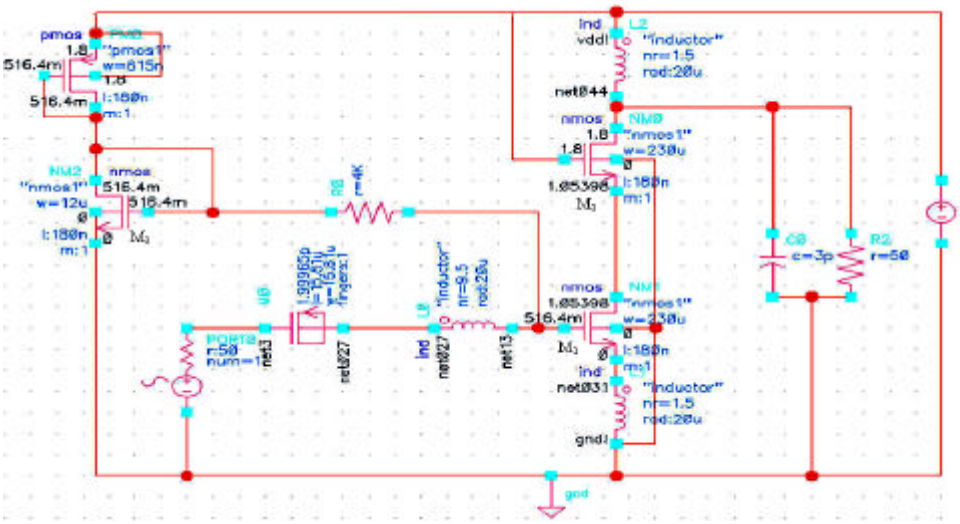

Fig. 7: The schematic diagram of integrated LNA

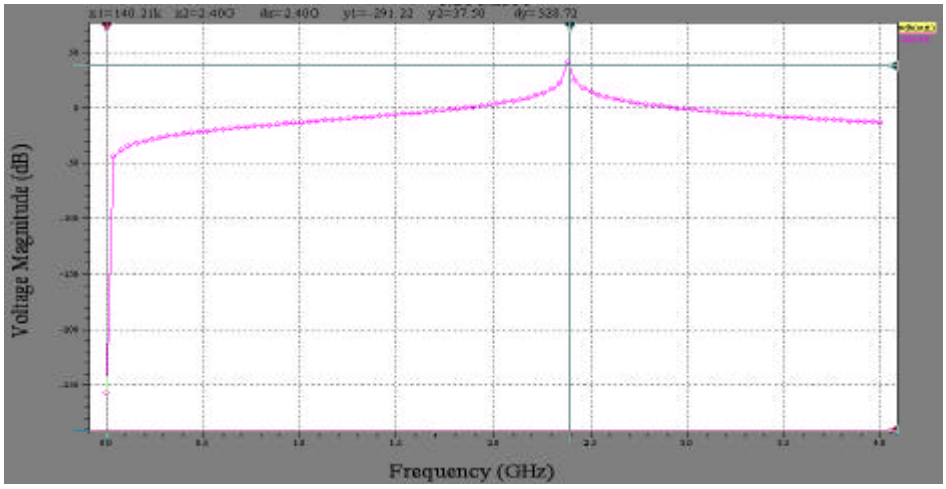

Fig. 8: Voltage Gain is 38.50 @ 2.4GHz

Voltage Gain is a measure of the ability of a circuit to increase the power or amplitude of a signal the output waveform of Low Noise Amplifier at operating voltage of 1.2V for 0.18μm technology. The obtained voltage gain obtained is 38.50dB at 2.4GHz frequency as shown in Fig. 8. Noise Figure is a measure of degradation of the Signal to Noise Ratio (SNR):

$$NF = \frac{(S/N)in}{(S/N)out}$$

The noise figure obtained at 2.4GHz frequency is 2.2dB as shown in Fig. 9.

The corruptions of signals due to 3rd order inter modulation of two nearby interferer is so common and so critical that a performance metrics has been defined to characterize their behavior called the 3rd order Input intercept point (IIP3). The Noise Figure obtained is -6.06347dBm at 2.4GHz frequency as shown in Fig. 10.

The 1-dB compression point is the input signal level that causes the small signal gain to drop by 1dB. The 1-dB compression point obtained is -17.131dBm at 2.4GHz frequency as shown in Fig. 11.

S-parameters results: S-Parameters obtained at 2.4GHz frequency as shown in Fig. 12 and 13.

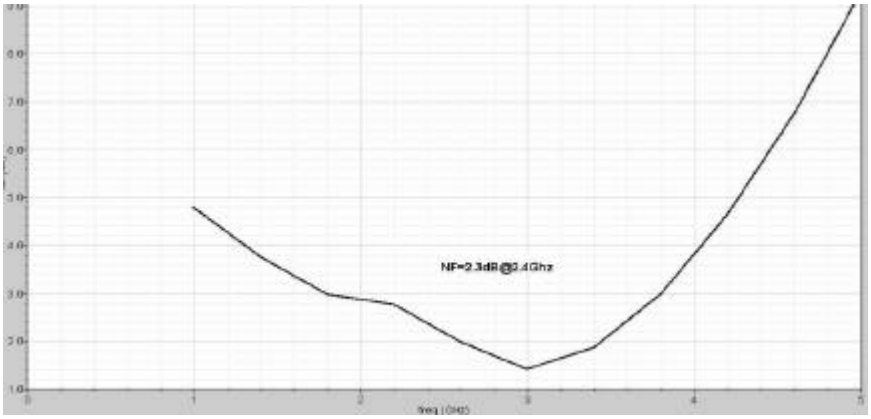

Fig. 9: Noise Figure is 2.2dB @ 2.4GHz

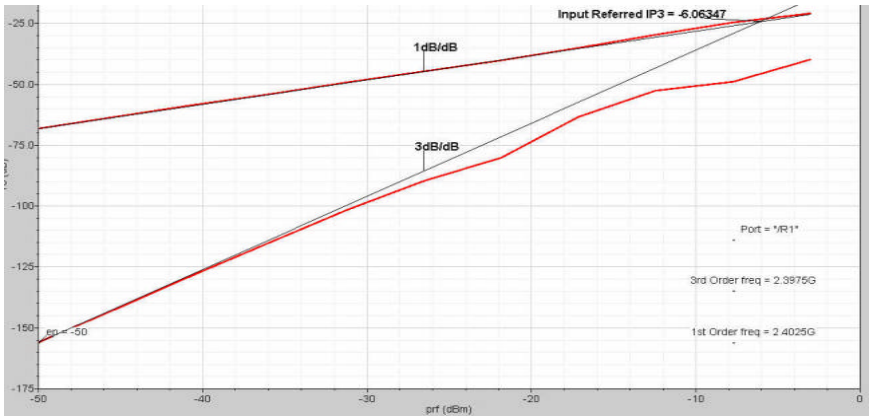

Fig. 10: IIP3 of LNA is -6.06347dBm

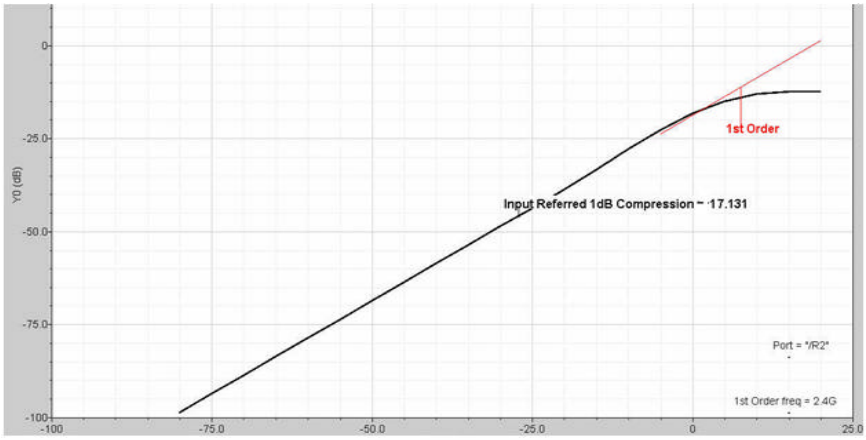

Fig. 11: The 1-dB Compression point of LNA is -17.131dBm

- Input return loss(- S_{11})= -8.597dB
- Power gain(S_{21})= 11.2 dB
- Reverse isolation(-S_{12})= <-60dB

The Current consumption and power dissipation obtained from 1.2V supply voltage are shown in Fig. 11 and 12, respectively power supply.

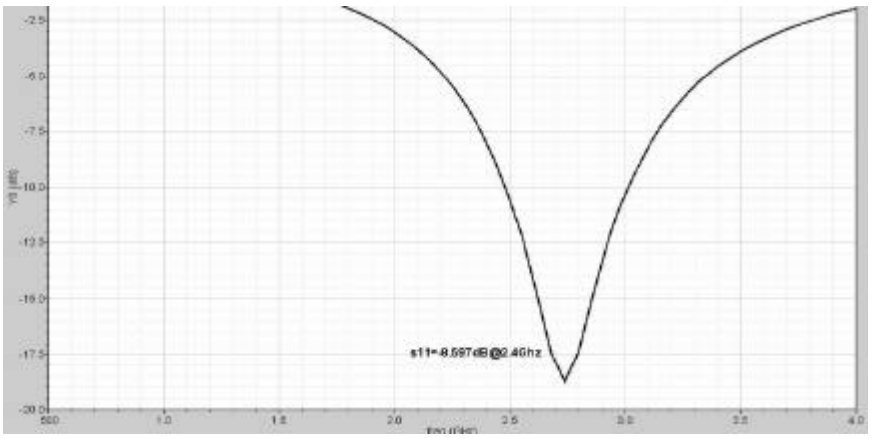

Fig. 12: S_{11} of LNA is -8.597 dB

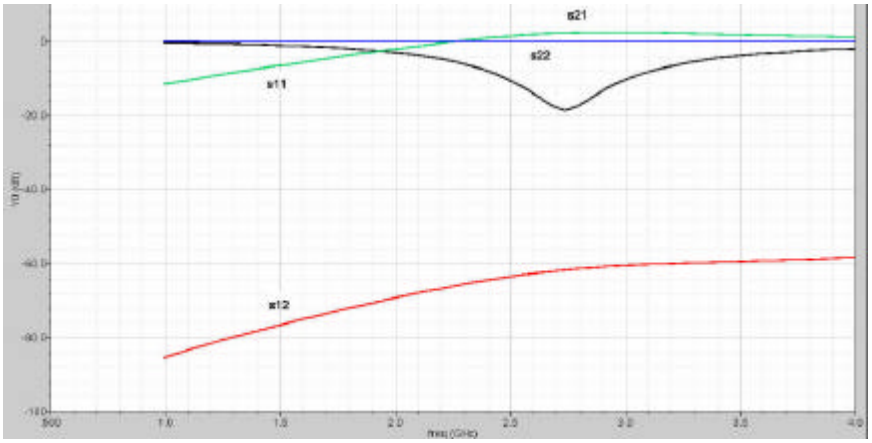

Fig. 13: S-Parameters of LNA

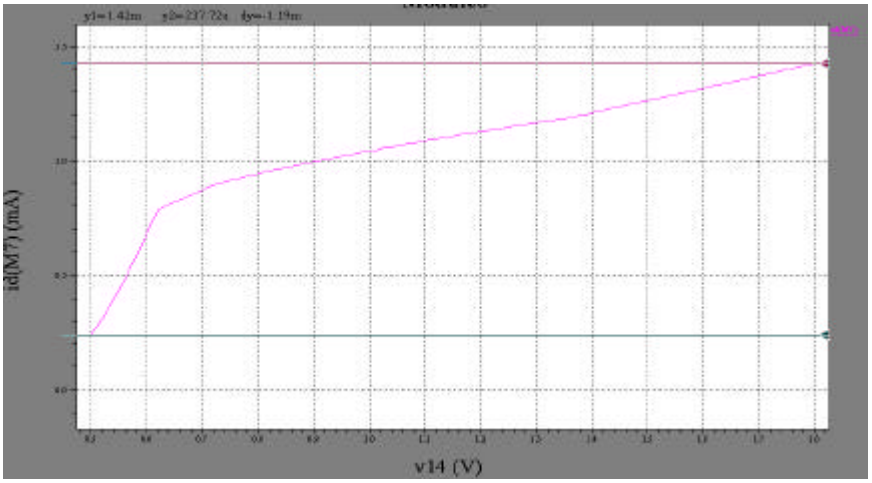

Fig. 14: Current consumption of 1.42mA from 1.2V supply

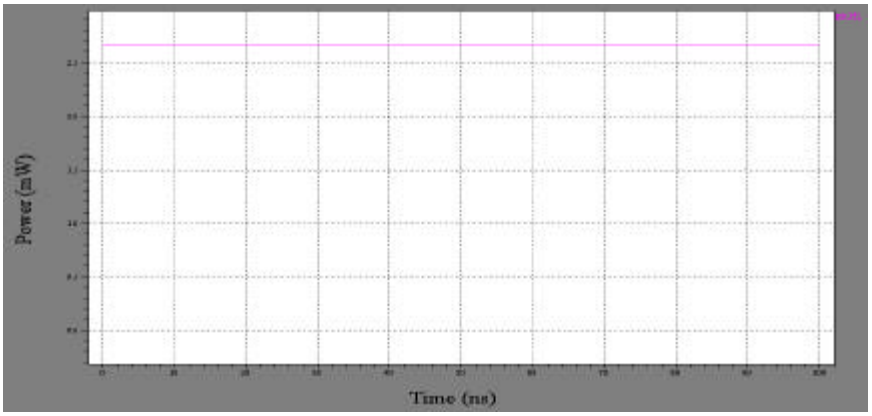

Fig. 15: Power dissipation of 2.7mW at 1.2V

Table 2: Comparison with previous papers

Parameters	Achieved value	Lin *et al.* (2014)	Toofan *et al.* (2007)
Center Frequency(GHz)	2.4GHz	2.4GHz	2.4GHz
Voltage Gain(dB)	38.5	24.03	37.6
Noise Figure(dB)	2.2	6.48	2.3
IIP_3(dBm)	-6.063	-14	--
Input return loss S_{11}(dB)	-11	-44.04	--
Power gain S_{21}(dB)	11.2	--	11.2
Reverse isolation S_{12}(dB)	-60	-27.3	<-60
Output return loss S_{22}(dB)	--	-9.6	--
1-dB compression point(dBm)	-17.13	-23.5	--
P_{dis} (mW)	2.7	2.53	2.7
Supply Voltage(V)	1.2	1.2	1.8
Technology	0.18	0.18	0.18µm CMOS

Comparison: The Table 2 shows comparisons of various parameters of designed LNA and other LNA work existing in literature.

CONCLUSION

Simulation results showed increased voltage gain with lower power consumption. Designed LNA has also better input impedance matching and suitable power gain. Hence, different topologies of the low noise amplifier are studied keeping in view the low noise requirements. The inductive source degeneration topology is chosen such that here is no noise due to the in put circuitry. With this topology, there quired input impedance of around 50Ω is achieved. The output load is a tuned circuit, constituting of a load inductance and the input capacitance of the following circuit. The amplifier is first designed to achieve noise optimization. The topology choose produced acceptable results.

With the advancing technology, inductors of different values,with reasonably good Q values can beintegrated for RF circuits. The performance of the circuit can be improved with the availability of a variety of inductor values at hand. The linearity of the circuit can be still improved from what is achieved in this research.

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