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Hybrid Architecture for Overlapped Test Vector Compression

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Abstract: This study depicts novel programmable low power test data compression architecture that permits formation of entropy encoded test scan envelope with exact and adaptable design in context of achieving continuous adjustment with the overlapped test vectors. The proposed architecture proficiently consolidates test compression with logic gates where both software and hardware strategies can work synergistically to convey top-notch test vector compression. Experimental results got from the simulation of proposed architecture add attainability of the proposed scheme and are accounted for test vector compression using hybrid i.e., both hardware and software based test data compression.

Key words: Built-in self-test, hybrid low power compression, low power test, test data compression, scan-based test, toggling

INTRODUCTION

Despite the fact that the essential goal of manufacturing, testing will remain basically the same to guarantee reliable and superb semiconductor items conditions and therefore test arrangements may experience a noteworthy advancement throughout the following years. The semiconductor innovation, outline qualities and the configuration procedure are among the key variables that will affect this development. With new sorts of imperfections that one will need to consider to give the sought test quality to the following innovation hubs, for example, 3D, it is suitable to offer the conversation starter of what matching Design For Testability (DFT) techniques should be conveyed.

Test compression, introduced ten years back, rapidly turned into the main stream DFT technique. In any case, it is vague whether test compression will be fit for coping with the quick rate of technological changes throughout the following decade. Interestingly, Logic Built-In Self-Test (LBIST) originally created for board, framework and in-field test is currently gaining acknowledgment for production test as it gives extremely hearty DFT and is utilized increasingly frequently with test compression. This half and half approach is by all accounts the following logical evolutionary stride in DFT. It has the potential for enhanced test quality; it might incredibly expand the capacities to keep running in conjunction with power aware tests and it can diminish the expense of manufacturing test while preserving all LBIST and scan compression focal points.

Endeavours to defeat the bottleneck of test data transmission capacity between the tester and the chip have made the idea of combining logic BIST and test data compression exceptionally basic innovative work territory. Specifically, a few cross breed BIST plans store deterministic top-up patterns (used to identify random pattern safe issues) on the tester in a compacted form and afterward utilize the existing BIST hardware to decompress these test patterns (Das and Touba, 2000; Dorsch and Wunderlich, 2001; Ichino *et al*., 2001; Krishna and Touba, 2003; Wohl *et al*., 2003; Jas *et al*., 2004; Li and Chakrabarty, 2005). A few arrangements install deterministic boosts by using packed weights or by perturbing the pseudorandom vectors in different styles (Wunderlich *et al*., 1996; Hellebrand *et al*., 2001; Liang and Kiefer, 2002; Touba and McCluskey, 2001; Li and Chakrabarty, 2004; Hakmi *et al*., 2007). On and off chance that BIST logic is utilized to convey compacted test data, then underlying encoding plots ordinarily exploit low fill rates as originally proposed in LFSR coding which hence advanced first into static LFSR reseeding (Hellabrand *et al*., 1995, 2001; Krishna and Touba, 2002; Gherman *et al*., 2004; Wang and Chakrabarty, 2006; Wohl *et al*., 2005; Hakmi *et al*., 2009) and afterward into element LFSR reseeding (Barnhart *et al*., 2002;

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Rajski *et al*., 2004). The careful studies of important test compression procedures can be found, for instance by Touba (2006) and Kapur *et al*. (2008). Likewise with ordinary scan-based test, half breed plans may expend more power than a circuit-under-test is appraised for. The resulting overheating or supply voltage commotion can bring about a gadget glitch, hence yield misfortune, increased chip dependability debasement, shorter item lifetime or even a lasting harm. Low power test compression plans (Rosinger *et al*., 2002); Lee and Touba, 2007 ; Wu *et al*., 2008; Liu and Xu, 2009) adjust again LFSR reseeding to diminish scan-in moves as the low fill rates make it conceivable to convey indistinguishable test data to scan chains for various movement cycles specifically from the decompressor, in this manner reducing the quantity of moves. Thus, low-move test pattern generators are key parts of numerous power aware BIST arrangements (Girard *et al*., 2001, 2010; Tehranipoor *et al*., 2005; Wang and Chakrabarty, 2006; Lin and Rajski 2010). Ordinarily, they utilize LFSRs to sustain scan chains through some kind of biasing logic such that the same qualities are more than once moved into scan chains for various movement cycles. Other BIST plans go for keeping the normal and crest power beneath a given limit by using gating logic to keep moves at memory components from propagating to combinational logic during scan shift (Gerstendorfer and Wunderlich, 2000; Zoellin *et al*., 2006). An exhaustive perspective of the low power test zone is given by Girard *et al*. (2001, 2010). Pseudorandom test patterns produced with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date Built-In-Self-Test (BIST) based pseudorandom test pattern generators is achieved by a Low Power (LP) programmable generator described in (Filibek *et al*., 2015).

As of late, a Pseudorandom Test Pattern Generator (PRPG) was proposed for low power BIST applications (Solecki *et al*., 2012). The generator goes for reducing the switching action during scan loading. The exceptionally same generator permits completely mechanized choice of its controls so that the resultant test patterns highlight craved preselected toggling rates. In this study, we exhibit that the same generator can likewise effectively go about as a test data decompressor, along these lines allowing one to execute a crossover test approach that combines LBIST and ATPG-based implanted test compression. This is the principal low power test compression conspire that gives originators a chance to shape the power envelope in a completely unsurprising, precise and adaptable design. Additionally, both strategies can supplement each other to address, for instance, a voltage drop brought on by a high switching movement during scan testing, constraints of at-speed ATPG-delivered test patterns or new blame models. As said before, this paper introduces a completely programmable low power test compression conspire that is integrated in each route with a power aware pseudorandom test pattern generator.

MATERIALS AND METHODS

Experimental Setup: Keeping in mind the end goal to exhibit the viability of the proposed test compression architecture, independent simulations were conducted. An automatic test generation project was first utilized for obtaining a set of test vectors giving 100% fault scope. The proposed compression architect was implemented in MATLAB programming environment on a Windows machine having Quad-center 2.5-GHz Ultra processor with 8GBs of RAM. On account of space constraints, only some partial results of the circuits are given. All the test vectors required for testing the SOC are first compacted in software mode. The packed test vectors and an efficient decompression system are then stacked into the simulation of embedded handling core of the SOC. The processor executes the decompression process and afterward applies all the uncompressed unique test vectors to every centre of SOC for generating and breaking down the output responses.

Architecture for test data compression: Figure 1 shows the proposed Simulink architecture for test data compression. In this compression technique all the test vectors are divided into several blocks comprising of equal size where the size of this blocks depends on the proportionality of bits in each vector. Here, the idea of compression is that primarily passed test vectors are considered as reference test vectors whereas the consequent vectors are generated from the weighted evaluation of the referenced one by storing those blocks/bits that exhibits difference with it. This will allow us to compress and recover the whole set of test vectors during the decompression process. The entropy of the test data is compressed using the estimated weighted factors deduced from the presented algorithm. It is applied for compression on test data set as a matrix of size m x n. Here, scan line generator block is used to generate several scan lines based on the following logic. Each of the rows belonging to C scan lines are divided into blocks of equal size. Owing to the structural relationships among the faults there tends to be many similarities between test vectors. Hence, this test vectors can be ordered optimally such that the successive test vectors experience difference by just a fewer number of blocks. Thereby, reducing the amount of information is requisite for storing these differences will comparatively fall beyond the size required for storing the entire test vectors.

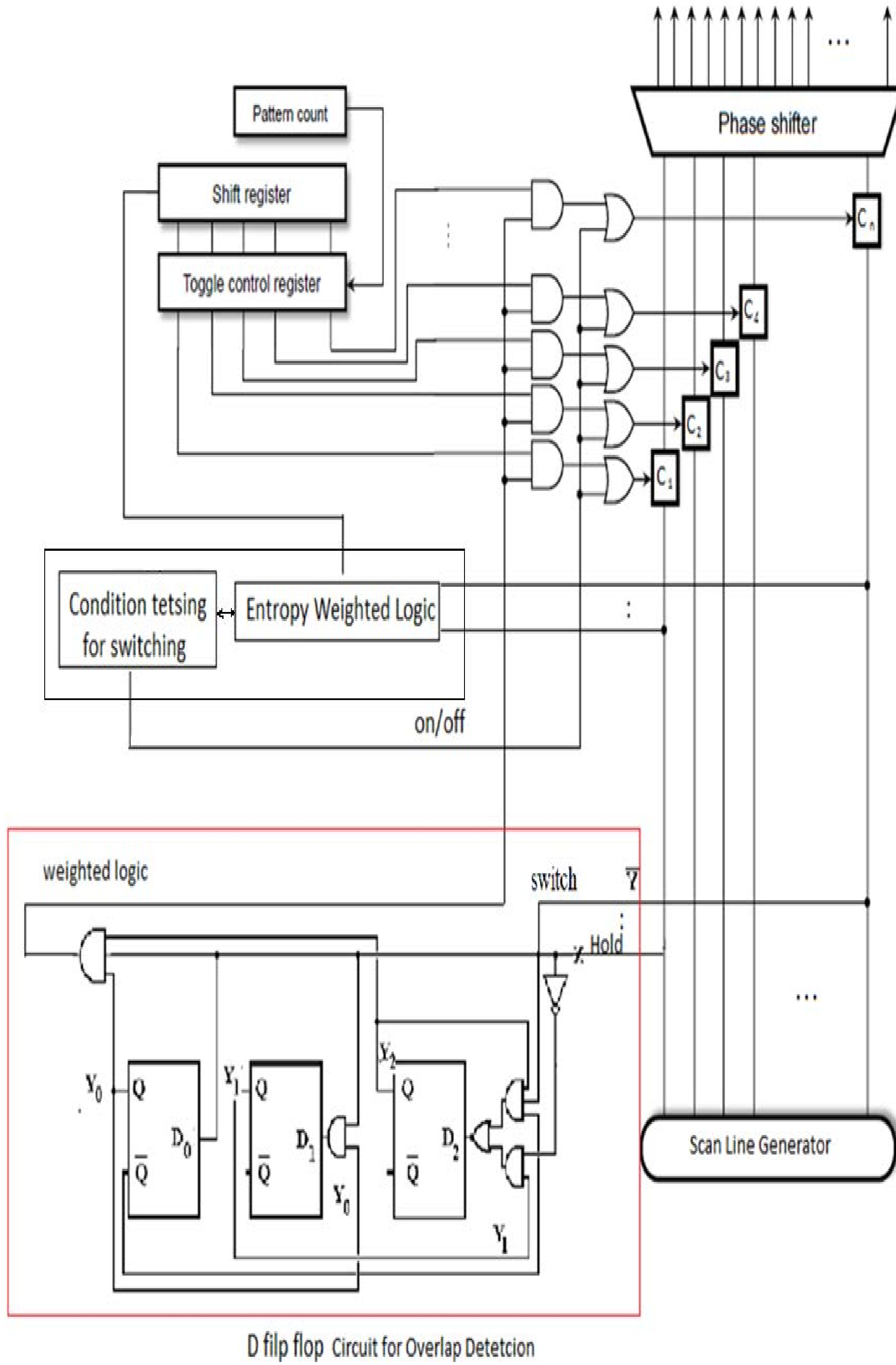

Fig. 1: Simulink block diagram of test vector compression

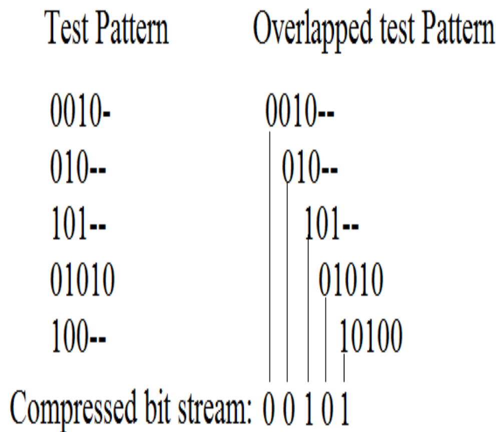

Fig. 2: Mechanism of overlapping bit compression using d flip flop based circuitry

Let C_K, be the test vectors where k = 1,2,3,… n of size m x n and N is the block size of data. Thus, the entropy of this test vector can be represented in Eq 1:

$$E(C_K)=-\sum_{i=1}^{n} P_i * \log_2 P_i \quad (1)$$

Where:

C_K = $\{C_1, C_2, \ldots C_n\}$

P_i = The index of bits

b_K = The weighted indices distances corresponding between the adjacent blocks of the test vectors

Since, the distribution changes with time, therefore it is necessary to use an encoding scheme with respect to the changing time. Thus, the distance frequency for the distribution of indexes needs optimum parameters for each C_K and C_K respectively. This correspond to the hard problem because of the increase in size relegates the necessity of general solution. Thus, for a given k distance of good vectors, the problem is in the fact that how we will encode each section of the scan vectors and what is the best parameter for reducing the size of encoded data is derived from EHMCA (Entropic Hidden Markov Chain Algorithm); where the data needs to be pre-processed or divided into scan lines of test vectors using Eq. 2:

$$C_K=-\sum_{i=1}^{m} C_0(K_i)+\sum_{i=1}^{K_i} C_0(b_i)+\ldots+\sum_{i=K_{m-1+1}}^{K} C_m(b_i) \quad (2)$$

Where:

$C_i(.)$ = The required size to encode the indices value at each section

Having instantiated the generated scan lines the data is dispatched to the D flip flop based overlap detection circuitry. The mechanism of bit overlapping is illustrated in the Fig. 2. This architecture by and large tries to discover bordering and continuous test bit patterns having the most maximum overlap. Deterministic test examples are created by an ATPG and compacted. Pattern in the scan chain are checked whether they coordinate with one or more test examples which were not utilized in the sequence yet. The comparing rundown of transitions is utilized to touch base with the underlying span of the switching, hold and weighted equalizer logic as the yield. These qualities are picked conservatively such that the proportion switching/hold is insignificant and there are no transitions inside a solitary hold period. The previous condition guarantees that the given template can at present oblige some of recently delivered test solid shapes. The last condition can be reworded as takes after: for every move either its range is more noteworthy than hold period or possibly one of its flanking bits exists in a switching period.

Followed by the process of compressing overlapped bits separately, the weight indices of the derivative bits are checked under module named condition testing for switching; where the optimum weighted parameter is determined using the following EHMCA algorithm. The algorithm is explained as follows. We assume the $P(C_K|C_{K-1})$ is independent of K which leads to the definition of the stochastic transition matrix $K = \{K_{ij}\} = P(C = j|C_{K-1} = i)$ The initial state distribution of the primary test vector (i.e. when K = 1) is given in Eq. 3:

$$t_i = P(C_1 = i) \quad (3)$$

The observation variables 0_K can take one of K possible values. The probability of a certain observation at K index for state j is obtained by Eq. 4:

$$b_i(0_k) = P(0_K = 0_t|C_t = j) \quad (4)$$

Taking into account all the possible values of 0_K and C_K we obtain the weighted b_K i.e., indices distances corresponding between the adjacent blocks by N matrix An observation sequence is given by. Thus, we can describe a hidden Markov chain by initializing the computing with $\theta = (C, 0, \tau)$ iteratively updating for local weighted maximum for. Algorithm: Entropic Hidden Markov Chain Algorithm (EHMCA) for test data:

Input: entropy based divided test vectors

Output: compressed test vectors and is the expected weighted indices distance corresponding between the adjacent blocks of the test vectors.

Step 1: Set $\theta = (C, 0, \tau)$ with random initial conditions by using prior information of primary test vector.

Step 2: Recursively determine the probability for the continued manifestation of bits. Let $\alpha_i(K) = P(0_1, 0_2 = 0_2,..., 0_T = 0_T, C_K = I|\theta)$,the probability of appearing $0_1, 0_2,..., 0_K$ the and being in state i at time K and j at time K+1 is represented in Eq 5 and 6:

$$a_i(1)=t_i b_i(0_1) \quad (5)$$

$$a_i(K+1) = b_i(0_{t+1})\sum_{i=1}^{N} a_i(K)a_{ij} \quad \mathbf{(6)}$$

Step 3: Calculate the temporary variables from the test vectors, by evaluating the transition probability of bit being in state i at time K given the spotted sequence O and the parameters θ (using the Bayes' theorem) is given in Eq. 7:

$$T_i(K)=P(C_k=i|0,?) \quad (7)$$

Step 4: Calculate the probability of being in state i and j at times K and K+1 respectively given the observed sequence O and parameters θ by the Eq 8:

$$f_{ij}(K)=P(C_K=i,C_{K+1}=j|0,?) \quad (8)$$

Step 5: Update θ in order to resolvethe expected number of transitions from state i to state j in comparison to the expected total number of shifts away from state i using Eq 9: $t_i^* = T_i(1)$ Expected frequency spent in state i at time 1:

$$t_{ij}^* = \frac{\sum_{K=1}^{K-1} f_{ij}(t)}{\sum_{K=1}^{K-1} T_i(t)} \quad \mathbf{(9)}$$

Step 6: Compress the bits by replacing 1 or 0 with r and simultaneously determining the final weighted vectors for the number of shifts away from state i that do not mean transitions to a different state j but but to any state including it self using Eq. 10. This is corresponding to the no of times state i is detected in the sequence from K = 1 to K-1:

$$b_K^*(r)=\frac{\sum_{K=1}^{K} 1_{0K=r} T_i(k)}{\sum_{t=1}^{T-1} T_i(K)} \quad (10)$$

where, b_K^* is the expected weighted indices distance corresponding between the adjacent blocks of the test vectors such that the number of times the output observations have been equal to while in state i over the expected total number of times in state i by Eq 11:

$$1_{0K=r} = \begin{cases} 1, & \text{if} 0_K = r \\ 0 & \text{otherwise} \end{cases} \quad (11)$$

Step 7: Repeat Steps 4-6 iteratively until $P(0|\theta_{final}) > P(0|\theta)$ is reached.

Step 8: Recalculate the entropy of the compressed test vector using Eq 12.

$$E(o_K)=-\sum_{i=1}^{n} P_i * \log_2 P_i // \text{for} 0_K = \{0_1, 0_2, ...0_n\} \quad (12)$$

where, $p_i = p_{i-1} + b_K^*$.

Step 9: Stop Having set all up important conditions, one can continue with the test specified bit encoding through the mix of shifting and counting the pattern of bits through the shift register, pattern count module over toggling of register control. This achieved in a way like that of the ordinary EDT stream. It is significant, notwithstanding, that interest of a given test bit pattern in a template does not ensure its real combining and pressure in view of either bit clashes on certain predetermined bits with other test blocks or constrained encoding abilities. Another prominent distinction between the displayed approach and a conventional EDT plan is the way compression process is aborted. Here, the test bit pattern is encoded with different weighted indices, to frame a template, which thusly alters conditions. Consequently, all the processed bit is accounted for low power consuming template and is then picked as the main part of a test vector. All compacted test scan lines are expelled from the entropy encoded bit pool, through the phase shifter module otherwise the computation proceeds by making another arrangement of templates until the length of the pool is not vacant. Once the above technique finishes, one need to ensure that all scan chains facilitating transitions are enabled. This can be accomplished for the length of time until there is no less than one switch enable phase shifter switching input that nourishes a given scan through a XOR logic gateway inside the phase shifter. Finding the insignificant subset of the switch control register stages expected to enact the required scan chains is equal to taking care of the minimum hitting set problem. In this study, we used the greedy approach to come up with the optimized solution of the problem.

In comparison with the desired switching ratio on/off chance that the resultant switching is underneath the ratio, then the weighted test template pattern for compression encoding can be at last acknowledged as a part of the template. Or else, the weighted test pattern is not compressible given the encoding constraints and must be disposed of. The weighted template comes back to its underlying status. When the total sum of templates has been initialised, the circuitry endeavours to connect the encoded bit with the rest of test bits. On the off a chance that template cannot oblige certain transitions included by a recently picked test vector, then the spans of switch, hold, and counterbalance periods can be further balanced. On the off chance that the test bits fits to the template and new dynamic scan chains are known, then we recalculate both the substance of the flip control register and the switching rate. Once more, if the switching is above, then the template comes back to its past structure, while the test bit scan line is gone to the following template. Besides, if none of the current templates can oblige the block, it stays in the pool until another arrangement of templates is produced such that this specific scan line can be in the long run allotted to its assigned LPT.

RESULTS AND DISCUSSION

The investigation results reported here evaluates execution of the new compression architecture. Trials are made on a few industrial circuitries whose qualities, including scan architecture. Figure 3 and 4 are given in Table 1. Simulation results obtained from simulink simulator presents after effects of investigations led with 64-bit compressor and the fancied scan shift-in switching level set to 15, 20 and 25%. For scan shift operations, the normal Weighted Transition Metric (WTM) gauges the resultant switching action by checking the quantity of conjured transitions in scan cells and considering their relative positions. To quantify flipping in the catch mode, the switching action at every door in the circuit is recorded by method for the normal Weighted Switching Activity (WSA). All investigations are directed in a manner that the first EDT-based test scope is constantly protected. We have additionally watched a comparable pattern for other switching rates in each test situation. It is important that diminishing the heap switching positively affect switching action amid catch and emptying of scan chains. This is additionally worth watching that the proposed arrangement is the principal low power pressure plot that offers an instrument to shape the force envelope in such an adaptable and precise style.

Table 1: Compression and Power Reduction Percentage of Experimented ISCAS'89 Benchmark

Test Si. No	Total original bits	Output compressed bits	Comp ression (%)	Power reduction (%)
C7552	2934	427	85.43	73.05
C6288	3342	516	84.54	77.03
C5315	3832	562	85.32	79.04
C3540	4786	754	84.23	78.06
C2670	5679	1002	82.34	78.07

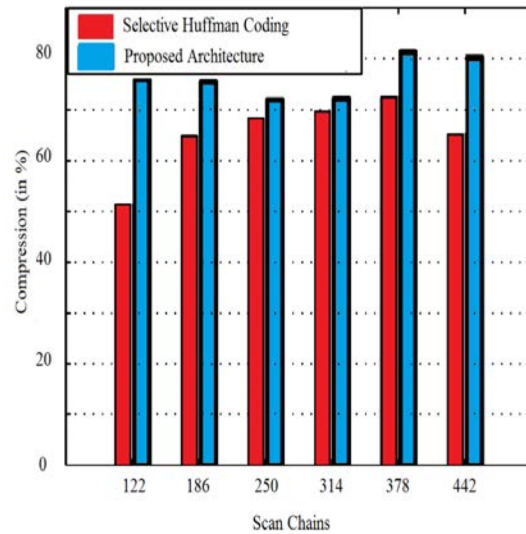

Fig. 3: Compression performance plot of the proposed architecture for different sizes of scan chains

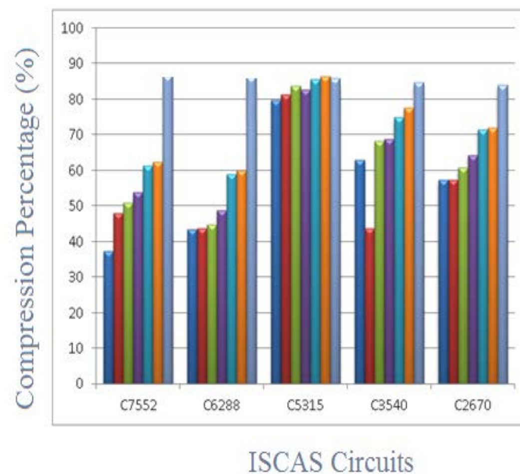

Fig. 4: Compression of performance with proposed method and that of past method in the literature

CONCLUSION

As presented in the study, the recently discussed low power architecture is equipped for as a completely

practical test data compressor with capacity to decisively control scan shift-in switching action through the procedure of encoding, its low power test logic requires impressively littler measure of silicon land than that of the current low power compression plans. The proposed arrangement allows one to effectively consolidate test compression with programming based compression logic where both strategies can work synergistically to convey excellent test. It is along these lines an extremely appealing low power test plot that allows for exchanging off test scope, sum of patterns and flipping rates.

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