Asian Journal of Information Technology 15 (4): 750-755, 2016
ISSN: 1682-3915

Low Power and Area Efficient Full Adder Design Using GDI Technique

Dhandapani Samiappan and R. Srinivasan
Department of ECE, Saveetha Engineering College, Chennai, India

Abstract: Full adder is the basic building blocks for various arithmetic circuits such as carry select adder, array multipliers, ripple carry adder, high speed adder, parallel adder and so on. In order to improve the performance of the digital computer systems one must improve the basic full adder cell. The proposed full adder design by using Gate Diffusion Input/Index (GDI) technique reduces the power consumption with less transistor count while maintaining less interconnection nodes of logic design, when compared with existing full adder designs such as complementary pass transistor logic, standard CMOS logic, transmission gate logic and transmission function adder logic. The simulation was carried out on TSMC HSPICE 180 nm technology. The simulation result shows that the design has more efficient with less area, less power consumption and as compared to existing hybrid full adder techniques.

Key words: Low power, area, CMOS, GDI, HSPICE

INTRODUTION

Addition is a fundamental operation that is mostly used in various VLSI systems such as application-specific digital signal processing architectures and micro processors. A full adder is a combinational circuit that produces the arithmetic sum of three bits. It has three inputs and two outputs. Two of the input variable, indicated by A and B, represent the two notable bits to be connected and the third input C, represents the carry from the former lower notable location. Two outputs are represented by the characters S for sum and C for carry. The basic of many arithmetic operation proceeds the reality into thought, the design of a GDI full adder consume less power and less complexity of circuit considerable regard for the execution of recent digital systems (Aguirrre-Hernandez and Linares-Aranda, 2011). The existing full adder design and showing comparison of GDI full adder cells executed with an ripple carry adder, array multiplier and carry select adder based on multiple of the Boolean functions AND/OR and MUX to equitable power in sum and carry outputs. There are four sources of power decadence: dynamic switching power due to the charging and discharging of load capacitance, leakage current through reverse biased diodes and sub threshold conduction, short circuit current power due to finite signal rise/fall times and static biasing power found in some logic style (i.e., pseudo-NMOS), there are following three prime elements of power decadence in complementary Metal Oxide Semi-conductor (CMOS) circuits.

Switching power: The power dissipated in charging and discharging the load capacitances is called switching power.

Short circuit power: Short circuit path exists for direct current flow from VDD to the ground terminal.

Static power: Static power dissipation in CMOS is due leakage currents and is small in comparison to other component

The main objective of GDI full adder is better presentation like a power consumption and transistor count differentiate with the previously existing ones. The GDI full adder circuit was executed using 180 nm technology by using TSMC HSPICE Simulation tools. The average power consumption (0.7535 μW) of the proposed GDI full adder circuit.

Literature review: There are different designs technique to implemented a digital logic circuit. In this regard, many innovative designs for basic logic functions have appeared in the literature recently. This includes static CMOS, CPL, transmission gates, pass transistor logic. CMOS transmission gates also known as CMOS pass gates consist of one PMOS and NMOS transistor, attached in parallel and complementary signals are applied to gate of both transistors (Goel *et al*., 2003). This transmission gates works as a bidirectional switch. The complexity of CMOS pass gate logic can be reduced by adopting CPL. All consists of purely NMOS transistors for logic operations. All inputs are applied in complementary form and output is also obtained in complementary form. The conventional CMOS adder cell using 28 transistor based on standard CMOS technique.

Corresponding Author: Dhandapani Samiappan, Department of ECE, Saveetha Engineering College, Chennai, India

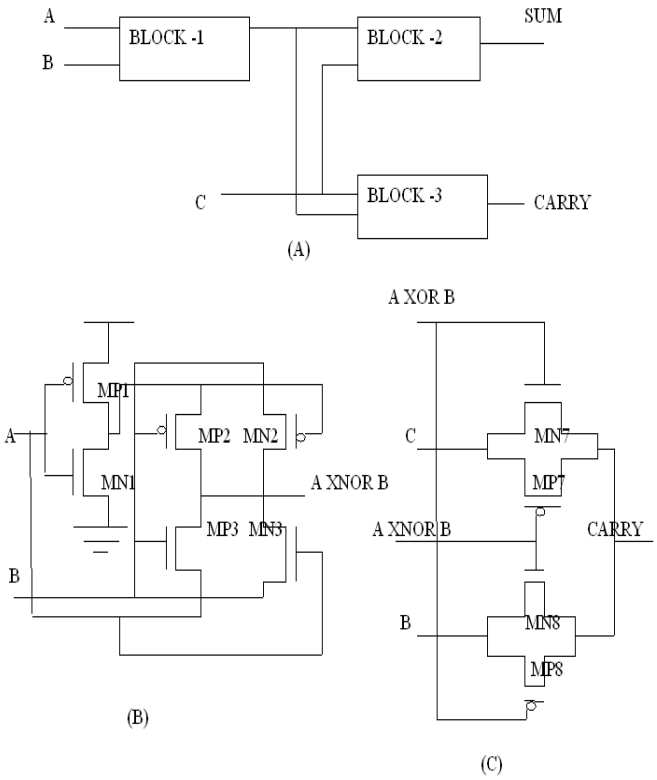

Fig. 1: a) Existing full adder schematic structure; b) XNOR generation and c) Carry generation

Due to large number of transistors, its power consumption also increase, speed reduces and it also occupies larger area (Hassoune *et al*., 2010). Larger PMOS transistor in pull up lattice produce in high input capacitances which source increase in dynamic power dissipation and larger delay. One of the most remarkable benefit of this full adder large noise margins and thus dependable behavior at low voltages. the CPL is not acceptable alternative for low power approach, it consist of 32 transistors and large interconnection node, high power, high transistor count, compare to CMOS full adder (Navi *et al*., 2009). The voltage degra dations was successfully in Transmission gate full adder which uses only 20 transistors for full adder executed. The other demerits of CPL likes large power consumption and less speed. The transmission gate full adder and standard CMOS full adder consume high power and interconnection node compare to proposed GDI full adder and existing hybrid full adder.

Existing system: The existing hybrid full adder circuit is consists by three blocks. Block1 and 2 are XNOR blocks that provide the sum output and block3 generate carry output. Each module design separately such that the whole adder circuit is performance in terms of power and transistor count (Fig. 1).

XNOR generation: In the existing hybrid full adder circuit, XNOR block is accountable for most of the power consumption of the whole conventional full adder circuit. Therefore, XNOR generation is planned for providing the sum output and it avoids the voltage mortification change. Full voltage oscillation of the levels of output is generated by the level replace transistors, MP3 and MN3. The XNOR generation investigated in use 6T to get preferable logic performance contrast with CMOS logic, transmission gate and CPL full adder (Bhattacharyya *et al*., 2015).

Carry generation: In the existing hybrid full adder circuit, the output carry signal is obtained by using transmission gate logic. The transistors MP7, MN7, MP8 and MN8 provide full adder carry output. The input carry signal is propagated only between a one transmission gate (Prashanth and Swamy, 2011). It minimizes the overall carry propagation path when compared to conventional full adder circuit.

Operation of the hybrid existing full adder: Existing hybrid full adder sum output is obtained from XNOR blocks. The CMOS inverter comprises of transistors MP1 and MN1 with input B, adequately used to design the

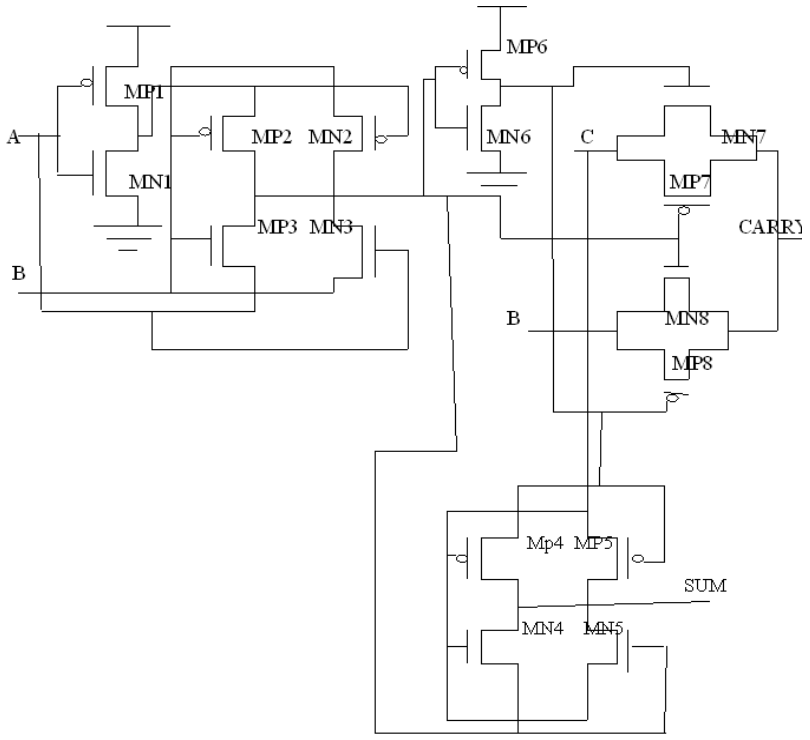

Fig. 2: Existing hybrid full adder

managed inverter using both the transistors MN2 and MP2 (Foroutan *et al*., 2014). But, it has some voltage mortification issue which has been separated using two pass transistors MP3 and MN3. PMOS transistors (MP4, 5 and 6) and NMOS transistor (MN4, 5 and 6) perceive the two blocks to device the entire SUM function (Wairya *et al*., 2011). Consider the truth table of full adder, If A = B, then carry = B, else carry = cin (Fig. 2).

MATERIALS AND METHODS

Proposed GDI full adder: GDI technique is used to decrease the power consumption and area with low complexity. Here, 12T GDI based full adder circuit will be able to perform low power applications.

The Gate Diffusion Input/Index (GDI) is a new method for minimizing the power consumption and area. The GDI allows the performance of a wide complicated logic function by using only two transistors (Zavarei *et al*., 2011). This technique is acceptable for the design of a fast, low power adder circuits. This technique is used to decrease the number of transistors and differentiate the CMOS and the existing hybrid full adder logic methods. It contains two transistors, PMOS transistor and NMOS transistor. It is flexible than the CMOS design because in CMOS design, VDD is connected to the source of PMOS and GND (ground) is connected to the source of NMOS. But, in the GDI technique, instead of VDD and GND, it uses two extra

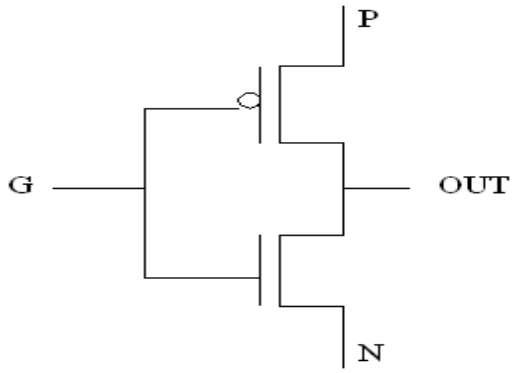

Fig. 3: Basic GDI structure

Table 1: Logic function GDI technique

G	N	P	Output	Function
A	GND	VDD	A’	NOT
A	VDD	B	A+B	OR
A	B	GND	AB	AND
A	GND	B	A’B	F1
A	B	VDD	A’+B	F2
A	C	B	B+AC	MUX

input pins. So totally, we have three inputs in a GDI logic design. The logic function of GDI technique is given in Table 1 and Fig. 3.

Substrate of NMOS and PMOS pair are attached to N or P (appropriately), so it can be approximately biased in variation with the CMOS inverter. It cannot be announced to all the functions that are manageable in

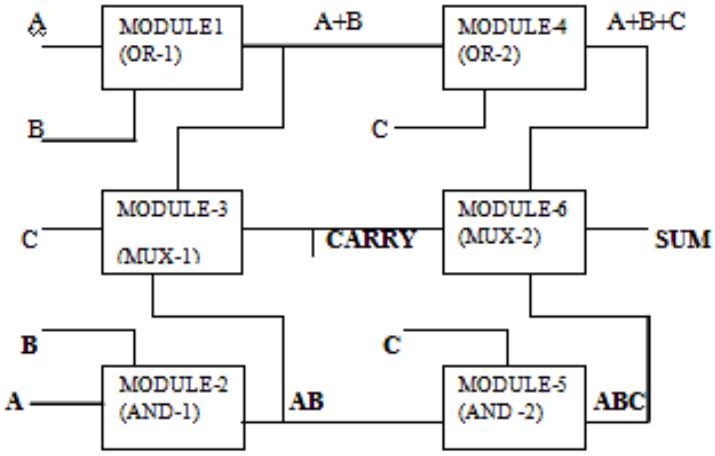

Fig. 4: The GDI full adder schematic structure

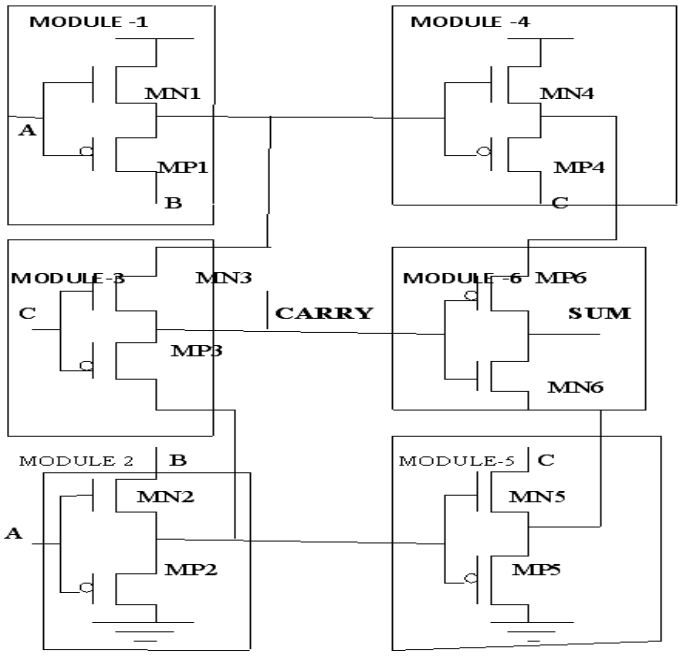

Fig. 5: Proposed GDI full adder

excellence like p-well CMOS operation but can be strongly executed in twin-well CMOS or SOI technologies. Thereby, there is no direct impediment track connecting VDD and GND as in the case of CMOS logic.

GDI full adder schematic structure is shown in Fig. 4. The proposed GDI full adder in sequence to execute (A OR B) the N input is attached to VDD, P is attached to B and G is attached to A as shown in Fig. 5, Module-1 is a GDI execution o f (AORB). In the upcoming step (AANDB) is planned by G attached A, N is connected to B and P is connected to GND, appropriately.

Module-1: The module-1 performs OR gate operation. The G is wired to A, P is connected to B and N is wired to VDD:

$$\text{Output} = A+B$$

Module-2: The module-2 performs AND gate operation with G input connected to A, P is wired to B and N is wired to the GND:

$$\text{Output} = AB$$

Module-3: The module-3 performs multiplexer producing carry, C is attached to G and the latter acts as a GDI multiplexer selector line and N is attached to the

module-1 output and P is attached to the module-2 output. The equation below shows the implementation of multiplexer:

$$\text{Carry} = (A+B)C+C'(AB)$$
$$= AC+BC+ABC'$$
$$= AC+ BC(1+A)+ABC'$$
$$= AB+BC+AC$$

Module-4: The module-4 performs OR gate operation, G input is connected to module-1 output, P is wired to C and N is connected to VDD:

$$\text{Output} = A+B+C$$

Module-5: The module-5 performs AND gate operation, G input is wired to module-2 output, p is connected to GND and N is wired to C:

$$\text{Output} = ABC$$

Module-6: The module-6 performs multiplexer operation to produce the SUM output, G input is connected to carry and p is wired to module-4 output and N is connected to module-5 output:

$$\text{SUM} = A \text{ XOR } B \text{ XOR } C$$

RESULTS AND DISCUSSION

The existing hybrid full adder output wave form is shown in Fig. 6. Here, we can observe the 12 transistors which are useful to design the GDI based full adder. Wave forms for the proposed GDI based full adder is shown in Fig. 7.

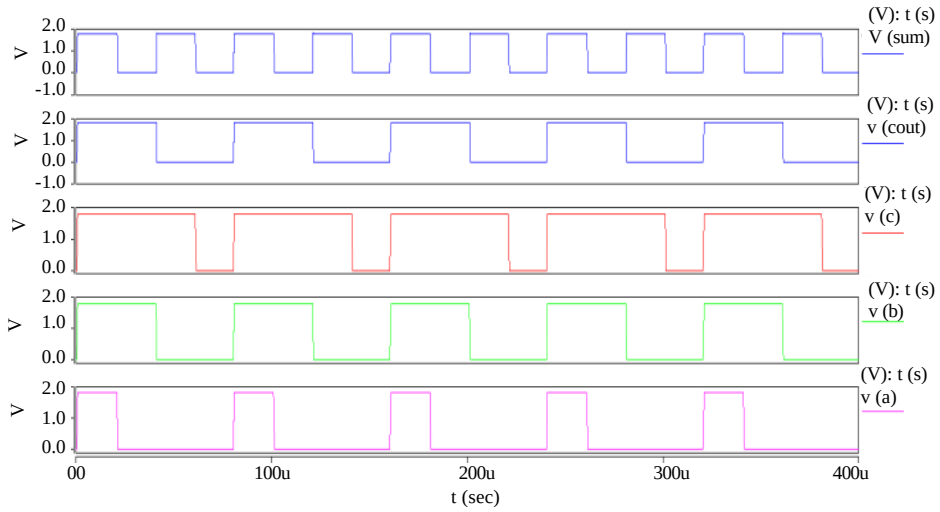

Fig. 6: Existing full adder output wave form

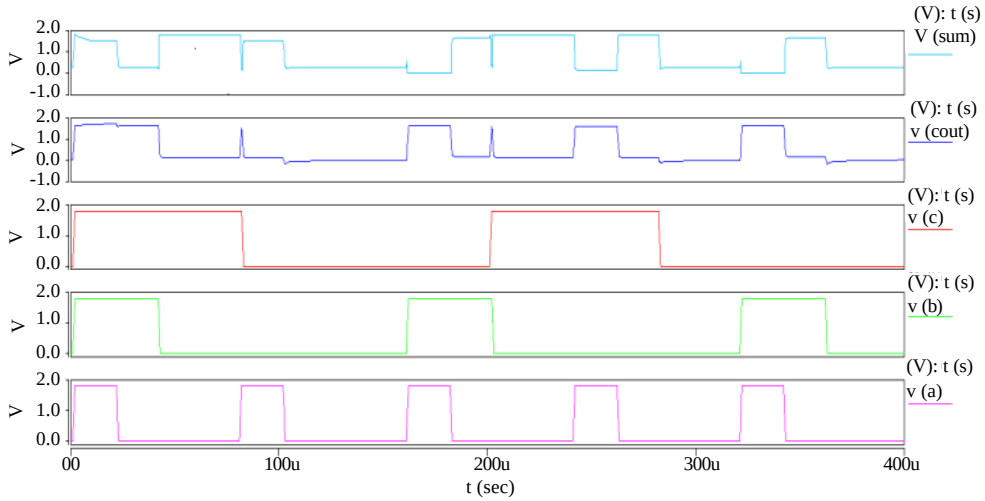

Fig. 7: Proposed GDI full adder output wave form

Table 2: Power comparision

Name of the circuit	Power (μw)	Transistor count
Static CMOS	9.1290	28
TGA	15.3800	20
TFA	7.5180	16
Existing	3.7650	16
GDI MUX	0.7535	12

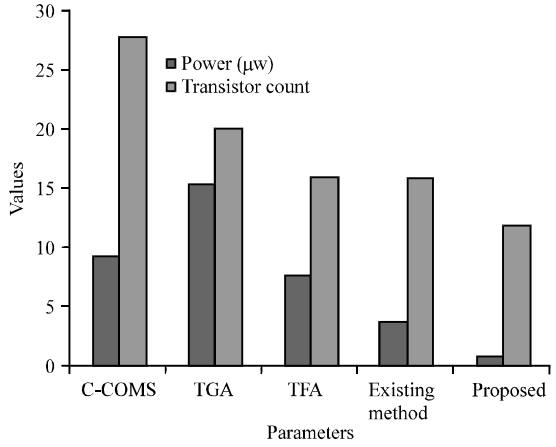

Fig. 8: Comparison chart

Here, we can observe the waveforms for all combinations. When, the inputs A = 0, B = 0 and C = 0, the both outputs Sum = 0 and carry = 0. When, A = 0, B = 0 and C = 1 then the output sum = 1 and carry = 0. When, A = 0, B = 1 and C = 0 then the output Sum = 1 and carry = 0. When, A = 0, B = 1 and C = 1 then the output sum = 0 and carry = 1. When, A = 1, B = 0 and C = 0 then sum = 1 and carry = 0. When, A = 1, B = 0 and C = 1 then the output sum = 0 and carry = 1. When, A = 1, B = 1 and C = 0 then the output Sum = 0 and Carry = 1. When A = 1, B = 1 and C = 1 then both outputs sum = 1 and carry = 1. Power comparison for various circuits along with transistor count is given in Table 2 and diagrammatically represented in Fig. 8.

CONCLUSION

The GDI full adder design provides a low power and area with immense signal probity and operating capacity. The full adder circuit is optimized for efficiency at 180 nm TSMC operation technology. Simulations have been executed on HSPICE to assess the new design as well as alternative adders including static CMOS, CPL, TGA, TFA and existing hybrid full adder.

REFERENCES

Aguirrre-Hernandez, M. and M. Linares-Aranda, 2011. CMOS Full-adders for energy-efficient arithmetic applications. Trans. Very Large Scale Integration Syst., 19: 718-721.

Bhattacharyya, P., B. Kundu, S. Ghosh, V. Kumar and A. Dandapat, 2015. Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit. IEEE Trans. Very Large Scale Integrat. (VLSI) Syst., 23: 2001-2008.

Foroutan, V., M. Taheri, K. Navi and A.A. Mazreah, 2014. Design of two low-power full adder cells using GDI structure and hybrid CMOS logic style. Integrat. VLSI J., 47: 48-61.

Goel, S., M.A. Elgamel and M.A. Bayoumi, 2003. Novel design methodology for high-performance XOR-XNOR circuit design. Proceedings of the 16th Symposium on Integrated Circuits and Systems Design, September 8-11, 2003, IEEE., pp: 71-76.

Hassoune, I., D. Flandre, I. O'Connor and J.D. Legat, 2010. ULPFA: A new efficient design of a power-aware full adder. IEEE Trans. Circ. Syst. I: Regular Papers, 57: 2066-2074.

Navi, K., M. Maeen, V. Foroutan, S. Timarchi and O. Kavehei, 2009. A novel low-power full-adder cell for low voltage. Integrat. VLSI J., 42: 457-467.

Prashanth, P. and P. Swamy, 2011. Architecture of adders based on speed, area and power dissipation. Proceedings of the World Congress on Information and Communication Technologies, December 11-14, 2011, Mumbai, pp: 240-244.

Wairya, S., G. Singh, R.K. Nagaria and S. Tiwari, 2011. Design analysis of XOR (4T) based low voltage CMOS full adder circuit. Proceedings of the IEEE 2011 Nirma University International Conference on Engineering, December 8-10, 2011, Ahmedabad, Gujarat, pp: 1-7.

Zavarei, M.J., M.R. Baghbanmanesh, E. Kargaran, H. Nabovati and A. Golmakani, 2011. Design of new full adder cell using hybrid-CMOS logic style. Proceedings of the 18th IEEE International Conference on Electronics, Circuits and Systems, December 11-14, 2011, Beirut, pp: 451-454.