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A Comprehensive Survey on Filter Bank Designs for Digital Hearing Aids

[1]N. Subbulakshmi and [2]R. Manimegalai
[1]Department of ECE, Sri Ramakrishna Engineering College, Coimbatore, India
[2]Park College of Technology, Coimbatore, India

Abstract: In Digital Signal Processing (DSP) systems, filter banks are an integral part of many audio signal processing algorithms. In digital hearing aid applications, multi-channel dynamic range compression is used to perform acoustic echo cancellation and speech enhancement is achieved using noise reduction algorithms. The design of filter bank has significant impact on the performance of DSP systems in terms of complexity, delay and quality of the signal. This study provides a comprehensive survey on various filter bank algorithms and also presents a detailed performance analysis of those algorithms. This study also discusses the parameters involved in selecting the best filter bank for processing the audio signal in signal processing applications. Various parameters to design a filter bank for digital hearing aids are: noise, delay and power. This study, describes the basics of DSP algorithms including the design of digital filter banks. It also briefly summarizes the filter bank design algorithms and techniques available in the literature. Most of the filter banks and algorithms have been implemented on FPGA and evaluated. This study also provides the various hardware implementations of filter bank designs on FPGA for the hearing aid applications.

Key words: Finite impulse response, filter bank, DSP algorithms, signal processing, hearing aids, dynamic range

INTRODUCTION

There is an increasing demand for filter bank in recent years, due to the emerging trends towards portable electronic devices in audio signal processing. The need for such devices is increasing as a result of migration from large to compact systems. A variety of signal processing algorithms are used to design a hearing aid device with enhanced speech quality. Auditory compensation is a process which compensates the hearing loss of the hearing impaired people. Spectral resolution, noise tolerance and hearing range are some of the factors that make the digital hearing aids more complex as discussed by Dillon (2001). Filter bank forms most of the signal processing circuitry in a digital hearing aid. Filter banks are mainly applied for many image and signal processing applications. Important factors to design a filter bank include hardware complexity, low power consumption and delay. A typical filter bank consists of analysis block, a processing unit and synthesis block. The analysis block splits the input signal into sub-bands. The sub-bands go through the processing unit and then the synthesis block retrieves the original signal at the end. The spectral transfer functions for digital audio signals are discussed by Vaidyanathan (1990). Several methods to design, Finite Impulse Response (FIR) filters and new sampling techniques for compressing the signals are discussed by Vaidyanathan (1990). The Analysis-Synthesis Filter Bank (ASFB) (Lollmann and Vary, 2008) provides minimum delay and less computational complexity than tree-structured filter bank (Gulzow *et al*., 2003). The filter bank for hearing aid devices is classified as uniform filter bank (Brennan and Schneider, 1998; Li *et al*., 2002; Dimitrov *et al*., 2001; Vaidyanathan, 1987; Lee and Yang, 2003; Jairaj and Subbaraman, 2010) and non-uniform filter bank (Kok *et al*., 2008; Karmakar *et al*., 2007; Yatsymirskyy and Stokfiszewsk, 2012; Jayawardena, 2003; Lian and Wei, 2005) as shown in Fig. 1. If the sub-bands are equally spaced and so it is called as a uniform filter bank. The uniform filter bank is subdivided into Quadrature Mirror Filter bank (QMF), Orthogonal Filter Bank (OFB) and Biorthogonal Filter Bank (BFB). A 32-band filter bank with the Discrete Fourier Transform (DFT) is designed by Brennan and Schneider (1998) and an eight-band filter bank using Finite Impulse Response (FIR) is described by Li *et al*. (2002) and Dimitrov *et al*. (2001). An iterative algorithm is discussed to design a lattice two-channel Perfect Reconstructions Quadrature Mirror Filter bank (PRQMF) by Vaidyanathan (1987). Though the hardware complexity is high, the hearing loss is compensated adequately in orthogonal filter bank (Karmakar *et al*., 2007). In the orthogonal filter bank, the prototype filter is a linear phase FIR filter and the order of the filter is equal to the filter bank delay. For the biorthogonal filter bank, the prototype filter is non-linear phase FIR filter bank and the delay of the filter

Corresponding Author: N. Subbulakshmi, Department of ECE, Sri Ramakrishna Engineering College, Coimbatore, India

Table 1: Uniform filters characteristics

Filter bank type	Phase, filter order	Number of unknowns	Filter bank delay	Perfect reconstruction
QMF	Linear phase, odd	$(N_0+1)/2$	N_0	NPR
	Non-linear phase, odd	N_0+1	$<N_0$	
Orthogonal	Non-linear phase, odd	N_0+1	N_0	PR or NPR
	Linear phase, odd-odd	$(N_0+N_1)/2+1$		
	Linear phase, even-even	$(N_0+N_1)/2+2$	$(N_0+N_1)/2$	
Biorthogonal	Non-linear phase, odd-odd, Even-even	$(N_0+N_1)+2$	$<(N_0+N_1)/2$	PR or NPR

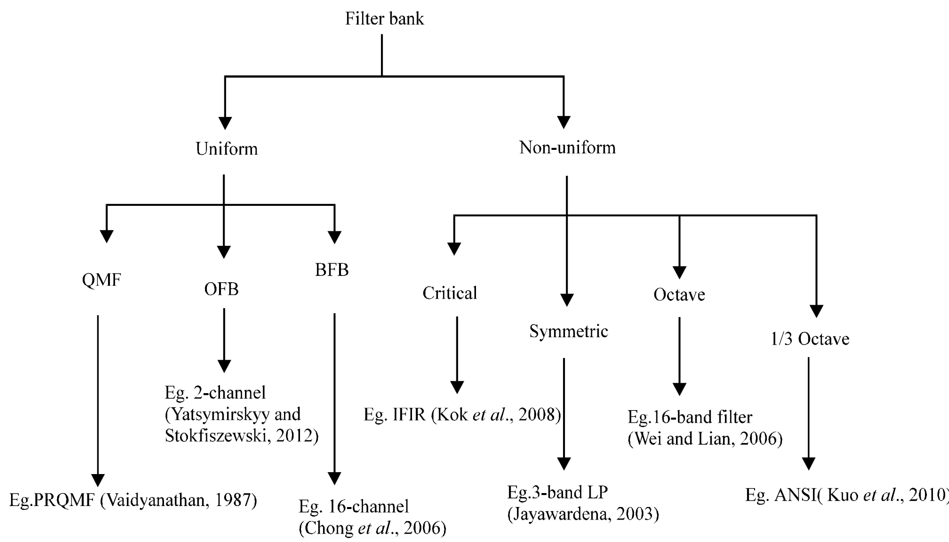

Fig. 1: Classification of filter bank

bank is less than that of the prototype filter order by Jayawardena (2003). The characteristics of the uniform filters are described in Table 1. N_0 and N_1 are the lengths of the filter. The linear and non-linear phase filter design depends on the properties of Perfectly Reconstruction (PR) and Non-Perfectly Reconstruction (NPR).

Non-uniform filter banks are categorized into octave bands (Lian and Wei, 2005; Lunner and Hellgren, 1991; Nielsen and Sparso, 1999), symmetric band (Wei and Lian, 2006, 2013), critical band (Chong *et al*., 2006) and one-third octave band (Davis, 1986; Kuo *et al*., 2010; Liu *et al*., 2013; Lozano and Carlosena, 2003) filter banks. A computationally efficient non-uniform digital FIR filter bank is proposed by Lian and Wei (2005). A 7 band octave band filter bank is discussed by Lunner and Hellgren (1991) and Nielsen and Sparso (1999) which use Interpolated Finite Impulse Response (IFIR). The symmetric band with a high-frequency resolution is presented by Wei and Lian (2006) and implemented in 0.35 um CMOS technology with power 245.5 μW. A 16-channel critical band filter bank for hearing aid devices is described by Chong *et al*. (2006). The proposed filter bank by Wei and Lian (2006) has a Pre-Computational Unit (PCU) that calculates the intermediate values and shares the values to all 16 channels. ANSI S1.11 octave band filter bank is used in many audio signal processing applications (Davis, 1986; Kuo *et al*., 2010; Liu *et al*., 2013; Lozano and Carlosena, 2003). Due to the high computational complexity, the ANSI filter bank is rarely chosen for hearing aid. It is adopted for hearing aid application for better matching capability with human hearing characteristics. A Quasi ANSI filter bank based on one-third octave filter co-efficient optimization algorithm is proposed by Liu *et al*. (2013) and the filter bank is implemented on 90 nm CMOS Technology. The computational complexity is reasonably reduced and it achieves 9 msec delay and 73 μW power consumption. The design of variable band edge FIR filters with the sharp transition band is proposed by Yu *et al*. (2009). The construction of the variable filter is formed from a fixed Fast Fourier (FF) filter bank. The filter structure is designed by shifting the signals in the frequency domain. Fixed filters with Frequency Response Masking (FRM) are applied to achieve low computational complexity when the transition band of the signals is sharp. The discussion by Yu *et al*. (2009), Subbulakshmi and Manimegalai (2014) and Gulzow *et al*. (1998) gives different ideas to design filter banks with less complexity and low delay. Designs of several filter banks to implement the digital hearing aids are discussed by Subbulakshmi and Manimegalai (2014), Gulzow *et al*. (1998) and Vetterli (1986).

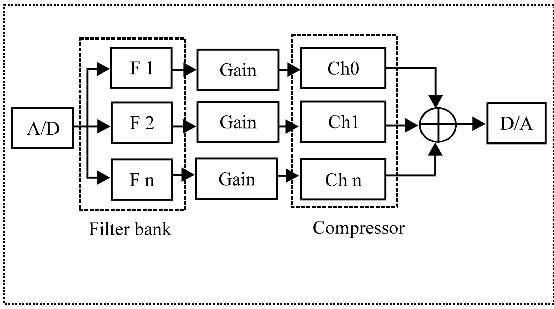

Fig. 2: A typical hearing aid

A typical hearing aid is shown in Fig. 2. The speech signal is converted into a digital signal for processing. Then it is divided into frequency sub-bands. Then each band is multiplied by the corresponding gain and passed through the compressor. Finally, the signal is again converted into analog form at the output. The sub-band coding is also another application of filter bank for audio signal processing. The principle of sub-band coding is presented by Jayant and Noll (1984). Foremost, the input signal is decomposed into several sub-bands. Then each sub-band is decimated by a factor and allocated bits for samples. The reconstruction of the original signal is carried out by the interpolation factor. Every sub-band is quantized independently using Adaptive Pulse Code Modulation (APCM) and Adaptive Delta Pulse Code Modulation (ADPCM). The poly-phase decomposition is the fundamental concept to design multi-rate filter bank. Real-time implementation networks for decimation, interpolation, sampling rate alteration and uniform Discrete Fourier Transform are discussed by Bellanger *et al*. (1976). The polyphase network has been realized for many filter banks.

MATERIALS AND METHODS

Uniform filter bank

Quadrature mirror filter bank: Quadrature mirror filter bank is a combination of a high-pass filter and a low-pass filter which performs the operation of dividing the input signal into two sub-bands. Perfect reconstruction structure of two band QMF, the relation between PRQMF and theconcept of lossless design arediscussed by Vaidyanathan (1987). In order to perform the perfect reconstruction, new lattice structures are introduced. The filter bank design has an unconstrained weighted square problem which is solved by the proposed algorithm. The practical design rules of PRQMF filter relating to 3 characteristics such as number of lattice co-efficient, low-pass filters stop-band edge and the stop-band ripple magnitude are considered. The quantization of the lattice coefficients is represented as Canonic Signed Digit (CSD). This design is implemented in TMS 320E25 with delay 4.4 msec. The two channel linear phase QMF (Lee and Yang, 2003) is designed with IIR filters. The optimization problem is solved with the help of Karmarkar's algorithm by frequency sampling and iterative algorithms. The output of this QMF is a linear phase response and not a magnitude response. The study (Jairaj and Subbaraman, 2010) is discussed about the utilization of Xilinx signal generation for hardware implementation. Peak constrained least square QMF (Kok *et al*., 2008) is designed to minimize the least square error of the reconstruction response and the sub-band filter response.

Orthogonal and biorthogonal filter bank: An optimal 2 channel orthogonal cyclic filter bank using semidefinite programming is designed to avoid the convex formulation problem in the traditional filter design (Karmakar *et al*., 2007). The orthogonality parameters are represented in terms of the cyclic autocorrelation sequence of the filter impulse response to obtain the optimality criterion. The positive semidefinite property is used in the cyclic autocorrelation matrix to avoid the problem. The 2 channel orthogonal filter bank with lattice structuresis designed to reduce the computational time of the filters by Yatsymirskyy and Stokfiszewski (2012). Lattice factorization of 2 channel orthogonal filter bank is derived which is used to extend the general biorthogonal filter banks. The 3 band linear phase biorthogonal wavelet filter bank is designed by Jayawardena (2003) Scaling filters are designed initially with the linear phase constraint. These linear phase wavelet filters are derived from 2 band factorization techniques. In order to find the reconstruction errors, the most familiar properties of orthogonal transform are usedin many applications. The reconstruction errors are obtained as the sum of sub-band distortions. Bi-orthogonal filter banks using rate distortion algorithm is used in.

MDLNS filter bank: Multi-Dimensional Logarithmic Number System (MDLNS) is designed with FIR filter by Brennan and Schneider (1998). It reduces the size of the number representation. It diminishes the hardware complexity using the logarithmic properties. The 1 and 2 digit MDLNS filter bank are designed and implemented. The filtering process is done with the help of linear and non-linear implementation. The design mainly concentrates on the construction of the FIR filter bank. The number of channels required by the MDLNS processor is equal to the number of coefficient digits multiplied by the number of data digits. The Greedy algorithm is used to reduce the relative magnitude of the second digit for a two digit system. In 2 digit implementation, the size of the lookup table ROM is decreased when compared to the single digit implementation. The MDLNS is implemented on 0.18 μm CMOS technology. The test chip components areused to test the filter bank are: MDLNS block-1883 cells, binary to 2-DLNS block-762 cells, Input block: serial to paralle l-128 cells and Output block: parallel to serial block-69 cells. The test portion of the filter bank is 550×1100 μm^2.

RESULTS AND DISCUSSION

Non-uniform filter bank

Interpolated FIR: Interpolated half band linear phase complementary FIR filter bank is realized by Lunner and Hellgren (1991). Prototype filter specifications are used to decide the number of bands in a filter bank. Arbitrary magnitude response, linear phase response, the size of the system to fit into a canal aid and low power consumption are idealised properties to specify the proposed design. The arbitrary magnitude response is approximated with piecewise constant function which is realized by a filter bank with M narrow bands. Linear phase is achieved by the linear phase filters. Further, the size of the system is designed using application specific integrated circuits. The asynchronous filter bank is one of famous important designs in audio applications. The Interpolated FIR (IFIR) method discusses the asynchronous low power design by Nielsen and Sparso (1999). The IFIR filter bank is difficult to convey some of the characteristics of asynchronous design, stillit introduces hearing filter bank algorithm. In order to consume low power, the multiplications are reduced. In IFIR filter bank, most of the coefficients are zero and the non-zero coefficients are considered as symmetric at mid-point. The bit serial arithmetic units used in the time domain and switching activity in both data path and the sampled audio signals are also discussed. This design is implemented on 0.7 μm CMOS technology with power consumption 85 μW.

Multi-rate filter bank: Complexity-effective multi-rate filter bank algorithm with a systematic co-efficient design flow is discussed. An 18 band ANSI S1.11 filter bank (one-third octave) is implemented with the recursive structure to diminish the complexity of hearing aids by Kuo *et al.* (2010). The 18-band filter bank consists of 6 octaves. Each octave has three sub-bands. Every nth octave is down sampled by 2^{n-1} where n is the number of iterations. So, there is no down-sampling for the 1st iteration, during which the 1st octave frequencies are generated at the end of the output. It repeats till the 6th octave frequencies are obtained at the output. The filter bank is implemented in 0.13 um CMOS technology. The foremost demerit of this method is that the group delay is large. ANSI S1.11 filter bank discusses about the characteristics of a spectrum analyzer for low frequency signals by Lozano and Carlosena (2003). These signals depend upon the sub-bands which are logarithmically distributed in octaves. The acoustic analyzer is designed and implemented in DSP. A multi-rate architecture is proposed to implement ANSI S1.11 standard filter bank with FIR filters for digital hearing AIDS by Kuo *et al.* (2007). It is implemented in MATLAB (7.2) with sampling rate 24 kHz. The number of computationsis reduced with the multi-rate processing technique. A systematic flow for optimizing the filter co-efficient is described which also minimizes the filter order significantly. It satisfies the linear-phase property and has less computational cost than Infinite Impulse Response (IIR) filter bank. In order to reduce the complexity of auditory compensation, the FIR based design of one-third octave filter bank is proposed by Kuo *et al.* (2008). This method increases the bandwidth of each sub-band. The structure has an analysis filter bank with ANSI S1.11 and synthesis filter bank with dynamic range compressor.

Reconfigurable filter bank: Filter banks are designed with fixed sub-bands in general. The filter bank with fixed sub-bands cannot be adopted for the people who suffer from their own specific hearing loss. But the design of reconfigurable filter bank can be customized for all the hearing problems. In order to produce a range of sub bands, the control parameters are varied without affecting the structure of the filter bank system by Wei and Liu (2013). This method focuses on the improvement of the hearing ability. This filter bank performs operations such as interpolation, decimation and frequency response masking. Realization of the entire system holds only three prototype filters to reduce the complexity. The reconfigurable filter bank consists of 2 blocks, namely, multi-band generation block and sub-band selection block. The multi-band generation block produces magnitude responses with multiple sub-bands. The sub-band selection block extracts the desired bands at the end. The main drawback of the design is relatively high delay. A reconfigurable non-uniform filter bank with Variable Bandwidth Filter (VBF) is proposed for hearing aid applications. VBF is designed by combining two arbitrary sample rate converters with fixed bandwidth FIR. In the realization of the VBF, the sample rate and bandwidth are utilized without changing the values of co-efficient. The advantage of this method is that the bandwidth can be changed by controlling the bandwidth ratio and frequency shift. The reusability of the design is improved using a reconfigurable filter bank.

Adjustable filter bank: Three prototype filters are combined to realize the adjustable filter bank structure by Wei and Liu (2011). It reduces the complexity in accordance with the frequency response masking technique. The adjustable filter bank structure has 4 stages. The prototype filters are decimated and then interpolated in the 1st stage. In the 2nd stage, masking filters are used to expand the input signals obtained from the 1st stage. Further, according to the frequency ranges the sub-bands are divided into 3 groups. At the final stage, sub-bands in each group are selected based on the selection signals of the multiplexer.

Warped filter: A warped filter structure is formed by the Nth order prototype filter (Darak *et al*., 2013). The frequency response masking technique (Lim, 1986; Shen and Lim, 2011) and co-efficient decimation technique is adopted for the design of the warped filter bank. The Computationally efficient variable band-pass digital filter is proposed by Darak *et al*. (2013). Warped-FIR with a co-efficient decimation technique is designed to reduce the gate count. In frequency response masking technique (Lim, 1986) a digital filter is replaced by a unit delay whereas in the co-efficient decimation technique, low complexity variable filter with fixed co-efficient is used to realize the structure. All pass transformation is a typical technique to design the frequency warped filter banks. For audio signal processing applications, these filter banks use a lower number of frequency channels than the uniform filter banks. An unequal bandwidth spectrum analysis technique with warped frequency is discussed by Braccini and Oppenheim (1974). A variable filter bank is proposed by Ito and Deng (2010) to implement digital hearing aids. In order to optimize the parameters in all-pass filter design, digital transformation is done. This filter is implemented in 0.18 μm CMOS technology. It consumes less power and requires a minimum number of multiplierswhen compared toa fixed filter bank. The spectral transformations are discussed by.

Other filter banks: Single Edge Triggered (SET) latches (Aezinia *et al*., 2006) are replaced by Dual Edge Triggered (DET) latches to reduce the power consumption by Das and Mahapatra (2008). Folded Direct Form (FDF) of 8-Tap filter structure is used. Multi-stage clock gating and stop glitch latch barriers are used to design the filter banks. In multi-stage clock gating, multiple clock gates are cascaded to minimize the useless toggling. Stop glitch latch barriers are connected in front of the multiplier because multipliers are more energy-hungry circuits in filter processing. The future work by Das and Mahapatra (2008) can be suggested to design 16, 32-tap, etc., to enhance the filter performance. Flavio *et al*., achieved 42% power reduction using a symmetric level sensitive clocking along with glitch aware registers by Carbognani *et al*. (2006).

Various parameters involved in designing a filter bank

Filter banks suitable for noise reduction: Noise Reduction is used to improve the Signal to Noise-Ratio (SNR) of the output signals and it enhances the speech quality over various background noises. The zone-of-quiet approach is proposed by Serizel *et al*. (2012). It concentrates on speech enhancement in digital hearing aids and provides a method for noise reduction. The combined feedback algorithm and noise suppression in hearing aid are achieved by Prediction Error Method (PEM) by Spriet *et al*. (2007). The speech distortion is avoided at low computational cost using this method. A typical integrated Active Noise Control (ANC) and Noise Reduction (NR) techniques are introduced by Marin-Hurtado *et al*. (2012) and Klasen *et al*. (2005). Different multiple-microphone noise reduction techniques are proposed by Spriet *et al*. (2007). It describes a binaural noise reduction based on Multi-channel Weiner Filter (MWF) (Marin-Hurtado *et al*., 2012; Klasen *et al*., 2005; Doclo *et al*., 2005; Klasen *et al*., 2007) and Blind Source Separation (BSS) (Wehr *et al*., 2006; Aichner *et al*., 2007; Reindl *et al*., 2010) with low processing delay. Power Spectral Density (PSD) estimator is introduced for real-life complex acoustic environments by Kamkar-Parsi and Bouchard (2011). It produces a substantial reduction of various background noises when compared to several algorithms. A Singular Value Decomposition (SVD) based optimal filtering is proposed for noise reduction in dual microphone hearing aid by Maj *et al*. (2005).

Power aware filter banks: During FIR filtering, Multiply and Accumulate (MAC) data path involves maximum signal activity. The data memory is configured as a circular buffer to minimize the power dissipation by Mehendale *et al*. (1998). The measure of power dissipation in the multiplier mainly depends on the input values and these values are analysed by the transition density by Najm (1993). The transition density is the hamming distance (the probability of the number of ones existing in the inputs) between two input signals of the multiplier. This brings the measure of power dissipation in the multiplier block. Parallel processing and pipelining techniques are used for power reduction by Chandrasekaran and Broderson (1995) and the same is applied for linear phase implementation of FIR filters. It is not suitable for the design to have one processor

Table 2: Comparison of filter bank techniques

Types of filter bank	Classification of the filter bank	Algorithm used in the filter bank	Achieved results	Tools used
Digital filter bank (Brennan and Schnieder, 1998)	8-bands	Complementary interpolated linear-phase filter	Minimizes the number of multipliers	TMS320E25 Delay 4.4 msec
Multi-dimensional logarithmic number system (Li *et al*., 2002)	8-bands	Weighted overlap add DFT with two digit structure	Minimizes the size of the look up table	0.18um technology, 1883 cells
QMF Vaidyanathan (1987)	2-channel	Efficient least square algorithm	Minimizes the co-efficients	Simulated frequency responses in MATLAB
Orthogonal (Karmakar *et al*., 2007)	2-channel FIR	Semi definite programming scheme	Diminishes stop-band energy	MATLAB, 3GHz, Pentium
Computationally efficient FIR (Lian and Wei, 2007)	Non-uniform 8-bands	Frequency response masking with 2 half band FIR	Minimizes the number of multipliers	80 band stop band attenuation
Interpolated FIR (Nielsen and Sparso, 1999)	7-bands	Asynchronous circuit techniques	Power consumption	0.7 um CMOS technology power 85uW
16-channel critical like (Chong *et al*., 2006)	16-bands	Pre-computational unit	Complexity is less	0.35um technology area 1.62 mm^2 power 247.5 uW
ANSI (Davis, 1986)	18-bands	Multi-rate filter bank algorithm	Minimizes power and complexity	TSMC 0.13 um CMOS technology power 87 uW
Quasi Liu (2013)	18-bands	Filter order optimization algorithm	Less complexity	90 nm CMOS technology power 73 uW delay 10 msec
ANSI S1.11 (Kuo, 2007)	18-bands	Multirate IIR	96% of multiplications can be reduced compared to parallel filter bank	MATLAB (Version 7.2) sampling rate 24 kHz
Band edge filter (Yu *et al*., 2009)	Variable	Fast fourier transform with half band filter	Low computational complexity	MATLAB, 3-GHz
Reconfigurable filter (Wei and Liu, 2003)	Variable filter bank	Sound decomposition methods	Complexity is less	-
Adjustable filter (Elias and George, 2014)	Variable filter bank	Sub-band distribution methods	Improves sound quality	-
Reconfigurable warped filter bank (Wei and Liu, 2011)	Variable	Warped filters with co-efficient decimation technique	Reduction in gate count and power	Xilinx vertex 4vsx35
Variable band pass filter with all-pass transformation (Ito and Deng, 2010)	Variable	Warped FIR with coefficient decimation	Gate count is reduced	TSMC 0.18 um CMOS technology
(Mandarin chip Wei *et al*., 2010)	18-bands	Wide dynamic range compression technique	Complexity is less	90 nm CMOS technology 314uW@ sampling rate 24Khz

while the power reduction is achieved using multiple processors. Selective coefficient negation technique reduces the co-efficient input values of the multiplier by Samueli (1989). The Mandarin specific auditory compensation algorithm is introduced by Wei *et al*. (2010). The hearing aid device consists of the filter bank block, insertion gain block wide range dynamic compressor and noise reduction circuitry. Logarithms and divisions are adopted for complicated mathematical operations. Mitchell's algorithm is used to simplify the logarithmic calculations. The signal quality is improved in this filter bank using voltage activity detection. For achieving low power multi-clock domain with clocking and handshake strategies by pass mode which decides the direction of the signal flow and voltage scaling are adopted. The power consumption of the filter bank is 314 μW at sampling rate 24 kHz. It is implemented in 90 nm CMOS technology.

Filter banks with low delay: Warped Discrete Fourier Transform (WDFT) method is designed for a filter bank with minimum delay by Franz *et al*. (2002). Unlike DFT, the frequency points of WDFT are non-uniformly spaced on the unit circle. The sub-band center frequencies are shifted and bandwidth remains the same during filter processing. Filter Bank Summation Method (FBSM) is derived by Crochiere and Rabiner (1983) to achieve low signal delay. But the drawback of this filter bank is high computational complexity. Further, low delay non-uniform filter banks are discussed by Deng *et al*. (2007) and Dumitrescu *et al*. (2006). Uniform and non-uniform filter banks with low delay are designed using lifting scheme, which proposes 2nd generation wavelets. The lifting steps and inverse lifting steps are applied at the analysis bank and the synthesis bank, respectively. The lifting scheme is used to all-pass transformed filterbanks. The distortions due to frequency warping are eliminatedby increasing the stop band attenuation of the sub-band filters. The degree of the filter is increased with low signal delay in the filter bank. Further, addition of the lifting steps does not change the performance enhancement in the stop band attenuation. Hence, only limited improvement of stop band attenuation is achieved with aliasing cancellation (Table 2).

CONCLUSION

This study presents a comprehensive survey on filter bank design and algorithms. The multi-rate filter bank is well suited for digital hearing aid. The co-efficient decimation technique is another important issue in the design of a filter bank. The summary of various filter bank techniques based on parameters such as type, classification, algorithms, etc.

In this study, various filter bank techniques are reviewed based on the following aspects:

- Algorithms used for design
- Number of sub-bands
- Various performance metrics such as area, power, delay and noise
- Simulation tools used to implement the filter bank design

Most of the algorithms try to diminish hardware complexity to improvethe system speed. Noise reduction is obtained by Active Noise Control (ANC). The reduction in hardware complexity is achieved using Frequency Response Masking as discussed in most of the papers. Lifting scheme is well suitablefor less number of lifting steps. It also produces minimum distortions in the signal. To optimize the power consumption, multi-clock, bypass mode, voltage scaling methods are used.

The filter bank design techniquesavailable in the literature discuss the following issues: delay, powerconsumption, computational complexity and quality of the signal. Few filter bank algorithms focus on the noise reduction. Implementing the filter bank techniques (Brennan and Schneider, 1998; Li *et al*., 2002; Nielsen and Sparso, 1999; Chong *et al*., 2006; Liu *et al*., 2013; Wei and Liu, 2011; Ito and Deng, 2010; Wei *et al*., 2010) in real-time and estimating the efficiency of the filter bank is an open issue. Based on the FPGA implementation of the filter bank techniques, we observe that the Interpolated FIR (Nielsen and Sparso, 1999) filter bank consumes 85 μW power with seven sub-bands and ANSI (Davis, 1986) filter bank minimizes the power consumption and complexity. Gate count is reduced in variable filter bank (Ito and Deng, 2010) using TSMC 0.18 μm CMOS technology. Moreover, Mandarin chip consumes 314 μW power using 90 nm CMOS technology with less complexity. The Quasi ANSI (Liu *et al*., 2013) filter bank consumes 73 μW power with minimum delay of 10 msec. It has minimum delay compared to other filter bank algorithms. Thus, the Quasi ANSI filter bank is well suitable for the hearing aid applications.

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