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A Low Offset Low Power Dynamic Comparator for High-Speed Applications in 65 nm Technology

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Abstract: The study presents a design of low noise, stacking reduction, low power and low voltage double tail comparator for high speed application. The comparator design occupies less area and is suitable for the input stage of a Flash ADC. The dynamic comparator proposed in this project not only eliminates the stacking issue related with the convential comparator but reduces the offset noise further. The need for low noise, low-power, area efficient and high speed flash adcs required in many application today made the work to progress in designing a comparator for analog-to-digital converter. In this study, the analysis and design of new dynamic comparator is proposed where the circuit of a conventional doubletail comparator is modified. The regenerative feedback is strengthened to reduce the delay time.The rail to rail output swing is also improved by 99% of V_{DD}. The simulation results in a 65 nm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator is increased to 2.2 and 3.5 GHz at supply voltages of 0.6 and 1 V. The simulation is carried out using predictive technology model for 65 nm in HSPICE.

Key words: Double-tail comparator, dynamic clocked comparator, CMOS technology, Flash ADC, HSPICE, simulation

INTRODUCTION

The objective of the research is to design a dynamic comparator for the flash ADC used in system on chip application. With respect to the objective different comparators are surveyed and based on the survey four important comparators are chosen for analysis and modification. The comparators are implemented using HSPICE Software and the outputs are observed. The average power and peak power is estimated for its efficiency. In literature several comparators are designed and utilized. Scott *et al*. (1986) in their research proposed a enhanced sign comparator plan with a pull-up/pull-down lock in a 3.5 μm twin-tub CMOS process. A Josephson latching dynamic comparator for use in a high-speed analog-to-digital converter is proposed by Petersen *et al*. (1987). The comparator is utilized to quantize quickly changing data waveforms. A double representation of a simple data method was the design for which the comparator is proposed. McCarroll *et al*. (1988) proposed a high-speed CMOS comparator for analog-to-digital converter with offset cancelled intensifier. Wang *et al*. (1998) a 1 GHz 64 bit high-speed comparator using ANT dynamic logic with two-phase clocking scheme is displayed. The 64 bit comparator is build by organizing the 2 bit comparator of 16 numbers. The correct result takes 3.5 cycles to reach the output. An input refereed noise reduction technique for high speed CMOS comparators is been proposed by Bruccoleri and Cusinato (1996). A similar Offset fluctuation cancellation technique is been proposed by Kotani *et al*. (1998). Boni *et al*. (1998) proposed a 3.3 V, 200-Ms/s BiCMOS comparator for current-mode interpolation using a transconductance stage. The comparator is designed using 180 nm technology. A priority encoder based high-performance and power-efficient cmos comparator was proposed by Huang and Wang (2003). The design features a multiple output domino logic. A Post-format recreation results were reported in the research demonstrates that a 64 b comparator outlined with the proposed procedures in a 3 V, 0.6 μm CMOS innovation is 16% quicker, half littler and 79% more power proficient.

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Jung *et al.* (2011) proposed a low-power and low-balance hooked comparator utilizing dynamic balance cancelation and a lock burden. In most of the ADCs the Offset values are so, troublesome which needs a comparator of less offset. For a 7 bit, 1.4 GS/s ADC Nakajima *et al.* (2013) proposed a offset drift suppression technique. The ratio between the transconductance and drain current is kept constant to suppress the offset drift. Yin *et al.* (1992) proposed a fast CMOS comparator comprising of a differential data stage, two regenerative flip-failures and a S-R lock. The reported design works under a+2.5 and -2.5 V control supply, performs 8 bit correlation with a symmetrical data dynamic scope of 2.5 V. A bulk driven based dynamic comparator is been proposed by Zhu *et al.* (2014) which reduces the threshold voltage. The comparator is designed using a preamplifier and latch. The problem with the design is the proper transistor sizing is required else it will lead to offset errors in the input stage. Babayan-Mashhadi and Lotfi (2014) have proposed a low-voltage low-power double-tail comparator utilizing the regenerative principle and current boosting. The researchers investigated the comparator delay and the tradeoffs in element comparator outline. In addition, the study proposes a traditional doubletail comparator for low-power and quick operation even in little supply voltages. The reported post-format reproduction results in a 0.18 μm CMOS innovation affirm the examination results. A switched dynamic comparator is proposed by Xu *et al.* (2014) which eliminates the limitation on the maximum operating speed due to regeneration time. The design consists of a dynamic amplification stage with a NAND gate for switching operation. Only one extra transistor is used in this proposed design.

The corruption of input signal by large kickback noise is addressed by Amico *et al.* (2014). The increase in the size of transistors will reduce the kickback noise but increases the large parasitic capacitances. The proposed double tail comparator presents a fixed bias current in the first stage eliminating the kickback noise. Zeller *et al.* (2014) proposed a dynamic latched comparator with complementary input stage for large input common-mode range and short decision time at small differential input voltages. The research reported presents that there are no static currents and all internal nodes are discharged during the low clock phase to avoid offset that depends on previous decisions. Xu *et al.* (2015) proposed an element comparator which works in lower voltage and rapid low-power.

Dynamic comparator: The dynamic latch comparator circuit is been widely used as a sense amplifier in dynamic RAM's and ADCs. The comparator is normally implemented using CMOS technology. The comparator is used in circuits where speed requirement are higher. But the mismatches between the transistors and circuit parameter deviations leads to large input offset current. The large input offset current limits the resolution. The offset voltage can be overcome by preceding the dynamic latch using linear amplifier. This can increase the feasibility of medium resolution comparators. The offset can be reduced by designing the comparator with differential input stage. This study discusses the detailed analysis of 4 existing comparators. The dynamic behavior of the CMOS latch is presented and a technique to reduce the input-referred offset is proposed.

The on chip ADCs for the SOC are designed to provide high speed operation. For high speed operation the choice is on flash ADC and the comparator is the most important component. In recent times the clocked regenerative comparators were used in applications due to their fast decisions behavior. The circuits have high input impedance, sufficient rail-to-rail output swing and no static power consumption. In recent years, several dynamic comparators have been widely employed in ADCs offer high operating speed while consuming no static power. The structure of conventional dynamic comparator is shown in Fig. 1.

The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, the output nodes Outn and Outp are pulled to VDD by the reset transistors (M7-8) which will define the initial condition. The reset transistors determine the valid logical level during reset. During comparison phase when CLK = V_{DD}, Mtail is ON and transistors M7 and M8 are off. Based on the input values (INN/INP) the precharged Output voltages (Outp, Outn), start to discharge with different discharging rates. When VINP>VINN, Outp discharges faster than Outn and If VINP<VINN, the circuits works vice versa. The circuit suffers from parasitic capacitances of input transistors which can be eliminated by designing large transistors for the input stage. The other tradeoff is the need of high supply voltage due to several stacked transistors. The circuit also suffers from only one current path. The draw backs can be rectified by the double tail comparator shown in Fig. 1.

The double-tail dynamic comparator topology has less stacking and therefore can operate at lower supply voltages compared to the dynamic comparator given in Fig. 2. The double tail enables both a large current in the latching stage and wider Mtail2 for fast latching independent of the input common-mode voltage (Vcm) and a small current in the input stage (small Mtail1) for

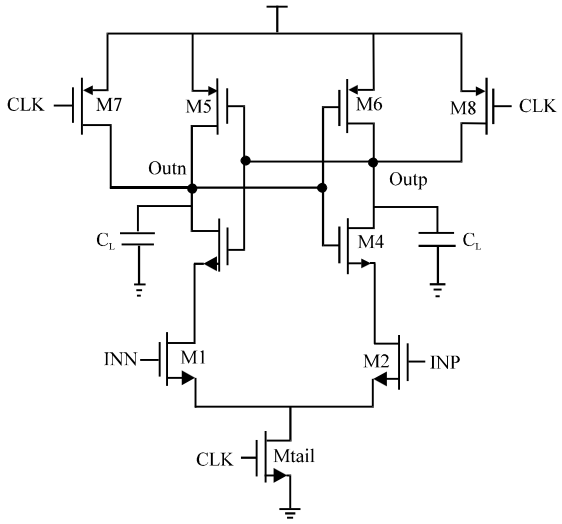

Fig. 1: Schematic diagram of the conventional dynamic comparator

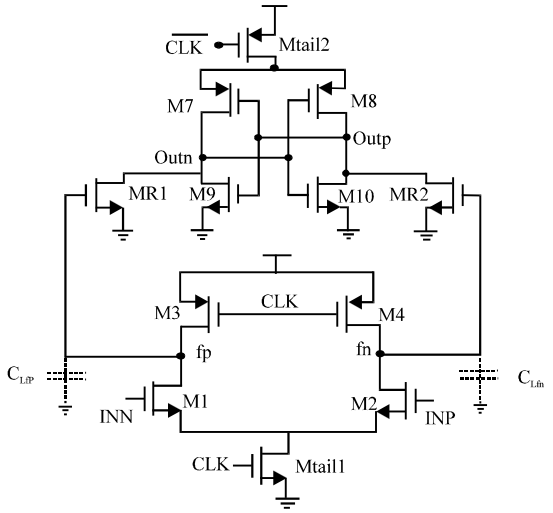

Fig. 2: Schematic diagram of the conventional double tail dynamic comparator

low offset. The operation of this comparator in Fig. 2 is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to V_{DD} which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = V_{DD}, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by $Im_{tail}1/Cfn$ (p) and on top of this an input-dependent differential voltage Δvfn (p) will build up. The intermediate stage formed by MR1 and MR2 passes Δvfn (p) to the crosscoupled inverters and also provides a good shielding between input and output,

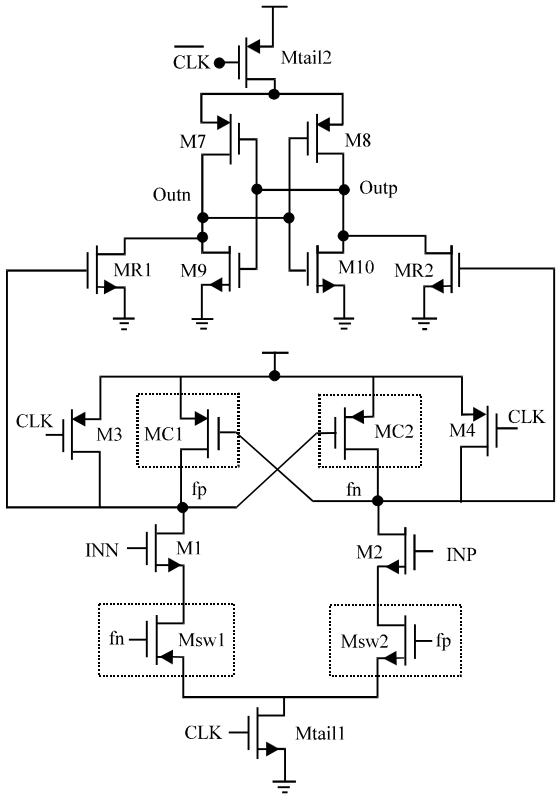

Fig. 3: Schematic diagram of the modified double tail dynamic comparator structure

resulting in reduced value of kickback noise. The circuit suffers from few disadvantages they are delay issues and power consumption. Sufficient output voltages at stage one is required to reduce the delay and power consumption. To eliminate this draw back two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner. This configuration increases the ΔVfn/fp by which the latch regeneration speed increases as shown in Fig. 3.

So from the analysis, it can be found that the circuits given in Fig. 1-3 eventhough, provide high input impedence, rail to rail output swing and less stacking the speed of operation is limited. So in this research, the circuit shown in Fig. 4 is adopted for modification. A high speed low power dynamic comparator is illustrated in Fig. 4. The inverter input structure boosts the input common mode voltage. The input referred noise is reduced by keeping the transistors M3 and 4 in saturation state through CLK 2 which is the delayed version of CLK 1. (CLK 1 = 1 and CLK 2 = 0). Transistors M7 and 8 accelerate the latch.

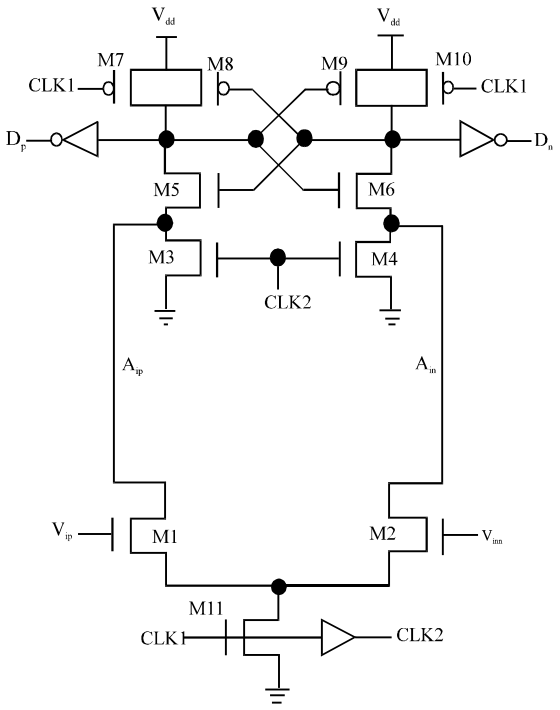

Fig. 4: High-speed low-power dynamic comparator

MATERIALS AND METHODS

A new dynamic comparator is proposed with low power, low supply voltage, low offset and low power consumption. The time sequence is adjusted using two different clocks by which the comparison speed is increased. The proposed circuit is given in Fig. 5. The proposed dynamic comparator with reduces the stacking issues and it contains a constant gm/Id biasing. The circuit in Fig. 4 is modified with a double tail latch to reduce the number of stacked transistors. During the reset phase (CLK = 0), M6-M9 pre-charge the D_i nodes to supply voltage V_{DD}. As a result, M6 discharge the X_I nodes to ground. After the reset phase, CLK turns to V_{DD}, M6-M9 turn off and M10 turns on. At the D_I nodes, the common-mode voltage drops with a rate determined by $I_{M3}/C_{Di}/C_{Di}$ is the load capacitance of the 1st stage) and an input dependent differential voltage ΔV_{DD} will build up in a short time. The proposed circuit has the additional tail transistor M3 and the bias circuit which keeps the I_{DI}/gm_I constant. This method successfully suppresses the environmental drift of V_{ORS}. A voltage buffer is placed between the drain of M4 and gate of M17 to drive

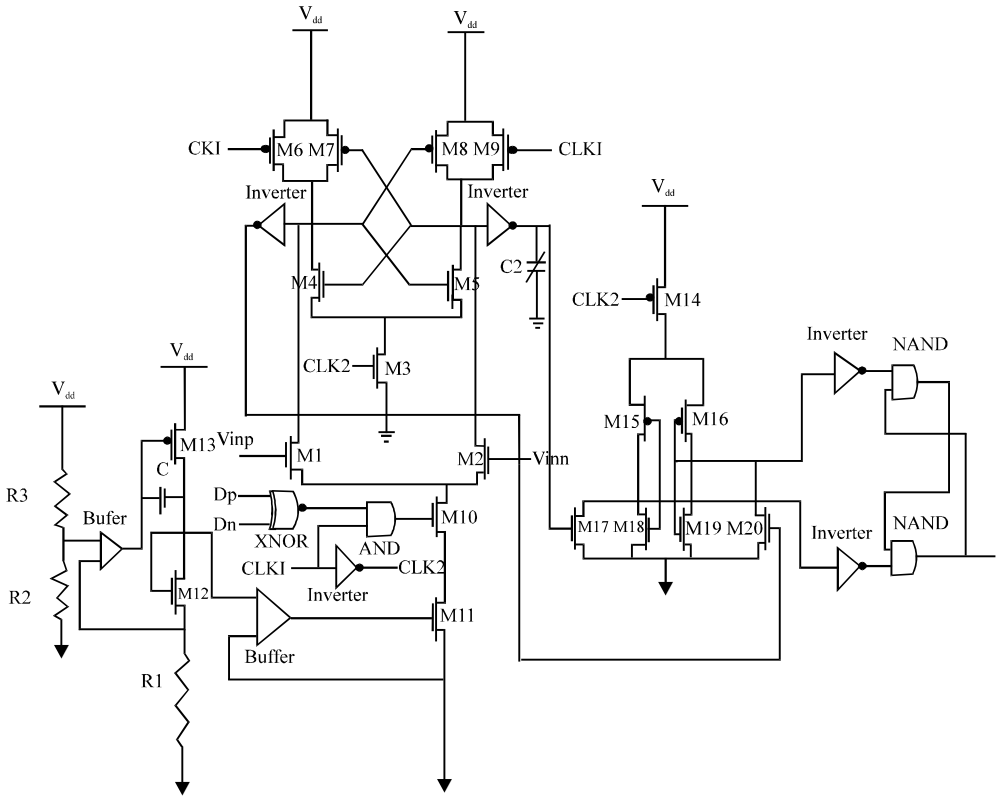

Fig. 5: Proposed high-speed low-power dynamic comparator

more drive comparators (8 bits). The buffer is designed using a differential unity gain circuit. Eventhough, the tail transistor M3 causes a slight degradation in the operation speed but through time sequence the speed is been increased. The sequence is done using a XNOR and AND gate. The CLK 1 and 2 become low voltage in reset phase. The voltages of Dip and Din make PMOS M7, M8 and NMOS M4, M5 to establish a positive feedback in the early period when CLK2 becomes high voltage. This behaviour would raise the speed of the comparator. M10 is turned off by the different voltages of Dp and Dn through the XNOR gate and the AND gate in the latch phase, this operational principle ensuring there is no static power consumption either in the reset or the latch phase compared with circuit in Fig. 3 and 4. The delay of CLK 2 compared with CLK 1 also ensures a low input-referred noise. So, the offset noise is removed by two ways one in the comparator block. Other due to constant gm/Id biasing. The double tail structure in addition reduces the stacking technique. As a result, it could achieve the required low supply voltage, low power, low offset and high speed.

RESULTS AND DISCUSSION

The circuits are implemented using predictive technology models in 65 nm technology using HSPICE. The conventional dynamic comparator shown in Fig. 1 is simulated using 9 transistors with the operating frequency of 40 MHz. The simulated circuit schematic is given in Fig. 6. Table 1 provides the performance of the conventional dynamic comparator.

The average power obtained was 29 μW while, the peak power is 191 μW. But the conventional dynamic comparator provides less noise immunity. The offset voltage is 43 mV and as frequency is increased above 40 MHz outputs are not obtained properly. The supply voltage is 1 V. The operating frequency is limited for the conventional dynamic comparator. The 40 MHz the performance reduces drastically. The implementation of the double tail comparator of Fig. 2 using 12 transistors is simulated. The simulated circuit schematic is given in Fig. 7. The stacking is avoided by the additional transistors. Table 2 provides the performance of the conventional double tail dynamic comparator.

The average power consumption is 0.9 mW and the peak power is 1.8 mW. The simulated schematic of the modified double tail comparator shown in Fig. 8 and the performance is given in Table 3.

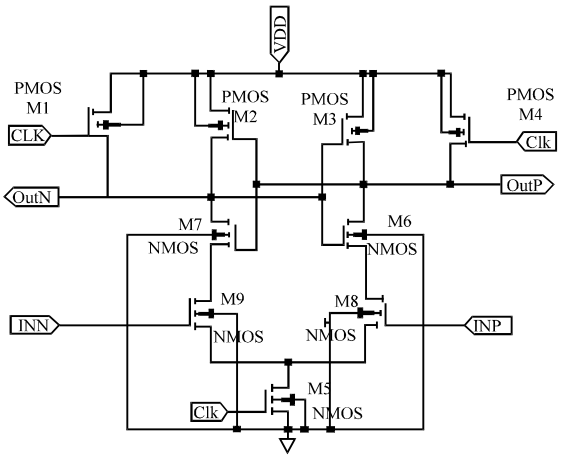

Fig. 6: Implementation diagram of the conventional dynamic comparator

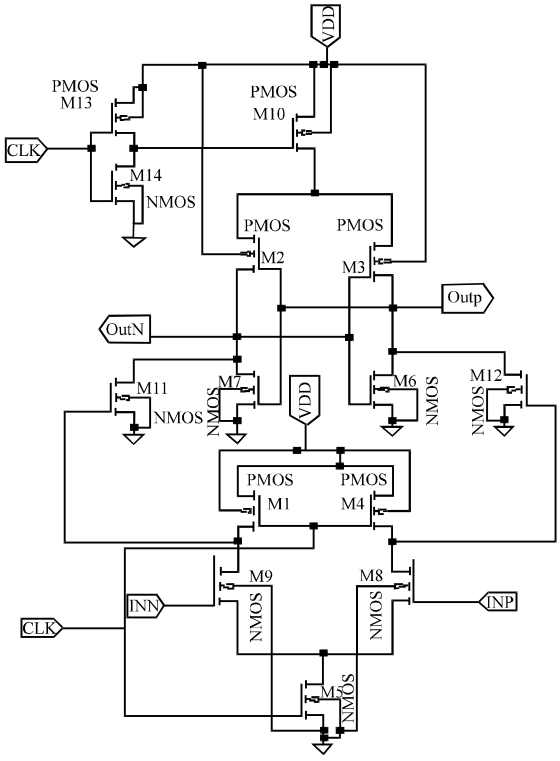

Fig. 7: Implementation diagram of the conventional double-tail dynamic comparator

The simulated schematic of the proposed high speed low power dynamic comparator is shown in Fig. 9. Table 4 provides the performance of the proposed high speed low power dynamic comparator. From Table 4, it can be observed that the voltage swing is about 99% with that of V_{DD}. The proposed circuits and the conventional circuits works in the supply voltage ranging from 0.8-1 V

Table 1: Performance of the conventional dynamic comparator

V+	V-	OUT+	OUT-
0.00	0	0.043594	0.043594
1.00	1	0.490040	0.490040
0.50	0	0.999790	0.055290
0.25	0	0.811820	0.035518
0.26	0	0.916790	0.031782

Table 2: Performance of the conventional double-tail dynamic comparator

V+	V-	OUT+	OUT-
0.00	0	0.050242	0.050242
1.00	1	0.999050	0.999330
0.50	0	0.999660	0.034177
0.20	0	0.81670	0.049634
0.21	0	0.96040	0.049823

Table 3: Performance of the Modified dynamic comparator structure

V+	V-	OUT+	OUT-
0.00	0	0.050385	0.050385
1.00	1	0.99985	0.996940
0.50	0	0.99929	0.042655
0.24	0	0.87767	0.050076
0.25	0	0.96285	0.049549

Table 4: Performance of the proposed high-speed low-power dynamic comparator

V+	V-	OUT+	OUT-
0.00	0	0.051385	0.050295
1.00	1	0.997850	0.995940
0.50	0	0.998290	0.042455
0.24	0	0.876670	0.050176
0.25	0	0.966850	0.049649

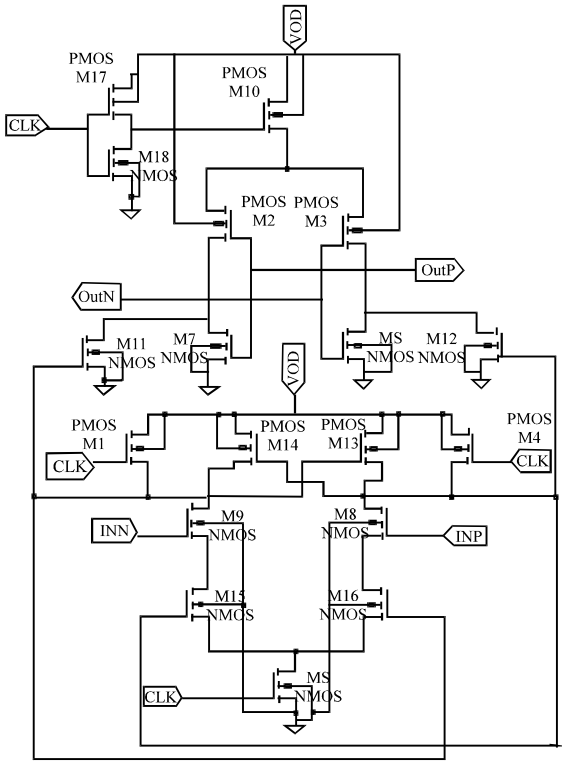

Fig. 8: Implementation diagram of the modified double tail dynamic comparator structure

Table 5: Performance of the proposed high-speed low-power dynamic comparator

N(V)	P(V)	Average power (mW)	Average current (mA)	Peak power (mW)
0.0	0.0	0.219	0.00373	16.90
0.3	0.0	0.218	0.00348	2.66
0.0	0.3	0.218	0.00240	15.10
0.7	0.0	0.219	0.00818	27.90
0.0	0.7	0.222	0.01260	2.40
1.0	0.0	0.219	0.02510	3.46
0.0	1.0	0.218	0.02920	10.40

Table 6: Performance of the proposed high-speed low-power dynamic comparator for clock = 2 Ghz

N(V)	P(V)	Average power (mW)	Average current (mA)	Peak power (mW)
0.0	0.0	6.87	6.61	19.80
0.3	0.0	6.87	6.64	8.37
0.0	0.3	6.86	6.59	19.20
0.7	0.0	6.86	6.59	11.10
0.0	0.7	6.87	6.58	18.80
1.0	0.0	6.86	6.65	8.75
0.0	1.0	6.86	6.63	9.94
1.0	1.0	6.86	6.58	11.70

to achieve the maximum output swing. Compared to the conventional methods eventhough the number of transistors is more the swing obtained is better. The required swing for a full load driving capacity is reached due to the dual rail introduced in the proposed design. Also the enviroimental drift is taken care by the tail transistors which keeps the I_{D1}/gm_{1} constant. The proposed high speed comparator shows an output voltage swing is about 99% of V_{DD} which is a 6% improvement in voltage swing when compared to the conventional methods. Additional transistors are consumed for the latching of the output stage at the right end which provides sufficient driving cutrrent to the subsequent stages. The inputs are varied for different voltage combination from 0-1 V and the outputs are obtained. Table 5 and 6 give the power and current consumption for the proposed comparator for clock frequency of 2 GHz used. The average and peak power is observed.

The operating frequency is upto 3.5 GHz the average and peak power is determined for the proposed circuit in both NAND gate mode and without NAND gate mode in 65 nm for various combinations of inputs. It can be noticed that, the difference in inputs will change the power. The power is reduced for the proposed method when compared to other method. The area also gets reduced. In the same way the average and peak current increases for the increase in operating frequency. From all the above analysis we can conclude that the proposed method has less area, low power and higher driving capacity.

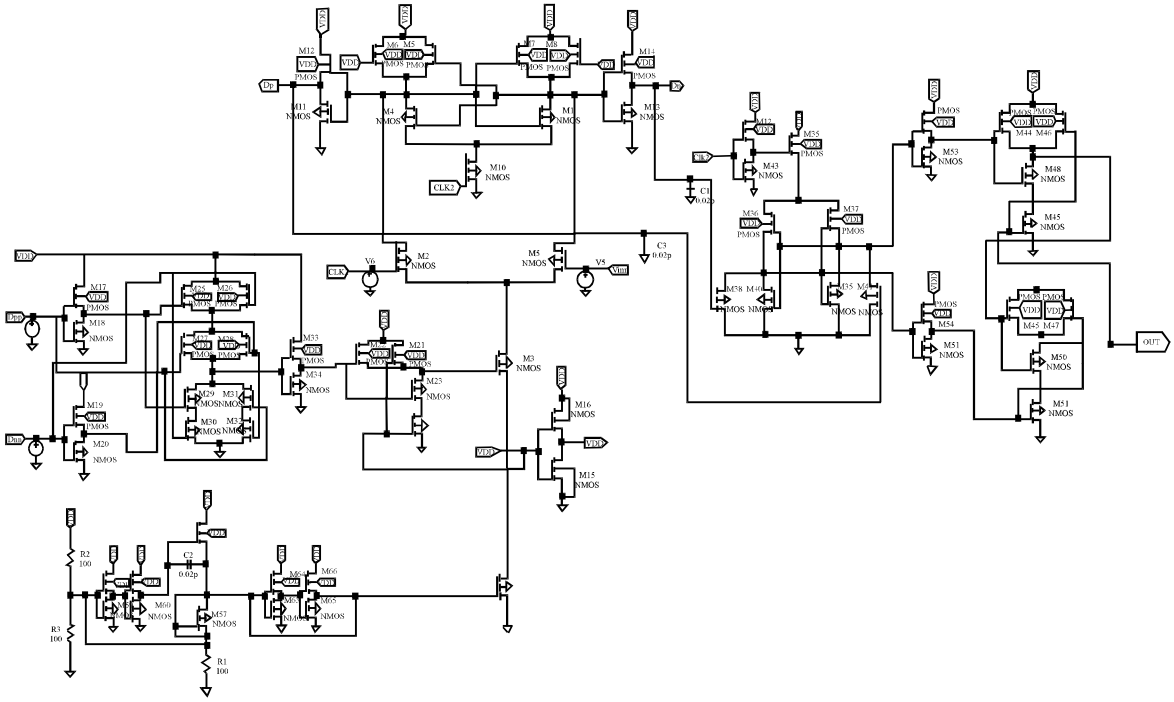

Fig. 9: Implementation of proposed high-speed low-power dynamic comparator

CONCLUSION

The design of low noise, stacking reduction, low power, low voltage double tail comparator for high speed application is presented in this study. The dynamic comparator proposed in this project not only eliminates the offset voltage in two levels but reduces the stacking issue related with the convential comparator. The regenerative feedback is strengthened to reduce the delay time through sequencing timing. The rail to rail output swing is also improved. The simulation results in a 65nm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 3.5 and 2.2 GHz at supply voltages of 1 and 0.6 V. The simulation is carried out using predictive technology model for 65 nm in HSPICE .

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