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Pulse Width Based CMOS Subcircuits for Voltage Mode Analog Neuron with 180 nm Technology

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Abstract: This study presents CMOS implementation of Voltage input to Pulse Converter (VPC) and activation function circuits in 180nm technology using PWM technique. The CMOS circuits are built with ±1.8 V supply. The circuits designed are reliably used in input or hidden layers of neural network. The pulsed output from VPC can be given as input to synapse multiplier along with activation function that uses PWM signals to compute. These subcircuits are of immense importance when an overall design goal is CMOS Multilayer Perceptron (MLP) design with PWM technique. The performance parameters are simulated and observed using cadence spectre Virtuoso 6.1.6 BSIM3v3.

Key words: Analog neuron, CMOS circuit, multilayer perceptron, pulsed neural network, PWM technique, input

INTRODUCTION

Analog, digital and mixed mode using current or voltage modes of operation are used to design artificial neurons. Analog pulsed neural network's capabilities are well used while implementing in VLSI. In pulsed neural network implementations, the state of neuron is a varying argument of pulse stream. In our case, it is thhe rate of fixed pulse width. In pulse width modulation techniques in voltage and current modes, significant contributions have been made (Murray *et al*., 1991; Bor and Wu, 1998; Chen and Shi, 2000; Takashi *et al*. 2000). Using a PWM signal to control the flow duration of a current, the total output charges are equal to multiplication of pulsewidth and current (Chen and Shi 2000, Mithila and Valsalam, 2015). For training and learning in neural networks, complete VLSI neural structure should be designed in CMOS.

Pulse-stream method of encoding has been found to be used in digital signal's activity that determines CMOS circuitry (Murray *et al*., 1991). Pulse bursts are produced by some neurons with defined intervals (Murray *et al*., 1991; Bor and Wu, 1998). Biologically, synaptic activity, cell morphology and electrical properties of membrane in the dendrite of neuron establish the behavior of the pulse (Reyneri, 1999). For the design of appropriate voltage mode CMOS neuron with Pulse Width Modulation (PWM) technique, it is required that we design an efficient circuit to convert voltage to pulse that maybe used in any layer of MLP (Bor and Wu, 1998; Mithilia and Valsalam, 2015).

The network design by Chen and Shi (2000) has been done using 0.8 μm technology with ±2.5 V supply. We have implemented the asynchronous design of two subcircuits for design of the pulsed neural network using 180nm technology with ±1.8V supply using cadence spectre Virtuoso 6.1.6 tool. With effective use of minimum aspect ratio values, the size of the circuit has been considerably reduced.

CMOS VPC circuit design:

Subcircuits-NAND and inverter design: The minimum aspect ratio values (S = W/L) are chosen and the circuitry design is done. The hand calculations are done with help of process and model parameters as described by BSIM3V3 manual and gpdk 180 process files used in cadence Virtuoso 6.1.6 (Cheng *et al*., 1996; Allen and Holberg, 2002). Using material and device parameters an opamp to meet the specifications has been designed where K^s is transconductance parameter, W is the channel width, L is the channel length, μ_0 is the mobility factor, C_{ox} is the oxide capacitance:

$$\text{Aspect ratio: } S = W/L$$

Chosen device length L = 1μm:

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$$\beta = K^{s}\frac{W}{L} \cong \mu o C_{Ox}\frac{W}{L}(A/V^{2}) \quad (1)$$

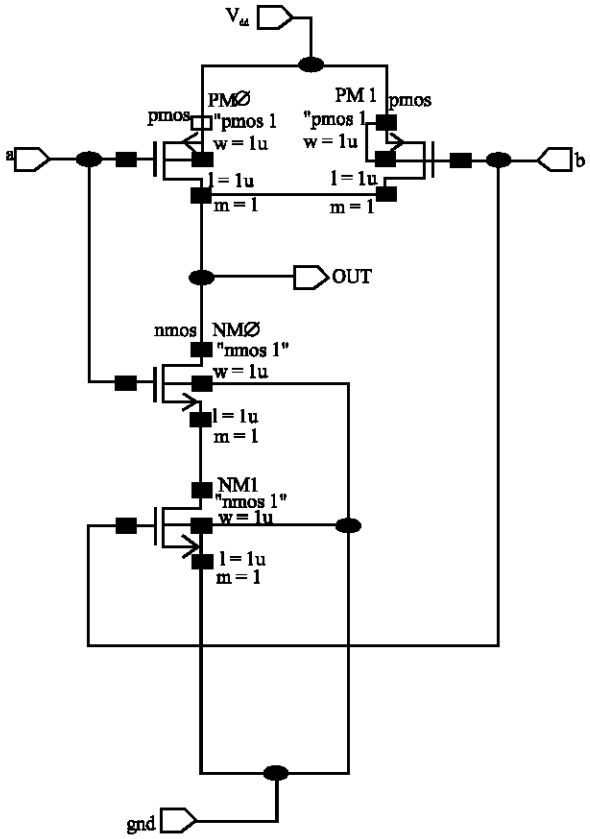

Fig. 1: CMOS NAND gate

The CMOS NAND gate is designed with two inputs 'a' and 'b' as seen in Fig. 1. Its output is verified as observed in Fig. 2. Similarly, Inverter gate is designed and its operation is also verified using Cadence Spectre. These sub blocks are used in construction of CMOS converter circuit.

CMOS VPC circuit-design and analysis: The summation and integration cell circuit adds and integrates output currents of synaptic portion of the neural network design (Mithilia and Valsalam, 2015). The integrated output synaptic voltage with different pulse widths is observed. The need to design voltage to pulse converter arises as the state of the neuron is propagated as pulse signal (Bor and Wu, 1998, Chen and Shi, 2000). Minimum aspect ratio values are used in design to ensure lesser area occupied by the converter circuit in overall neural network design. Table 1 shows the aspect ratio values for transistors used in the circuit. The value L is fixed to 1 μm. The schematic of the converter circuit is given in Fig. 3 which has V_v as the input voltage that varies from 0 -V_{dd} V_v has it's voltage levels determined from source follower M7-M10. Ctrl is the controlling pulse input voltage and V_p is the output pulse voltage. Both inverters act as comparators with transiting voltages adjusted to low value. Cap is the voltage across the capacitor C_0 = 220 fF. The biasing current I_B = 22 μA.

The circuit operates as follows. When Ctrl signal goes high, the voltage across capacitor C_0 represented as Cap voltage is lowest (i.e.,) 0 V. When Ctrl goes low, V_p becomes high and now Cap voltage should increase

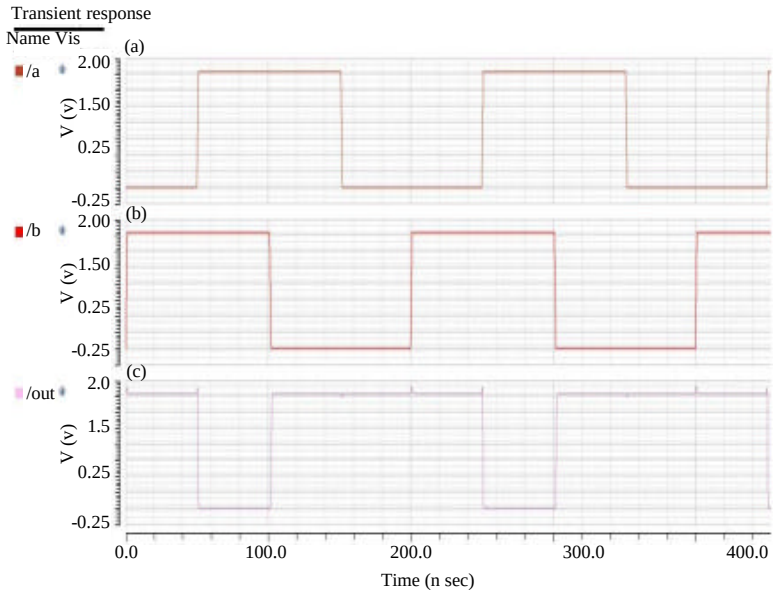

Fig. 2: Output of CMOS NAND gate

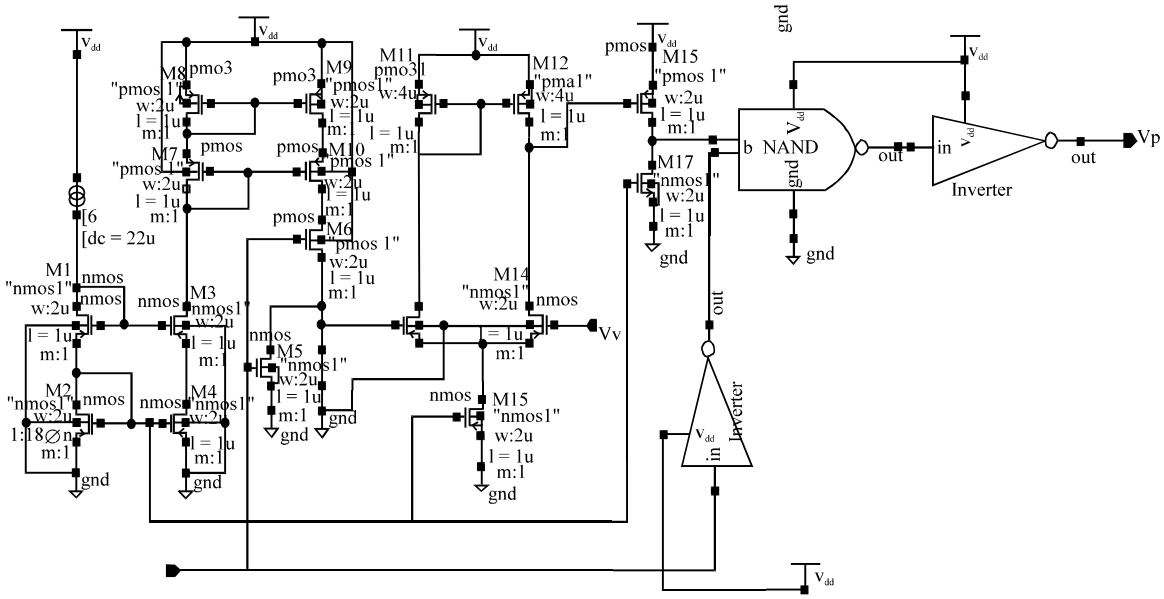

Fig. 3: CMOS VPC circuit

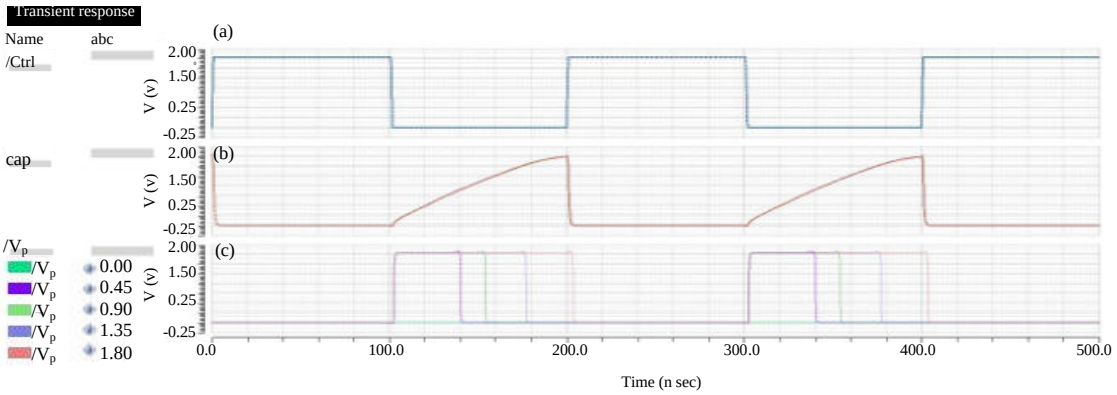

Fig. 4: Output of CMOS VPC circuit

linearly from low. When comparator overturn occurs, Cap voltage exceeding V_v, V_p should go low. This activity is clearly observed in output obtained as in Fig. 4. Parametric analysis is done to observe pulse width for various values of V ranging from 0-1.8 V.

According to the activity of pulsewidth (T_{width}) we arrived at the following Eq. 2:

$$T_{width} = 55.5 \times V_v \quad (2)$$

We observed that the value of pulse width changes for the range $0.45>V_v>1.8$ V That is V_p shows 0 value for $V_v<0.45$ V and no change in pulse width for $V_v>1.8$ V.

CMOS sigmoid circuit: Analog sigmoid function is a smooth version of step function. It is zero for low input. At some point, it starts rising rapidly and at even higher levels of input, it saturates. Naturally such a property can be noticed biologically, where the firing rates of neurons are limited by certain conditions.

The output of neuron in any of the various layers of MLP are multiplied by synaptic weights forming the multiplier (Chen and Shi 2000; Mithalia and Valsalam 2015). They are then summed to form the activation voltage for subsequent layers of the network.

Differential amplifier can be used as its transfer function is monotonic, continuous and saturates at the extremes. In PWM operations, design criteria are better set in analog as PWM circuits are localized. The hand calculations are done with help of process and model

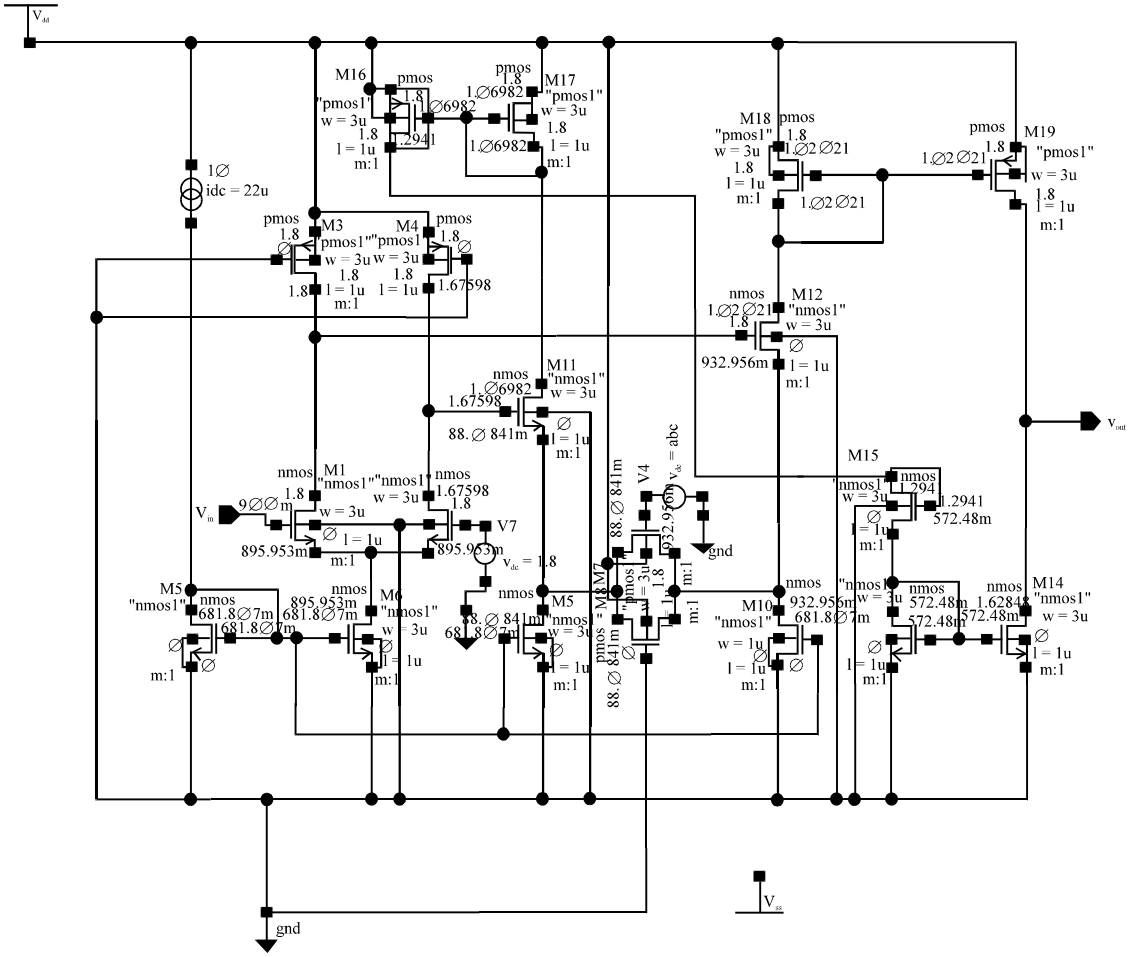

Fig. 5: CMOS sigmoid circuit

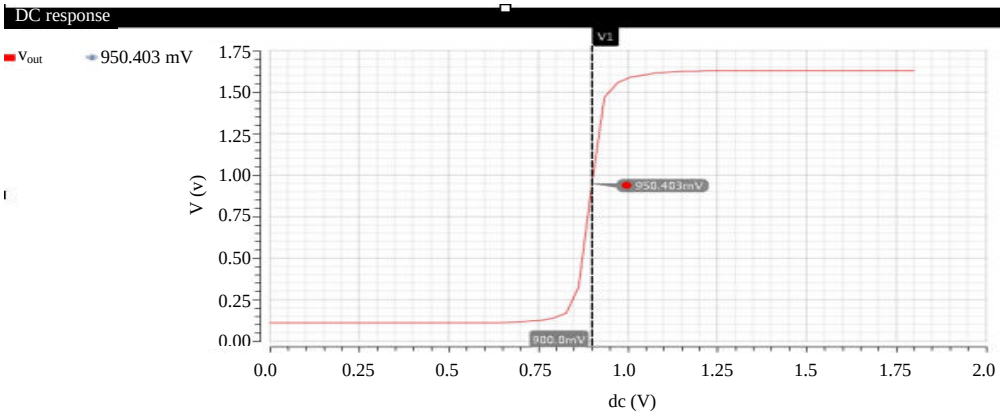

Fig. 6: Output of sigmoid function circuit

parameters as described by BSIM3V3 manual and GPDK 180 process files used in Cadence Virtuoso 6.1.6 (Cheng *et al*., 1996; Allen and Holberg, 2002).

In Fig. 1, for design of voltage mode sigmoid circuit, V_{in} is the input voltage, V_{dc} = abc is the controlling voltage used for parametric analysis and V_{out} is the output

Table 1: Aspect ratio (s) table

S = W/L	Calculated values
S_1-S_{10}	-
S_{13}-S_{17}	2
S_{11}, S_{12}	4

Table 2: Aspect ratio (s) table

S = W/L	Calculated values
S_1-S_6	3
S_7, S_8	2
S_9, S_{10}	1
S_{11}-S_{19}	3

voltage. The power supply is kept at ±1.8 V. The value of L = 1 μm and GPDK 180 process is used to calculate values of aspect ratio.

V_{out} is the output and the DC analysis for V_{in} vs. V_{out} shows the exponential curve as observed in output Fig. 3. The result in Eq. 3 is obtain:

$$V_{out} = \frac{1.8}{1+e^{-4}(V_{in}-0.9)} \quad (3)$$

This circuit can replace the working of Eq. 3 while designing the entire analog pulsed neural network using 180 nm process technology in Cadence Spectre Virtuoso 6.1.6.

CONCLUSION

A voltage mode CMOS based synapse multiplier, a voltage to pulse converter circuit and an activation function unit makes analog pulsed neural network. In the reserach two of these subcircuits have been designed using 180 nm process technology in Cadence Spectre Virtuoso 6.1.6. Its working can be tested for training analog neural networks and implemented in neural chips. They have wide use in communication systems and few hearing aid designs.

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