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Performance of Three Level Neutral Clamped PWM Inverter Fed Induction Motor Drive

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Abstract: This study presents the simulation of three level neutral clamped PWM inverter fed induction motor. The poor quality of current and voltage of a conventional inverter fed induction machine is due to the presence of harmonics. Using multilevel inverter harmonic content can be reduced. In symmetrical circuit the voltage and power increases with the increase in level of inverter. As power devices have been added in multilevel inverter structure, the voltage waveform has more redundant switching states, so that switching angle can be chosen for harmonic reduction. The simulation results closely agree with the theoretical results.

Key words: PWM, conventional, harmorics, symmetrical, reduction

INTRODUCTION

The recent advancement in power electronics has initiated to improve the level of inverter instead increasing the size of filter. In multilevel inverter, design involves parallel connection of inverter. In this paper space vector modulation technique is used. Figure 1 shows the single arm of three level inverter. For these redundant switching a space vector modulation is needed which is based on vector selection in dq stationary reference frame. For a multilevel system either space vector modulation or sinusoidal triangle modulation may be taken. However space vector modulation is having more advantages due to low harmonic production. So space vector modulation is preferred. In SVM the desired vector Vdq will follow the circular path, if a three-phase set of voltage are required on load.

The performance of the multilevel inverter is better than classical inverter. The total harmonic distortion of the classical inverter is very high. In other words the total harmonic distortion for multilevel inverter is low. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors. The voltage across the switches is only half of the DC bus voltage. These features effectively double the power rating of voltage source inverter for given semiconductor device. The total harmonic distortion is analyzed between multilevel inverter and other classical inverter. It is seen that THD is decreased if the level of inverter is raised.

Voltage level notation: The switching states s_a, s_b and s_c will be defined for the a, b and c phase, respectively. Each switching state has a range from 0 to (n-1) in order to represent the complete number of switching levels. Assuming proper operation, the inverter output line-to-ground voltages follow the switching states as,

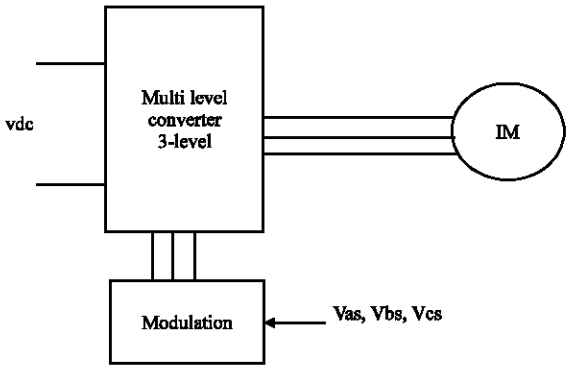

Fig. 1: Multilevel inverter system

$$\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} = \left(\frac{v_{dc}}{n-1}\right)\begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \quad (1)$$

From Fig. 1 it can be seen that the modulator determines the switching states. There by depicting the inverter output voltages. This system is somewhat idealized since, in practice, the output of the modulator is the transistor signals. Furthermore, the line-to-ground voltages may vary a bit from (1)-(3) since the voltage levels are typically made up from a series capacitor bank. However, these issues will be more formally addressed in the following section relating to the specific multi-level hardware.

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According to the modulation process, the output is an ideal sine-wave with switching harmonics. It is fairly obvious that increasing the inverter levels results in an inverter output voltage that more closely tracks the ideal sinusoidal output. The line-to-neutral voltages may be determined directly from the line-to-ground voltages by[1].

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (2)$$

Inverter line-to-line voltages are related to the line-to-ground voltages by

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (3)$$

Shows the switching state, line-to-ground voltage, line-to-neutral voltage and line-to-line voltage for the case where n = 3. Therein, the line-to ground voltage contains a third harmonic component which is added in order to maximize the inverter output voltage [1]. Therein, it can be seen that the line-to neutral and line-to-line voltages do not contain the third harmonic. Also, it is interesting to note that these voltages contain more levels than the original line-to ground voltages. It is easily understood that there are 2n-1 line-to-line voltage levels consisting of n positive levels, n negative levels and zero.

Voltage vectors: It is required to view the voltages in the q-d stationary reference frame. The resulting vector plot contains information from all three phases and displays redundant switching states. The plot is particularly useful for comprehending the higher number of switching states. In addition, some mathematical relationships and derivations can be readily obtained from the vector plot. The vector diagram has also been used to formulate multilevel modulation. However, it will be shown later that this is more readily accomplished in the time domain. The inverter voltages can be expressed in the arbitrary q-d reference frame by[1].

$$\begin{bmatrix} v_{qn} \\ v_{dn} \\ v_{0n} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta-\frac{2\pi}{3}) & \sin(\theta+\frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (4)$$

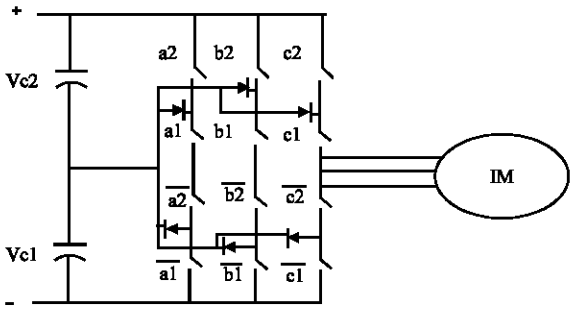

Fig. 2: Three-level diode-clamped inverter

Considering (1), (2) and that the angle is $\theta = 0$ for the stationary reference frame, the *q-d* stationary voltages can be expressed in terms of the switching states by

$$v_{qn}^{s} = \frac{v_{dc}}{3(n-1)}\left(2s_a - s_b - s_c\right) \quad (5)$$

$$v_{dn}^{s} = \frac{v_{dc}}{\sqrt{3}(n-1)}\left(s_c - s_b\right) \quad (6)$$

The vector plot created by graphing the voltage vector defined by

$$v_{sw} = v_{qn}^{s} - jv_{dn}^{s} \quad (7)$$

for all possible switching states. Figure 2 shows the vector plot for the three level inverter. Therein, each vector vsw is denoted with a unique number. For the general n level inverter vector number can be related to the switching state by

$$sw = n^2 s_a + n s_b + s_c \quad (8)$$

Figure 2 shows that there are several vectors, which result from a number of switching states. This switching state redundancy occurs since the common-mode component of the switching states is not included in the two-dimensional voltage vector plot. For the general n-level three-phase inverter, there are

$$n_{sw} = n^3 \quad (9)$$

Switching states and

$$n_{vec} = 3n(n-1) + 1 \quad (10)$$

Voltage vectors.

Redundant switching states: The redundant switching states seen in Fig. 3 provide some flexibility in the multilevel systems and will be used to achieve control objectives in later sections. For now, it is helpful to define some basic redundant state relationships. The number of redundant states for a particular switching state set can be calculated by

$$n_{RSS} = n - (s_{max} - s_{min}) \quad (11)$$

where max s and min s are the maximum and minimum of the switching state set or

$$s_{max} = \max (s_a, s_b, s_c) \quad (12)$$

$$s_{min} = \min (s_a, s_b, s_c) \quad (13)$$

Since this redundancy involves all three phases, it is referred to as joint-phase redundancy. It will be shown in later sections that some multilevel topologies have redundancy within each phase. This per-phase redundancy can be used or combined with joint-phase redundancy to achieve certain control objectives such as capacitor voltage balancing.

Diode-clamped multilevel inverter: The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention[2], the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels[3] where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped inverter was introduced[3]. However, with an even number of voltage levels, the neutral point is not accessible and the term multiple point clamped is sometimes applied[4]. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three level.

Figure 3 shows the topology of the three-level diode-clamped inverter. Although the structure is more complicated than the two-level inverter, the operation is straightforward and well known[4]. Each phase node (a, b, or c) can be connected to any node in the capacitor bank (d0, d1, or d2). Connection of the a-phase to junctions d0 and d2 can be accomplished by switching transistors Ta1 and Ta2 both off or both on, respectively. These states are the same as the two-level inverter yielding a line-to-ground voltage of zero or the dc voltage. Connection to the junction d1 is accomplished by gating

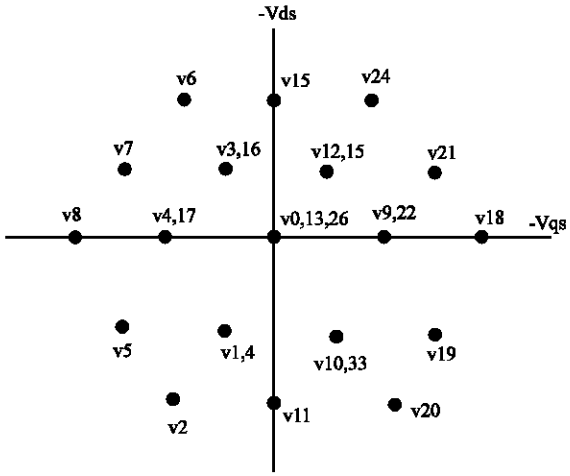

Fig. 3: Voltage vector plot

Ta1 off and Ta2 on. In this representation, the labels Ta1 and Ta2 are used to identify the transistors as well as the transistor logic (1 = on and 0 = off). In a practical implementation, some dead time is inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition[1]. However, for the discussion herein, the dead time will be ignored. From Fig. 2, it can be seen that, with this switching state, the a-phase current as i will flow into the junction through diode Da1 if it is negative or out of the junction through diode Da2 if the current is positive. According to this description, the inverter relationships for the a-phase are presented in Table 1. A Four Level Rectifier Inverter System is presented by Sinha and Lipo[5]. A Diode-Clamped Multi-Level Inverter for the Statcom is presented by Cheng and Crow[6]. Advanced Static Compensation using a Multilevel GTO Thyristor Inverter is presented by Menzies and Zhuang[7]. A Generalized Multilevel Inverter Topology with Self Voltage Balancing is presented by Peng[8]. Fundamentals of a New Diode Clamping Multilevel Inverter is presented by Yuan and Barbi[9]. DC Bus Ripple Minimization In Cascaded H-Bridge Multilevel Converters under Staircase Modulation is presented by Fukuta and Venkataramanan[10].

If each capacitor is charged to one-half of the dc voltage, then the line-to-ground voltage can be calculated by the ideal Eq. (1). The dc currents i1adc and i2 adc are the a-phase components to the junction currents i1 dc and i2dc, respectively. Extending the diode-clamped concept to four levels results in the topology shown in (Fig. 3). In the literature[1-10] the frequency spectrum and speed

Table 1: Three-level inverter relationships

S_a	T_{a2}	T_{a1}	v_{ag}	i_{adc1}	i_{adc2}
0	0	0	0	0	0
1	0	1	v_{c1}	i_{as}	0
2	1	1	$v_{c1} + v_{c2}$	0	i_{as}

response of three level inverter fed induction motor is not presented. In the present work an attempt is made to obtain the frequency spectrum and speed response of three phase induction motor drive system.

RESULTS AND DISCUSSION

The simulation studies have been done for three level inverter fed 5 HP induction motor model shown (Fig. 4) with line voltage 460 volts, 60 Hz, 1750 r.p.m and modulation index of 0.85. The (Fig. 5) shows the line to neutral voltage Van, line to line voltage Vab and load voltage. The (Fig. 6) shows the motor stator current and rotor current. The motor speed and electromagnetic

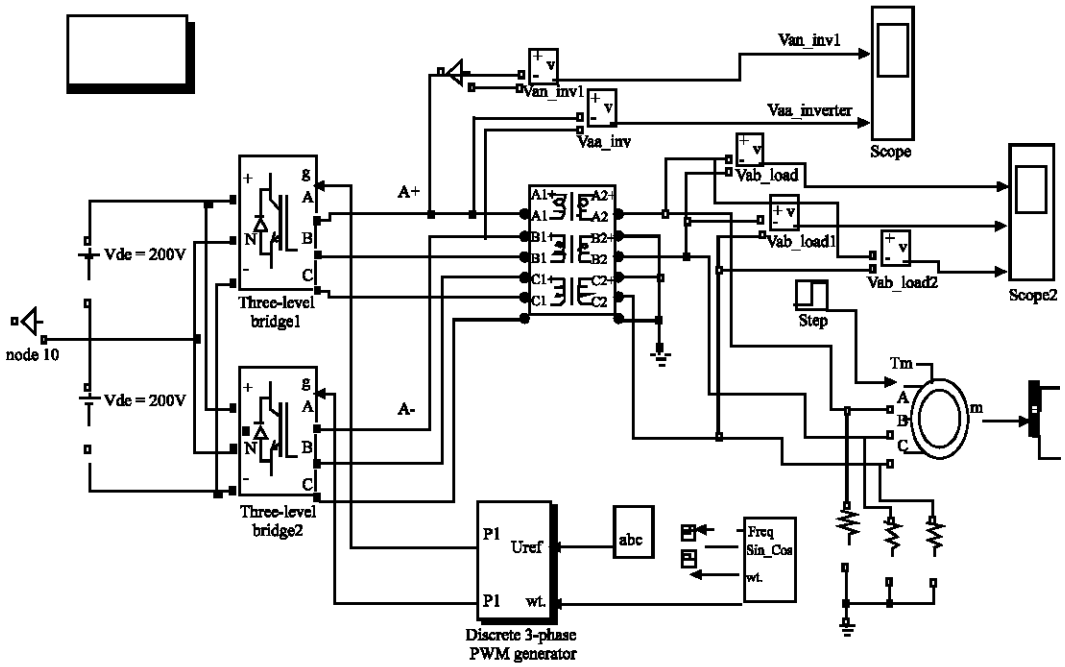

Fig. 4: Circuit model of three level inverter fed induction motor

Fig. 5: Phase, line and load voltages

Fig. 6: Stator and Rotor currents

Fig. 7: Motor Speed

Fig. 8: Electromagnetic Torque

Fig. 9: FFT Spectrum

torque are shown in (Fig. 7 and 8). The (Fig. 9) shows FFT Spectrum of the load voltage. The total harmonic distortion is 0.15% and it is very low compared to that of the conventional inverter.

CONCLUSION

The modeling of three level inverter fed induction motor drive has been done with redundant switching strategy and simulated using MATLAB SIMULINK. The total harmonic distortion is 0.15% and it is very low compared to that of conventional inverter. The simulation result shows that the harmonics have been reduced considerably. The PWM inverter fed induction motor system has been successfully simulated. The frequency spectrum for the output was obtained. The induction motor system considered has reduced harmonics.

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