International Journal of Electrical and Power Engineering 1 (1): 36-42, 2007
© Medwell Journals, 2007

An Improvement of Electrical and Technological Properties in Second Generation Mesfet Devices

[1]Mohamed Salah Benbouza and [2]Nadjim Merabtine
[1]Département d'électrotechnique Faculté des Sciences Université de Batna Algeria
[2]Laboratoire Electromagnétisme et Télécommunications Université de Constantine Algeria

Abstract: Since 1961 date of the first integrated circuit to 1971 which has seen the first microprocessor application, the micro-electronics passed from a discrete transistor to MSI integrated circuits with many thousands of integrated components and now to VLSI integrating many hundreds of thousands of devices. Technological recent technological progress permitted the GaAs and its ternary derivative to be the second generation material. So, we present a study on the Gallium arsenide material specifying its transport and electric properties and its specific advantages over the silicon material. A semi insulating substrate study of a gate Schottky diode for the GaAs MESFET devices manufacturing such as structures with and without buffer layer, with buried gate, mushroom and several fingers are carried over. We will study the influence of the input impedance and output resistance to the gate as well as the noise generated by the structures to several fingers.

Key words: GaAs MESFET, gate in T and PI, gate resistance, noise

INTRODUCTION

The aim of this research is the study of the logical integrated circuits based gallium arsenide gate Schottky field-effect transistors called GaAs MESFET. As a matter of fact, the integrated circuits development has a very important impact on the whole of electronics effectively, since 1961 dates from the first integrated circuit, to 1971 that saw the first microprocessor apparition, the micro electronics passed from to LSI circuits with thousand of integrated components and now to circuits VLSI circuits integrating several hundreds of thousands of devices.

In this study, we are first interested by the gallium arsenide GaAs material that is the bases of this technological evolution, then to different structures of MESFET GaAs component which composes a choice device for the conception and the realization of ultra fast logic circuits at propagation time inferior to the nanosecond.

GaAs material: The choice of GaAs as material permitting to obtain very high performances for the integrated circuits is not only related to very interesting semi-conducting properties but to a propitious compromise between different criterion such as the metallurgic properties, ability to technological realisation, working temperature, tolerance to radiations. The last year technological progress permitted GaAs and its ternary derivatives to be the second generation material.

Transport properties: The N type gallium arsenide presents excellent transport properties[1]. For weak values of the doping of material doping, mobility at weak field can reach values of 8000-9000 cm2/Vs at the ambient temperature (10000 to 80000 cm2/Vs with 77°K). At the usual doping (10^{17}. Cm^{-3}), the electrons mobility is six times higher in GaAs than in the Si and their transport speed is twice (higher) faster. The speed saturation at high electric field is reached for an electric field less higher than the Si. As a result ,the transit time of GaAs MESFET with gate length between 0.5 and 0.1 μm is of the order of 10 to 20 picoseconds corresponding to cut-off frequencies of gain the product incurrent-pass band-between 20 to 30 GHz. For a similar conception, we point out merit factor for to six times superior to those obtained on silicon JFET devices.

Electric properties: The electric properties of GaAs with 300°K intervening in the discrete or integrated circuits manufacture are gathered in Table 1.

Semi-insulating substrate: The semi insulating GaAs material availability[2] (resistivity included between 10^7 and 10^9 Ωcm with T=300°K°) is a substantial advantage from technological and electrical performance point of view. The inter device insulation is ensured without circuits performances damage: thus the parasitic capacities linked to the mass plan remain inferior to the coplanar parasitic capacities of drain-source contacts interconnections lines.

Corresponding Author: Mohamed Salah Benbouza, Département d'électrotechnique Faculté des Sciences Université de Batna Algeria

Table 1: Main properties of GaAs and SI at 300°K

Properties	GaAs	SI
forbidden band energy	1.43eV	1.12eV
forbidden band type	Direct	Indirect
State density in the conduction band	$5.10^{17}cm^{-3}$	$5.10^{19}cm^{-3}$
Charge at MIS interface	$10^{13}cm^{-3}$	$10^{10}cm^{-3}$
Life duration of the minority carriers	$10^{8}s$	$10^{4}s$
critical field at high field mode	$3.10^{2}Vcm^{-1}$	$1.10^{2}Vcm^{-1}$
Break-down field	$4.10^{5}Vcm^{-1}$	$3.10^{5}Vcm^{-1}$
Schottky barrier height	0.7-0.8V	0.4-0.6V
Electronic mobility at Nd $=10^{17}$ Cm^{-3}	$4900cm^{2}$ $V^{-1}s^{-1}$	$800cm^{2}$ $V^{-1}s^{-1}$
holes mobility	$250cm^{2}$ $V^{-1}s^{-1}$	$350cm^{2}$ $V^{-1}s^{-1}$
electrons mobility speed	1.10^{7} cms^{-1}	$1.10^{9}cms^{-1}$
Maximale resistivity	$10^{9}\Omega cm$	$10^{9}\Omega cm$

The obtaining method of semi-insulating GaAs substrates consists in compensating the residual levels obtained materials using the of Bridgman method by a specifically deep impurity; the chrome being mostly used. The use of ionic implantation of the chrome doped GaAs obtained by Bridgman growth revealed anomalies appearing during the annealing after implantation.

The phenomenon tied to the Cr oxodiffusion during the thermal treatment is identical to the one met on epitaxied layers on Cr doped GaAs.

GaAs MESFET transistors manufacture: On GaAs, the base component is in fact the Schottky gate field-effect transistor called MESFET (Metal Semiconductor Field Effect- Transistor) which is a majority carriers device, its structure is particularly simple easily realizable in N type thin layer. This MESFET active layer is a thin conducting uniform layer with a thickness d (1000-2000Å) with can vary doping between 10^{16} and 3.10^{17} Cm^{-3} according to the structure, N doped by means of sulphur or tin some time. The active layer growth is realized by various technologies[3]:

- Liquid phase epitaxy, the later does not allow a strict control thickness d.
- molecular jets epitaxy[4] that allows an excellent control of active layer thickness(a few thousands of Angströms-layer) and is particularly well adapted to the GaAs MESFET realization, of normally blocked said Normally off.
- Ionic implantation, this semi isolating doping technique permits to realise layers with properties similar to those obtained by epitaxy and present certain advantages for the reproducibility and structure homogeneity.
- Vapor phase epitaxy by metallic device or chlorids[4] is the softest method and the most adapted to the industrial treatment; it actually remains the privileged toolt for the discrete devices.

The N layer region Fig. 1a form the active area. The source-drain contact are composed by an eutectique obtained by an alloy (400-500°C) of thr gold germanium layer with GaAs.

Metallization of nearly 0.5 μm thicknesses formed by a titanium gold compo doposit ensure the device interconnections with the elements.

The MESFET main advantage is the particularly simple gate structure that always to reduce its geometry to extreme values comparatively to other transistors.

It is sufficient to engrave on GaAs the metallic band that forms the grate. For the integrated circuits, the typical length is of 1 μm but the actual tendency is to pass to the submicronics geometries. the gate length which determines at the time the input capacity on the electrons transit time in the channel conditions the performances at average velocity of 10^{7} $cm.s^{-1}$, leads to a 10 ps a transit time and a current gain cut-off frequency of the order of 15 GHz. Taking the new possibilities in micro lithography into consideration, the microelectronics on GaAs is more advanced than silicon technology.

Structure with and without buffer layer: The first transistor as being realised by means of epitaxial layers directly deposited on semi -insulating substrate Fig. 1a.

Their performances have being affected by effects by hysteresis. Is effect in order to minimize the activate substrate interface layer, it has became classical to insert an epitaxial layer called "buffer" weakly doped (10^{12} to 10^{11} cm^{-3}) and which the average thickness is of 1the order 10 μm Fig. 1b.

In order to improve the device performances, several manufacture techniques has being proposed .We will present some of them[5].

Ploughed or "buried"gate GaAs MESFET": In GaAs and for a free face, there is potential barrier near the surface one Fig. 2. This latter is expressed by the space charge density existence, extending in the drain gate and source gate-space.

It follows a noticeable increase in access resistances. The latter limit the current which is then badly controlled by the gate (particularly for the weak gate polarization or lightly positive) . To improve the transistor command, we realise a buried gate. This structure is realised by grooving using by a chemic attack or plasma engraving, a trench in the semiconductor between the source and drain contacts. Then the gate metal is pulverized at the very bottom of this trench. By this method we reduce the access resistances to the intrinsic region of the component (under the gate) due the lateral region uncontrolled by the gate. This process presents, however,

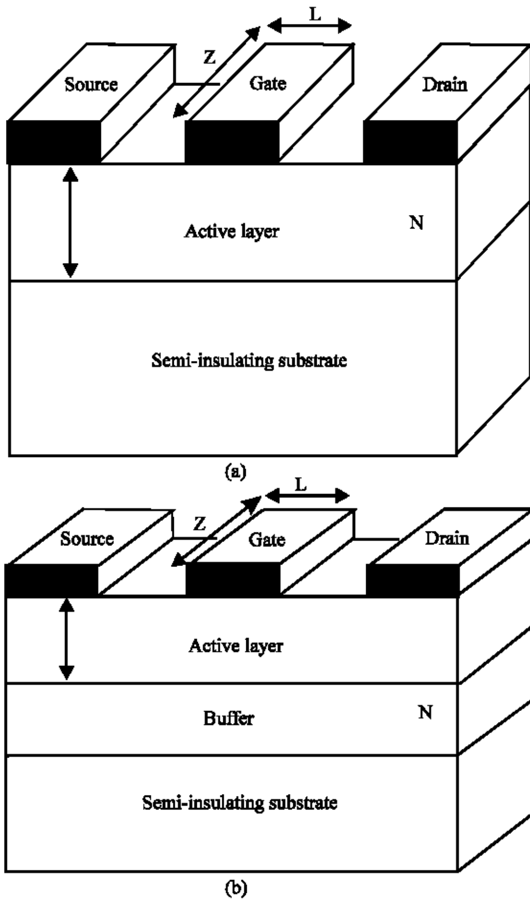

Fig. 1: Structure of the GaAs MESFET; (a) MESFET without buffer layer; (b) MESFET with buffer layer

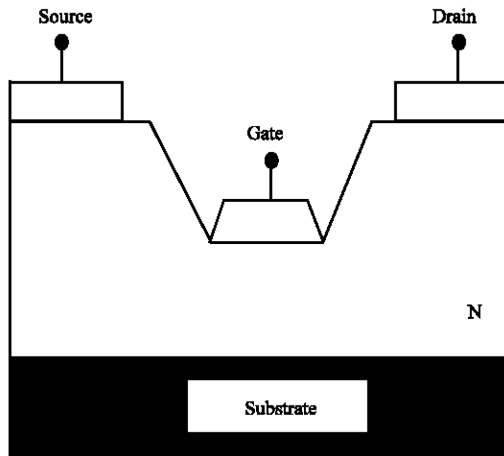

Fig. 2: Longitudinal section of the MESFET with buried gate

the disadvantage to increase the technological operations complexity .we often prefers the locad ionic implantation technics that permit to over dope the inter electrode regions and consequently to decrease the access

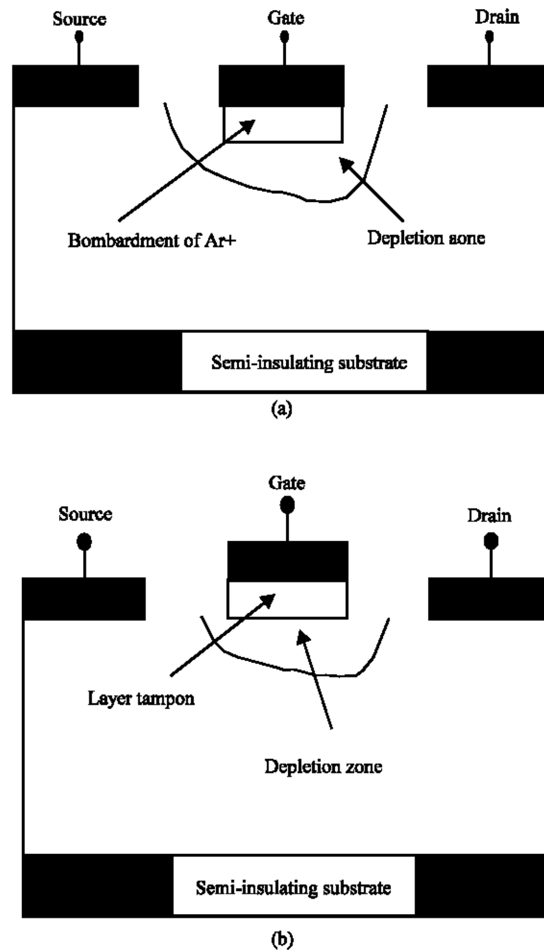

Fig. 3: Structure GaAs MESFET with buffer layer; (a) Gate bombardment with Argon Ions; (b): Gate buffer layer

resistances by selectively increasing the donors density Nd (N type semiconductor N type) under the lateral regions.

Buffer layer structure GaAs MESFET: To improve the GaAs MESFET commutation and hyper frequency performances many gate configuration are considered Fig. 3a shows a structure with semi insulating gate, manufactured by Ar bombing of the gate region. The device can reduce the capacity, reduce also gate the leakage current and increase the tension of breakdown voltage. The Fig. 3b shows a similar structure with a gate in "buffer". This layer is inserted between the gate metal and the active layer, the self-aligning technics has being used to realised components with submicronic gate length.

T and PI GaAs MESFET structures:

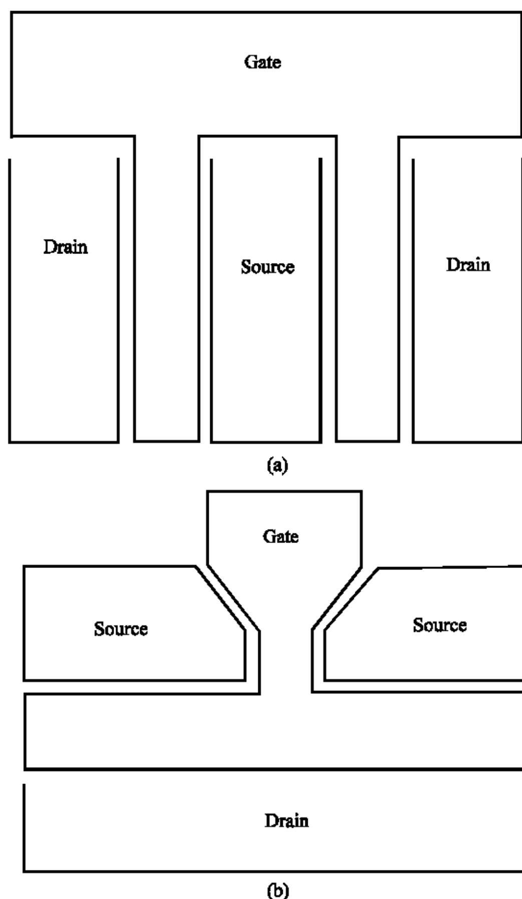

Fig. 4: T and PI GaAs MESFET structures; (a) T GaAs MESFET; (b) PI GaAs MESFET

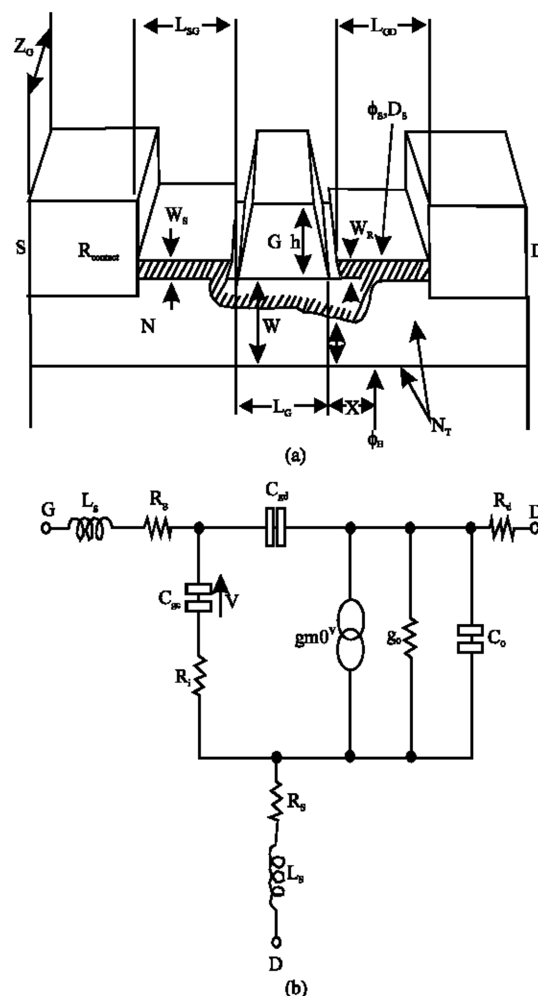

Fig. 5: Parameters of MESFET; (a) geometrical parameters; (b) equivalent circuit in high frequency

Equivalent circuit of the MESFET: The equivalent circuit of a component MMIC must sufficiently represent all the important physical characteristics of the device and exploit the relationship between the equivalent elements of the circuit and physique of the device which will be useful in the mathematical formulation.

Transistor MESFET and HEMT to study is represented on Fig. 5a. the structure which determines the behaviour of microwave of a transistor MESFET is identified on the Fig. 5b; some of parameters important are deferred in[6,7].

Where: N is the doping density in the N layer of the channel, W is the thickness of the layer N of the channel under the gate, Z_G is the width of the gate, L_G is the length of the metal gate, L_{SG} is the separation gate-source, L_{GD} is the separation gate-drain, W the depression depth of the gate, Ws is the exhaustion depth of the surface, d is the depth of exhaustion, h is the height of the gate, X is the extension of the gate charge space under the gate.

Influence of gate resistance on the input impedance: Resistance associated to the gate metallization deteriorates the microwaves and commutation performances. To carry out weak noise MESFET, it is important to decrease the gate resistance. This gate resistance Rg was identified a long time as a parasitic parameter which deteriorates the noise factor and limits the power gain of the Schottky-barrier-gate MESFETS (SBGMESFETs). We add a metallization resistance: Rga to Rg as shown on the Fig. 5b this gate metallization resistance contributes clearly to Rg[8]. It is given in a distributed way and confirms the effect of the resistance end to end of the gate finger:

$$Rga = \frac{r_{ga} W_g}{3Nk^2} \quad (1)$$

To distinguish this well-known resistance from the component MESFET which is the aim of this article, we presented this access resistance along the gate finger rga, it is then the end to end normal metallization resistance given by:

$$r_{ga} = \frac{\rho}{A_{gx}} \quad (2)$$

where ρ is the metal resistivity of gate and Agx is the gate section . Wg is the gate and Nk is the number of parallel fingers. Because the undercarriage length of door is narrowed with major submicronic dimensions it is usual to limit the increase in the rga by using a formed cut T and to increase the number of parallel fingers. The skin effect will present the frequency response in the metallization access resistance of the gate in AC regime[4]:

$$r_{ga}^{ae}(f) = r_{ga}\sqrt{1+\frac{f}{fse}} \quad (3)$$

where the frequency characteristic for the beginning of the significant skin effect is:

$$fse = \beta\frac{r_{ga}}{\mu o} \quad (4)$$

μo = 4.10-7 Vs/Am is the free space permeability and β a geometrical factor, roughly equal to 3,5 for a cross section of the cross-section. For a rga=150 Ω/mm, the fse is 420 GHz. Although β can be reduced by the presence of a plane on the ground[5], the skin effect seems certainly to be negligible. We prove numerically that the skin effect is indeed negligible and that Eq. 3, 4 are precise and adapted for SBGMESFET. Another resistive component on the input side of the MESFET is the filling resistance Ri (or Rgs) for the gate-source capacity. This parameter is often hard to separate from Rg during the extraction of the equivalent circuit[6]. However, Ri is between a sixth and a fifth of the channel resistance for a used zero-drain-polarization[7].

$$Ri = \frac{1}{5}Ro\left(\frac{Lg}{Wg}\right)\left(\frac{Id\max}{Id}\right) = \frac{Lg.vsat}{5\mu Id} \quad (5)$$

where Ro is the plate resistance and Idmax the current saturation of the channel, vsat is the speed of saturation and μ the mobility. The factor 1/5 in Eq. 5 is the higher limit of quantity:

$$(R11-R12)/(I11-I12)^2$$

where Rij and Iij parameters determine the Y parameters and are derived from the waves linear equation of the MESFET inside[8]. It explains both the distributed nature of Ri and the change of the electron concentration of the sheet along the channel. Both Eq. 1 and 5 foresee very small resistances, often much smaller than the values produced by methods of extraction of equivalent circuit. It is an indication of an additional component in the input resistance, whose physics must be established in order to understand better the MESFET component and to produce measurable models. To finish the study of effect of the conducting semi metal interface, we add a component to Rg resistance[9] which defines the gate resistance f the normalized interfacial resistance. This resistance is defined as a contact resistance with the substrate, rgi being the normal gate resistance of the normalized interfacial resistance.

$$Rgi = \frac{r_{gi}}{WgLg} \quad (6)$$

Simulation AC of the influence of the gate resistance and gate length on the input and output impedance of GaAs MESFET transistors are represented on Fig. 6, 7 and 8.

Influence of the gate on the noise factor: We can observe three different sources of noise: For low frequencies the factor (1/F) called wavering noise which draws its performance from the low frequency and the care should be taken to avoid excessive attenuation of the signal compared to the signal at lower frequencies; this noise will not be important in amplifiers which operate above the frequency (which is the frequency that the thermal noise

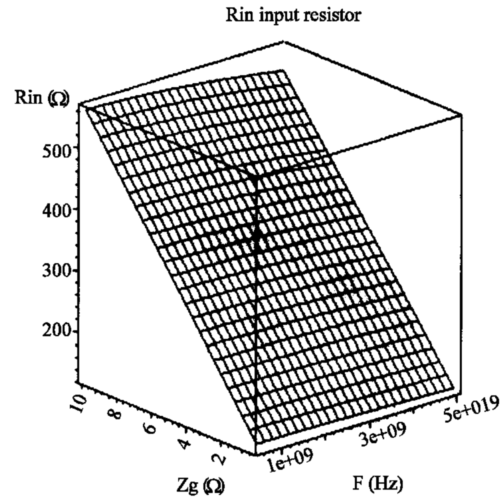

Fig. 6: Gate influence on Z in

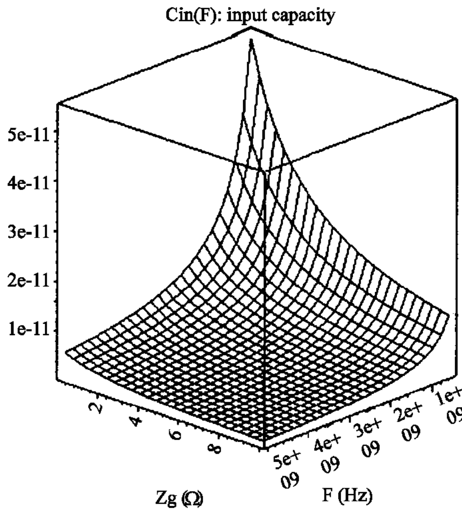

Fig. 7: Gate influence on C in

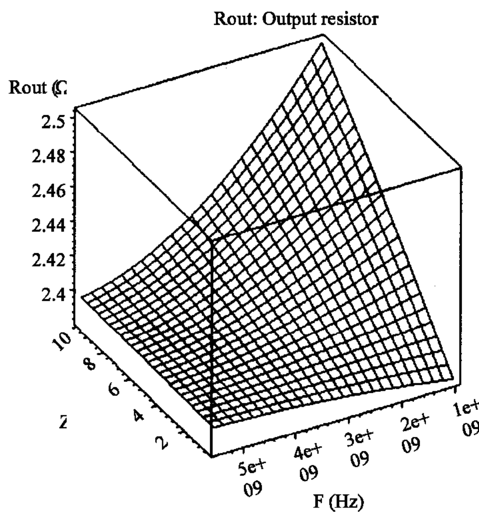

Fig. 8: Gate influence on R out

starts to dominate this noise). This noise causes a serious problem in the oscillators and the mixers because of the non -linearity intrinsic devices. This noise is primarily due to carriers hopping in and out of deep levels in the substrate, buffer and active layer and out of surface traps on the channel surfaces. It can be minimized by the deep-level density control and by the passivation of active layer surfaces. For this reason, HBT and HEMT appear essentially to be of better candidates for these applications with great controls and qualities which are now available with the epitaxial growth techniques. At larger frequencies parasitic resistances such as R_S and R_G starts to dominate the sources of disturbance of the

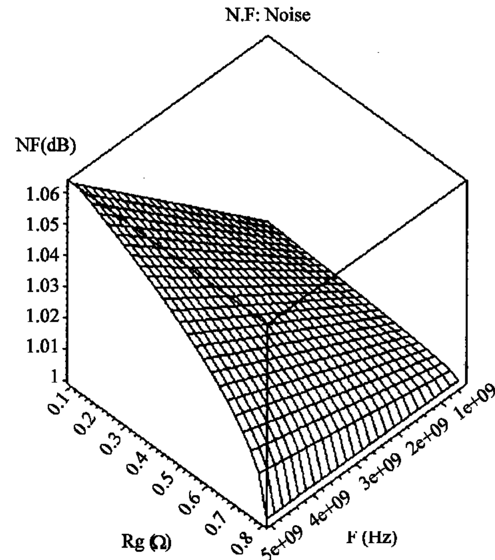

Fig. 9: Gate influence on the noise

device. We should add to this the noise created by the thermally induced statistic fluctuation in the local carrier density in the channel.

The principal application of GaAs MESFET was in amplification with weak noise. It is important in the determination of a simple analytical expression to calculate the factor of minimum noise of a field-effect transistor. Since the factor of noise of a field-effect transistor is carried out by taking into account the point of operation and the equivalent impedance of the circuit. The noise factor: NF is related to four elements: gmo, Cgc R_S and Rg which are measured starting from the S parameters extracted empirically from small model signal, Fukui derived a simple expression for NF[8]:

$$NF \approx 1 + K_F ?\, C_{gc}\left(\frac{R_S - R_g}{g_{mo}}\right)^{1/2} \quad (7)$$

Or the factor KF = 2.5 to 3.0 transistors MESFET and KF = 1.5 to 2.0 for HEMT. Factor KF is often a simplification of noise generated by the drain current. Another simple expression of the noise was defined by Delagebeaudeuf and Al[10];

$$NF \approx 1 + 2?\, \frac{C_{gs}}{g_{mo}}\left(\frac{R_S - R_g}{R_i}\right)^{1/2} \quad (8)$$

The simulation of the noise factor is shown on the Fig. 9 shows that we must reduce the gate length and

minimize the parasitic source of the gate resistances. At a given frequency, the noise factor decreases with the channel length; it also decreases with the channel width; as a consequence of the reduction of R_G for narrower gate. It is also proved that a field-effect transistor uniformly doped yields less noise than the other devices which have the same geometry. This result is due to the reduction of gm (but not gm/C_{GS}) for MESFET transistors.

CONCLUSION

We presented the effect of the gate resistance of Schottky gate GaAs MESFETS for gate lengths lower than 0.5 μm. The metallization resistance Rgi is practically undetectable for wider gate lengths. This resistance Rg due to the skin effect can be induced starting from theoretical Ri. The considerations and the experimental observations prove that these resistances are not defined in an obvious manner by a fraction of input series resistance of the short gate MESFETS.

We have also studied the frequency response of the noise factor generated by these resistances. In ordre to improve the component's performances and to have a weak noise, we should reduce the gate length and minimize the parasitic' sources and also reduce the gate resistances. At a given frequency, the noise decreases with decreasing channel length. It also decreases with decreasing channel width; as a consequence of the reduction of R_G for narrower gate. It is also proved that the use of field-effect transistor yields less noise than conponents uniformly doped with the same geometry. It results in gm reduction (but not gm/C_{GS}) for field-effect transistors.

We note that resistance r_{gi} has a capacitive effect at higher frequencies and cannot be ignored at the microwave and millimetre-length wave frequencies.

REFERENCES

1. Baransky, P., V. Klotchlov and L. Potykevttch, 1978. Electronique des Semi-Conducteur, Ed Masson.
2. Lindquist, P.F. and W.M. Ford, 1980. GaAs FET Principles and Technology. JAMS.V.D.
3. Martinez, A., 1976. Thèse d'Etat,Univ Paul Sabatier, Toulouse France.
4. Baudet, P., 1980. Acta Electronica, 23, N°2. Février.
5. Graffeuil, J. and J. Obergon, 1984. Application des MESFET GaAs, ED.
6. Chen, C.L. *et al*., 2002. High-performance fully-depleted SOI RF CMOS,IEEE Electron Device Lett., pp: 52-54.
7. Ladbrooke, P.H., 1989. MMIC Design: GaAs FETs and HEMTs, Artech House, MA.
8. Tiallet-Guy, B., Z. Ouarche, M. Prigent, R. Quere and J. Obregon, 1998. Direct Extraction of a Distributed Nonlinear FET Model from Pulsed, IEEE Microwave and Guided Wave Letters.
9. Allee, D.R., A.N. Broers and R.F.W. Pease, 1991. Limits of Nano-Gate Fabrication, Proc. IEEE, pp: 1093-1991.
10. Fukui, H., 1979. Determination of the Basic Device Parameters of a GaAs MESFET, Bell Syst., Tech. J., pp: 71-1979.