International Journal of Electrical and Power Engineering 3 (4): 208-214, 2009
ISSN: 1990-7958

A Neuro Control Strategy for Cascaded Multilevel Inverter Based Dynamic Voltage Restorer

[1]S.N.V. Ganesh, [2]K. Ramesh Reddy and [3]B.V. Shankar Ram
[1]Department of Electrical Engineering, Velagapudi Siddhartha Engineering College, Vijayawada, India
[2]Department of Electrical Engineering, G. Narayanamma Institute of Technology, Hyderabad, India
[3]Department of Electrical Engineering, Jawaharlal Nehru Technical University, Hyderabad, India

Abstract: This study proposes a neural controller for cascade inverter-type Dynamic Voltage Restorer (DVR) to compensate voltage sags in utility voltages in power distribution network. The proposed DVR is implemented using multilevel inverter topology with isolated dc energy storage. The phase shifted PWM technique is described to generate firing pulses to cascaded inverter. The proposed controller adopts itself to the sag and provides effective means of mitigating the voltage sags with minimum harmonics at the utility end. The proposed concept was simulated using MATLAB simulink environment. The simulation results are presented to verify the performance of the proposed multilevel dynamic voltage restorer.

Key words: DVR, multilevel, neural, cascade inverter, mitigation

INTRODUCTION

Voltage sags are one of the power quality assets, which dragged the attention of many researchers especially in developing countries like India as the sensitivity of loads are increasing due extensive usage of power electronics devices. Faults at distribution level, sudden increase of load, motor starting are some of the causes of the voltage sags. Such sudden variations of voltage are undesirable for sensitive loads.

A dynamic voltage restorer is one such device having capability of protecting sensitive loads from all supply side disturbances. Figure 1 shows the series connection of a Dynamic Voltage Restorer (DVR) between the utility source and loads through a coupling transformer as proposed by Fang *et al.* (1998) and Chan (1998). During normal operating conditions, DVR is switched off or controlled to compensate for any injected harmonic voltages in the utility. During sag period, the DVR operates in boost mode and injects voltage of sufficient magnitude to maintain constant voltage throughout the sag period. However, phase of the load can be either be shifted or remain unchanged depending on the compensation technique adopted.

Many topologies proposed (Lai and Peng, 1995), for DVR in past, most common being 2-3-level three phase converter with dc capacitor connected alternatively to all phases. H-bridge cascade inverter (Al-Hadidi and Menzies, 2003) is the one such popularly used converter topology. Multilevel topology offers the following advantages.

- Simple structure and requires fewer components
- Packaging layout is much easier because of simplicity of structure and lower component count
- Each bridge can be controlled independently permitting efficient single-phase voltage compensation
- Ability to reach high voltage and reduce harmonics by their own structures without any transformers
- Generates multi step staircase voltage waveform similar to pure sinusoidal output voltage by increasing the number of levels

Because of performance of the overall control system largely depends on the quality of the applied

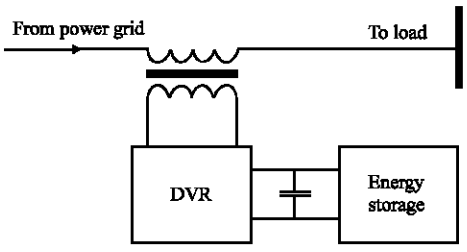

Fig. 1: Configuration of DVR

Corresponding Author: S.N.V. Ganesh, Department of Electrical Engineering, Velagapudi Siddhartha Engineering College, Vijayawada, India

control strategy, a high performance-controller with fast transient response and good steady state characteristics is required. Various control strategies have been proposed for voltage source PWM converters namely, (Kazmierkowski and Malesani, 1998; Loh *et al*., 2002a, b; Rendusara *et al*., 2000; Zhang *et al*., 2000; Corzine, 2000; Marchesoni, 1992; Buso *et al*., 2000). Some of them are ramp comparison regulator, synchronous PI regulator; state feedback regulator, hysteresis regulator, neural network and fuzzy logic regulator etc. Nonlinear controller is more suitable than the linear since, the converter is truly a nonlinear system.

The neural network is a universal estimator. This implies that neural network can be trained to approximate any smooth nonlinear function with accuracy. A Variable Structure Control (cascaded VSC) is designed initially and then the neural network is used to approximate the VSC control law. The main advantage of neural network implementation in comparison with direct VSC control is that reduces the complexity and cost of the controller.

MATERIALS AND METHODS

The series voltage controller is connected in series with the protected load as shown in Fig. 1. Usually, the connection is made via a transformer, but configurations with direct connection via power electronics also exist. The resulting voltage at the load bus bar equals the sum of the grid voltage and the injected voltage from the DVR. The converter generates the reactive power needed, while the active power is taken from the energy storage.

The energy storage can be different depending on the needs of compensating. The DVR often has limitations on the depth and duration of the voltage dip that it can compensate.

The circuit on left hand side of the DVR represents the venin equivalent circuit of the system. The system impedance Z_{th} depends on the fault level of the load bus. When the system Voltage (V_{th}) drops, the DVR injects a series voltage V_{DVR} through the injection transformer so that the desired load voltage magnitude V_L can be maintained. The series injected voltage of the DVR can be written as:

$$V_{DVR} = V_L + Z_{th}I_L - V_{th} \quad (1)$$

where:

V_L = The desired load voltage magnitude
Z_{th} = The load impedance
I_L = The load current
V_{th} = The system voltage during fault condition

The load current I_L is given by:

$$I_L = \left(\frac{P_L - J\times Q_L}{V_L}\right)^x \quad (2)$$

when:

V_L = Considered as a reference

Equation 1 can be rewritten as:

$$V_{DVR} \angle\alpha = V_L \angle 0 + Z_{th} I_L \angle (\beta-\theta) - V_{th} \angle\delta \quad (3)$$

Here α, β and δ are the angle of V_{DVR}, Z_{th} and V_{th}, respectively and θ is the load power factor angle.

The complex power injection of the DVR can be written as:

$$S_{DVR} = V_{DVR} I_L^* \quad (4)$$

It may be mentioned here that when the injected voltage V_{DVR} is kept in quadrature with I_L, no active power injection by the DVR is required to correct the voltage. It requires the injection of only reactive power and the DVR itself is capable of generating the reactive power. Note that DVR can be kept in quadrature with I_L only up to a certain value of voltage sag and beyond, which the quadrature relationship cannot be maintained to correct the voltage sag. For such a case, injection of active power into the system is essential. The injected active power must be provided by the energy storage system of the DVR.

Modulation strategy: Usually stair case modulation is commonly used for cascaded H-bridge converters. For SCM, the switching instants of each module are calculated offline to attenuate certain harmonics. In that case dc link voltage has to be varied in accordance to the desired ac output voltage. Due to bulk dc link voltage dynamic response slows down. As the voltage sag duration ranges from half cycle to 30 cycles, fast dynamic response is required for the DVR application. Based on this consideration, Phase shifted PWM modulation scheme is adopted to maintain a relatively constant dc link voltage, while achieving the fast dynamic response required of the output voltage by varying modulation index.

Multilevel invertors require carrier based modulation schemes due to higher levels. The carrier-based modulation schemes for multilevel invertors are classified as phase-shifted and level-shifted modulations. Multilevel inverter with m voltage levels requires (m-1) triangular carriers. In the phase-shifted multi carrier modulation, all the triangular carriers have the same frequency and the peak-peak amplitude with phase shift between any 2 adjacent carrier waves given by:

$$\Phi_{cr} = 360°/_{(m-1)}$$

The sinusoidal signal $V_{control}$ is phase-modulated by means of the angle α i.e.,

$$V_A = \text{Sin}(\omega t + \delta)$$
$$V_B = \text{Sin}(\omega t + \delta - 2\pi/3)$$
$$V_C = \text{Sin}(\omega t + \delta + 2\pi/3)$$

The modulated signal $V_{control}$ is compared against a phase shifted triangular signals in order to generate the switching signals for the VSC valves. Figure 2 shows the pulses for one phase. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal and the frequency modulation index of the triangular signal.

The amplitude index is kept fixed at 1 pu, in order to obtain the highest fundamental voltage component at the controller output.

$$M_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} = 1 \text{ pu} \quad (5)$$

where:

$\hat{V}_{control}$ = The peak amplitude of the control signal
$\hat{V}_{tri}$ = The peak amplitude of the triangular signals

The switching frequency is set at 2000 Hz. The frequency modulation index is given by

$$M_f = f_s/f_1 \quad (6)$$

where:

f_1 = The fundamental frequency

The modulating angle is applied to the PWM generators in phase A. The angles for phases B and C are shifted by 240° and 120°, respectively. It can be seen in that the control implementation is kept very simple by using only voltage measurements as the feedback variable

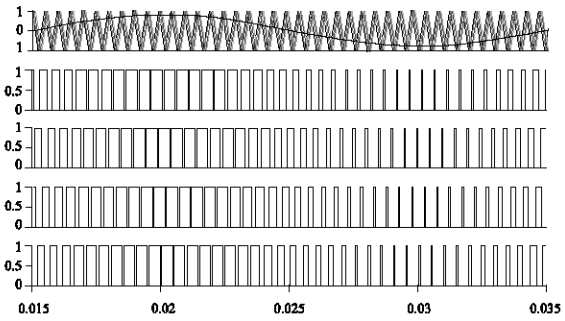

Fig. 2: Phase-shifted PWM pulses for 1 phase

in the control scheme. The speed of response and robustness of the control scheme are clearly shown in the simulation results.

The voltage level and switching state of the five level CHB (Cascaded H-Bridge inverter) is shown in Table 1.

Neural network architecture: The effective mitigation of sag and harmonics depends on the effectiveness of the controller design. Usually PI control is used to improve the static and dynamic characteristics of the system. The PI control depends on deviation regulation. The main problem of PI control is its adaptability. Because the parameters once fixed may not accommodate all conditions when the status and parameters of the system is changed. Tuning, the PI controller is also very difficult sometimes. The usage of intelligent techniques provides the better solution for tuning the respective gains and adaptability problem. Neural network is the optimal solution for such problem.

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load is connected, under system disturbances. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the Fundamental Frequency Switching (FFS) methods favored in FACTS applications. Besides, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

The controller input is an error signal obtained from the reference voltage and the value rms of the terminal voltage measured. Such error is processed by a neural PI

Table 1: Voltage level and switching states of five level CHB

	Switching state					
Output voltage van	S11	S31	S12	S32	Vh1	Vh2
2E	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	-E
	0	1	1	0	-E	E
-E	0	1	1	1	-E	0
	0	1	0	0	-E	0
	1	1	0	1	0	-E
	0	0	0	1	0	-E
-2E	0	1	0	1	-E	-E

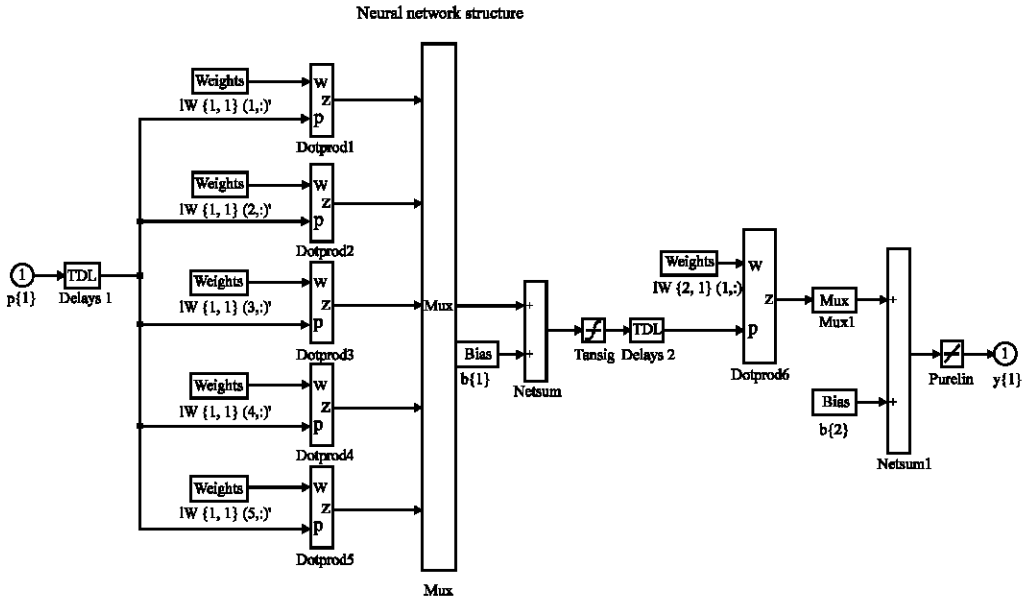

Fig. 3: Neural network structure

controller the output is the angle δ, which is provided to the carrier PWM signal generator. It is important to note that in this case, indirectly controlled converter, there is active and reactive power exchange with the network simultaneously: an error signal is obtained by comparing the reference voltage with the rms voltage measured at the load point. The neural PI controller process the error signal generates the required angle to drive the error to zero, i.e., the load rms voltage is brought back to the reference voltage.

Back propagation algorithm: Back propagation, which is the most training method for a multi-layer feed forward network is shown in Fig. 3. The ANN with back propagation algorithm is trained with 2000 data for voltage. The topology is trained with one input layer, five hidden layers and one output layer with standard purelin, tansigmoid activation function. In Fig. 3, the error data are set as PI vector and V_j^m are the corresponding output vectors, where, m is the number of iterations. The vector V_j^{m-1} is the hidden layer activation function for desired output. The input to ANN is the error and the output is the desired proportional gain K_p and the integral gain K_i for fixing the dc voltage to compensate the voltage disturbances at the load side. The training data for the neural controllers are derived from the appropriate PI controller gain values for a typical load condition. The following steps are used for tuning the parameters neural controller using BP algorithm.

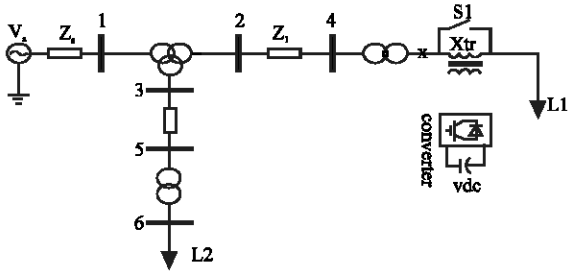

Fig. 4: Single line diagram of test system for DVR

Step 1: Initially all the weights are set to small random value

Step 2: Present an input vector P and a desired output O apply I to the input layer (m = 0) so that $V^0 = 1$

Step 3: For other layers, namely m = 1.....M, forward computation is performed using the Eq. 7:

$$V_i^{(m)} = f\left(\sum_i w_{ij}^m v_j^{m-1}\right) \quad (7)$$

where:

$w_{ij}^m v_j^{m-1}$ = The connection weight from v_j^{m-1} to v_{ij}^m

Step 4: The error is updated making use of the Eq. 7 and fed to the output layer

$$\delta_i^{(m)} = v_i^m (1 - v_i^m)(0_i - v_i^m) \quad (8)$$

Step 5: Then back propagation errors for the preceding layers M-1…1 are calculated using the Eq. 9:

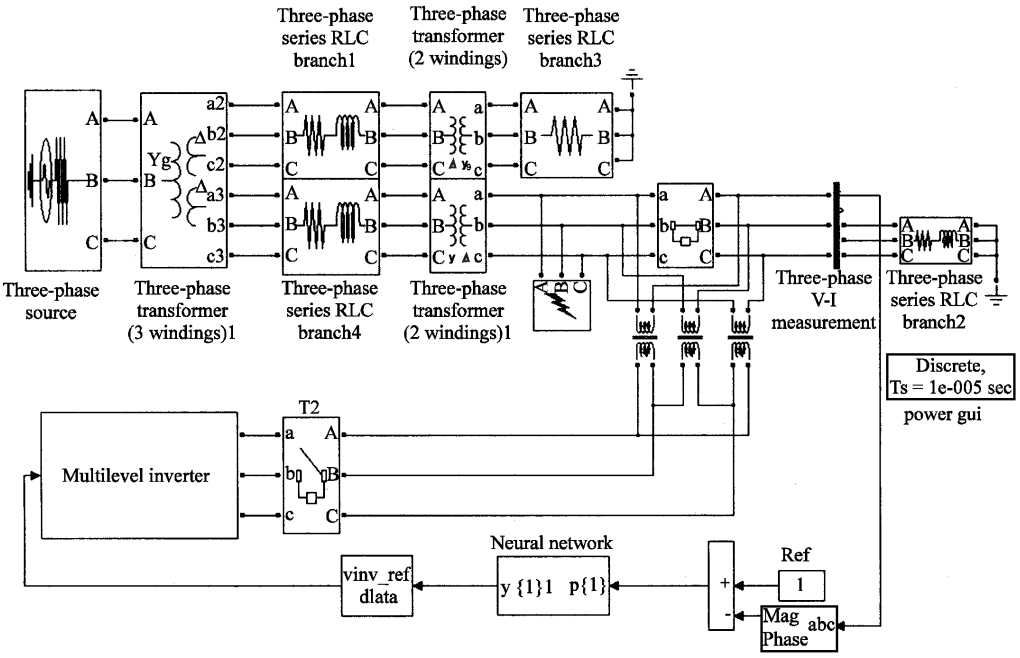

Fig. 5: Simulink model of a DVR test system for voltage sag

$$\delta_i^{(m-1)} = v_i^{m-1}(1 - v_i^{m-1})\sum_j w_{ji}^m \delta_j^m \quad (9)$$

Step 6: Finally, all the weights are adjusted for next iteration and is given by the Eq. 10:

$$w_{ij}^{(m)} = (t+1) = w_{ij}^m (t) + \eta \delta_i^m \; v_j^{(m-1)} \quad (10)$$

where:

η = A gain parameter

Step 7: Repeat and go to step 2 until the desired epoch is achieved. The neural PI controller is shown in Fig. 3.

Test system: Single line diagram of the test system for DVR is shown in Fig. 4 and the test system employed to carry out the simulations for DVR is shown in Fig. 5. Such system is composed by a 13 kV, 50 Hz generation system, feeding two transmission lines through a 3-winding transformer connected in Y/Δ/Δ, 13/115/15 kV. Such transmission lines feed two distribution networks through 2 transformers connected in Δ/Y, 15/11 kV.

To verify the working of a DVR employed to avoid voltage sags during short-circuit, a fault is applied at point X via resistance of 0.4 Ω. Such fault is applied for 100 msec. The capacity of the dc storage is 2.5 kV.

Using facilities available in MATLAB/SIMULINK the DVR is simulated to be in operation only for the duration of the fault as it is expected to be the case in practical situation. Power system bock set for the use with Matlab simulink is based on state-variable analysis and employs either variable or fixed integration-step algorithms. Figure 4 shows the simulink model of DVR and Fig. 5 shows the simulink model of the test system for DVR.

RESULTS AND DISCUSSION

Case 1: Simulation results of voltage during single line to ground fault: The fisrt simulation contains no DVR and a single line to ground fault is applied at point A in Fig. 5 via a fault resistance of 0.2 Ω, during the period 500-900 m sec. The voltage sag at the load point is 30% with respect to the reference voltage as shown in Fig. 6. The second simulation is carried out using the same scenario as above but now with the DVR in operation. The total simulation period is 1100 msec.

When the DVR is in operation the voltage sag is mitigated almost completely and rms voltage at the sensitive load point is maintained at 98% as shown in Fig. 7. The total harmonic distortion is maintained at 0.05% at the load end.

Case 2: Simulation result of voltage interruption during 3 phase fault: The first simulation contains no DVR and three phase fault is applied at point A in Fig. 5, via a fault

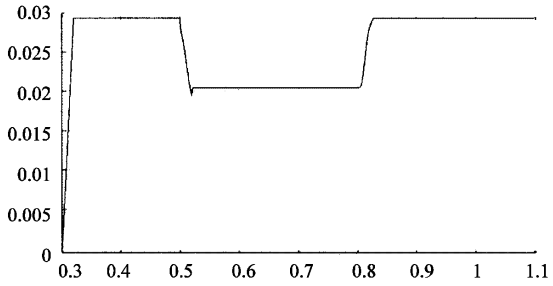

Fig. 6: Load voltage without DVR-voltage sag

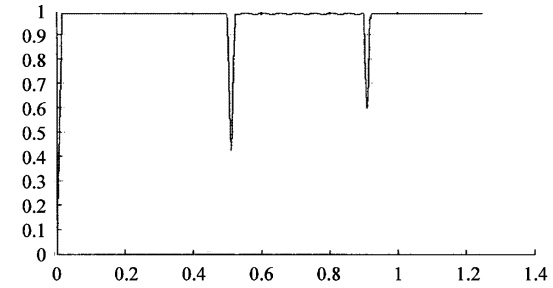

Fig. 7: Load voltage with DVR –mitigation of voltage sag

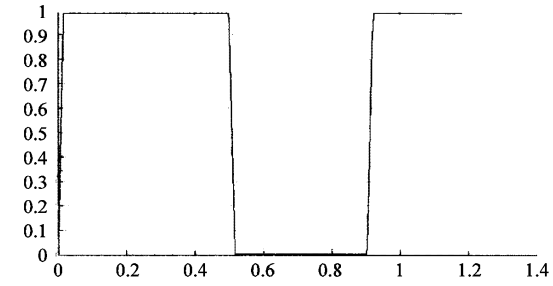

Fig. 8: Load voltage without DVR-voltage interruption

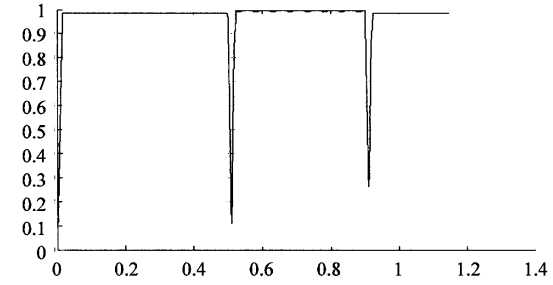

Fig. 9: Load voltage with DVR-mitigation of voltage interruption

resistance of 0.001 Ω, during the period 500-900 msec. The voltage at the load point is 0.05% with respect to the reference voltage as shown in Fig. 8. The 2nd simulation is carried out using the same scenario as above, but with the DVR in operation. The total simulation period is 1400 msec.

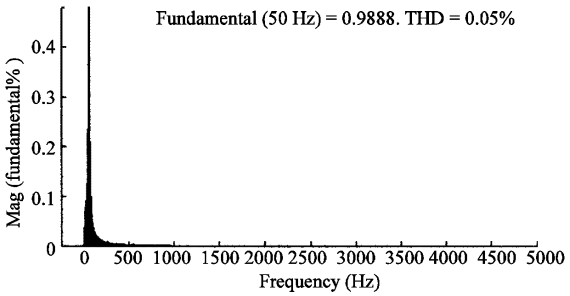

Fig. 10: FFT analysis for load voltage

When DVR is in operation the voltage sag is mitigated almost completely and the rms voltage at the sensitive load point is maintained at 98% as shown in Fig. 9. The total harmonic distortion is maintained at 0.05% at the load end as shown in Fig. 10.

CONCLUSION

This study has presented the power quality problems such as voltage dips, interruptions, consequences and mitigation techniques of custom power electronic device DVR. The design and applications of DVR for voltage sags, interruptions and comprehensive results are presented.

This study presents multilevel cascaded h bridge topology for DVR modeling. The carrier phase shifted modulation method is implemented to control the electronic valves in the 5-level cascaded multilevel inverter. The advantage of using phase shifted modulation scheme is very effective in maintaining load voltage constant.

The neural PI controller added the advantage of limiting the harmonics at the load end. It was observed that with low rating of dc storage high voltage can be injected through cascaded multilevel inverter.

ACKNOWLEDGEMENTS

Researcher express sincere thanks to JNTU college of Engineering of providing necessary support for research.

Researchers also express thanks to VR Siddhartha Academy and EEE department faculty to their help and support.

REFERENCES

Al-Hadidi, H.K. and R.W. Menzies, 2003. Investigation of a cascade multilevel inverter as a STATCOM. IEEE. Power Eng. Soc. General Meeting, Jul, 13-17, 1: 193-193. DOI: 10.1109/PES.2003.1267164.

Buso, S., S. Fasolo, L. Malesani and P. Mattavelli, 2000. A dead-beat adaptive hysteresis current control. IEEE. Trans. Ind. Appl., 36: 1174-1180. DOI: 10.1109/28.855976.

Chan, K., 1998. Technical and performance aspects of a dynamic voltage restorer. Dynamic voltage. Replacing those Missing Cycles IEE Half Day Colloquium, pp: 5/1-525. Digest No. 1998/189.

Corzine, K.A., 2000. A hysteresis current-regulated control for multi-level drives IEEE. Trans. Energy Conv., 15: 169-175. DOI: 10.1109/60.866995.

Fang, M., A.I. Gardiner, A. MacDougall and G.A. Mathieson, 1998. A novel series dynamic voltage restorer for distribution systems. IEEE Proceedings, POWERCON, 18-August, 1: 38-42. DOI: 10.109/ ICPST.1998.728702.

Kazmierkowski, M.P. and L. Malesani, 1998. Current control techniques for three-phase voltage source PWM converters: A survey. IEEE. Trans. Ind. Elect., 45 (5): 691-703. DOI: 10.1109/41.720325.

Loh, P.C., D.G. Holmes, Y. Fukuta and T.A. Lipo, 2002a. Reduced common mode carrier-based modulation strategies for cascaded multilevel inverters. IEEE. 37th IAS Ann. Meeting, 3: 2002-2009. DOI: 10.10.1109/IAS.2002.1043807.

Loh, P.C., G.H. Bode, D.G. Holmes and T.A. Lipo, 2002b. A time-based double-band hysteresis current regulation strategy for single-phase multilevel inverters. IEEE. Trans. Ind. Appl., 36 (3): 883-892. DOI: 10.1109/TIA.2003.810667.

Lai, J.S. and F.Z. Peng, 1995. Multilevel converters: A new breed of power converters. IEEE. Proceedings-Ind. Appl. Soc. Ann. Meeting, August 10, 3: 2348-2356. DOI: 10.1109/IAS.1995.530601.

Marchesoni, M., 1992. High performance current control techniques for applications to multilevel high power voltage source inverters. IEEE. Trans. Power Elect., 7: 189-204.

Rendusara, D.A., E. Cengelci, P.N. Enjeti, V.R. Stefanovic and J.W. Gray, 2000. Analysis of common mode voltage-neutral shift. In Medium Voltage PWM Adjustable Speed Drive (MV-ASD) systems. IEEE. Trans. Power Elect., 15: 1124-1133. DOI: 10.1109/63.892827.

Zhang, H., A.V. Jouanne, S. Dai, A.K. Wallace and F. Wang, 2000. Multilevel inverter modulation schemes to eliminate common-mode voltages. IEEE. Trans. Ind. Appl., 36: 1645-1653. DOI: 10.1109/28.887217.