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Modeling and Simulation of Various Inverter Circuits for Photovoltaic Applications

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Abstract: Buck-boost inverters found widespread applications in grid-connected systems, Uninterruptible Power Supplies (UPS) and other applications requiring voltage regulation above and below the output ac voltage. This study focuses on modeling of the working principles, computer simulation and design consideration of full bridge inverters. About 3 circuit configurations are described with various switching approaches and operation principles where comparison analysis between these circuits is conducted with respect to the output voltage, power, switch voltage and dissipated power. The simulation results stated that the proposed configuration of four-switch inverter with improved stability realized optimum output performances with reduced switching losses. Power electronic simulation platform (PSIM) and Matlab/Simulink platforms are used for simulating the circuit behaviors where applying both platforms in simulation process provides this study with additional tools in selecting the optimum circuit and results comparison.

Key words: AC-DC converters, DC-DC converters, PWM inverters, photovoltaic cells, flyback converters, palestine

INTRODUCTION

In the past century, serious greenhouse effect and environmental pollution caused by overusing fossil fuels have disturbed the balance of global climate. High rate gas emissions mainly of CO_2 in the atmosphere have affected global surface temperatures which increase at a rate 0.6°C/century (Hodge, 2010; Chuang and Ke, 2008). Reducing the emissions of exhausted gases can be realized by using so called zero-emission renewable energy sources.

These sources have been rapidly developed in the past 2 decades mainly the applications of solar energy throughout using Photovoltaic (PV) cells which are clean, quiet and an efficient method for generating electricity. The PV power system has been widely used in power processing technologies such as solar power generation for grid connection; solar vehicle constriction, battery charger, water pump, satellite power system, traffic signals, electronic signs and so on (Bull, 2001; Rahman, 2003; Tseng *et al*., 2008). There are various electronics conversion systems and conversion topologies; one of these is called flyback based converters.

This kind converter found widespread applications due to its construction varieties starting from simple design to complicated design in additional to existing acceptable efficiency. Consequently, there are many research works on how to improve the efficiency of such converters (Hwu *et al*., 2008; Rouger *et al*., 2008; Weng and Xing, 2004; Lin *et al*., 2006; Jinno *et al*., 2003) for powering Light Emitted Diodes (LED) using high-efficiency flyback converter, fully integrated self driving converter, dual transformer, synchronous rectification and non-dissipated snubber circuits.

The resulting circuits are complicated due to the specific components required to drive the half-bridge switches in the active voltage clamping circuits. DC-DC and DC-AC converter circuits have huge configuration spectrum depending on the input/output requirements and operation condition (Hart, 2010; Kanaan and Al-Haddad, 2005; Jovcic, 2009). About three-switch flyback converter presents, one of most popular circuit due to simple design, acceptable efficiency and reduced number of components.

Here in after study proposes modified conversion circuit with various chopping switches aiming at realizing enhanced output performances and further elements reduction.

MATERIALS AND METHODS

Figure 1 shown Photovoltaic (PV) cells energized load circuit in both on-line and off-line grid connected mode where the PV cells/arrays can be connected directly to the inverter in daytime mode and charging the batteries while during the nighttime mode the batteries energized the load

throughout the inverter circuit. This configuration has several merits such as reducing the battery operation time, better efficiency and better solar energy utilization. In the hereinafter descriptions, the PV source is described during the daytime operation and represented by two batteries with voltage of V_{pv1} and V_{pv2}.

Circuit configurations: Several circuit configurations are discussed aiming at studying the behaviors of the output voltage, load current, boost current, transistor current, switching losses and output power. These circuits are:

- Four-switch inverter configuration-circuit 1
- Two-switch inverter configuration-circuit 2
- Four-switch modified inverter configuration-circuit 3

Four-switch inverter configuration-circuit 1: Figure 2 shown single inverter with four transistorized switches built in PSIM environment where, the input voltage is supplied by PV panel and the output voltage is obtained by using Sinusoidal Pulse Width Modulation (SPWM) technique with purpose minimizing the voltage harmonics and ripples.

Principle of operation: About 2 operation modes can be described during single modulation period T_o as follows:

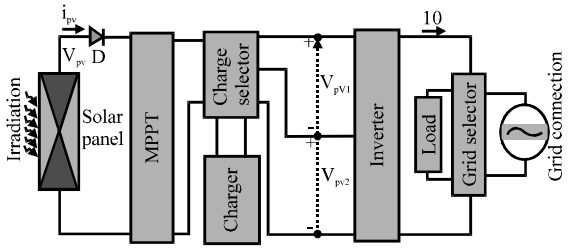

Fig. 1: PV circuit with inverter energized grid/load connection

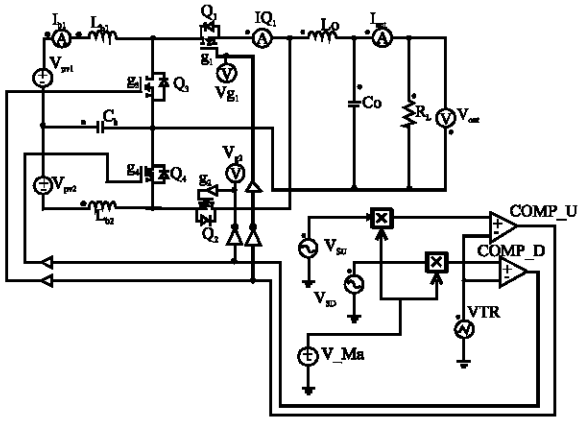

Fig. 2: Four-switch inverter-circuit 1

Mode 1: Transistor switches Q_1 and Q_3 operates in complementary mode for positive half cycle of the output voltage while Q_2 and Q_4 operates for the negative half cycle. $L_{b1\text{-}b2}$ and C_b presents boost elements and C_o presents low-pass voltage filter. When Q_3 is switched on the inductor L_{b1} accumulates the source voltage V_{pv1} and the current oscillates with ringing frequency that depends on L_{b1} and C_b. When Q_1 is switched on during the rest of the half modulation period $T_o/2$, the stored energy is transferred to the load. The equivalent circuits for both modes are shown on Fig. 3 and 4 while the obtained mathematical model is derived as follows:

Mathematical modeling: During the interval $(0 \le t \le D.T_o/2)$ where, Q_3 = on and Q_1 = off according to KVL, the voltage balance equations are:

$$V_{pv1} = L_{b1}\frac{di_{b1}(t)}{dt} + \frac{1}{C_b}\int i_{b1}(t).dt + V_{cb}(0)$$
$$V_{co}(0) = R_L.i_o(t) - \frac{1}{C_o}\int i_o(t).dt \quad (1)$$

Equation 1 in matrix form:

$$\begin{vmatrix} \frac{(V_{pv1} - V_{cb}(0))}{S} + L_{b1}.I_{b1}(0) \\ \frac{V_{co}(0)}{S} \end{vmatrix} = \begin{vmatrix} L_{b1}.S + \frac{1}{C_b.S} & 0 \\ R_L & -(R_L + \frac{1}{C_o.S}) \end{vmatrix} \begin{vmatrix} I_{b1}(S) \\ I_{co}(S) \end{vmatrix} \quad (2)$$

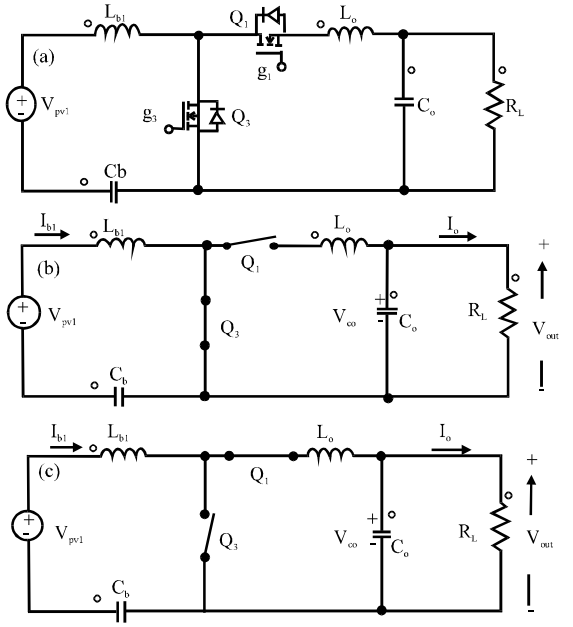

Fig. 3: Circuit configuration for mode 1 a) circuit configuration b) the equivalent circuit when Q_3 is switched on c) the equivalent circuit when Q_1 is switched on

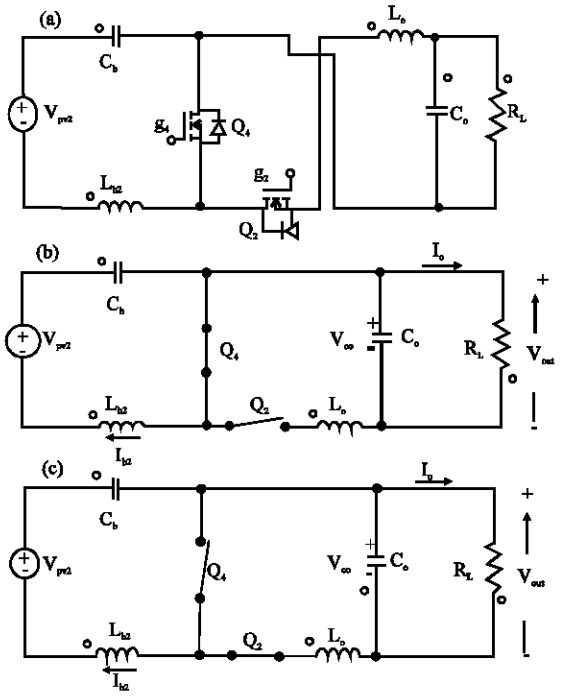

Fig. 4: Circuit configuration for mode 2: a) circuit configuration; b) the equivalent circuit when Q_4 is switched on and c) the equivalent circuit when Q_1 is switched on

The boost current during this mode based on Eq. 2 is:

$$i_{b1}(t) = I_{bm1}.\sin\omega_r.t + I_{b1}(0).\cos\omega_r.t$$
$$i_o(t) = \frac{V_{co}(0)}{R_L} e^{-t/\tau} \quad (3)$$

Where:

$$I_{bm1} = (V_{D1} - V_{cb}(0))\sqrt{\frac{C_b}{L_{b1}}}$$
$$\omega_r = 1/\sqrt{L_{b1}.C_b}; \quad \tau = R_L.C_o$$

Where:

D = The duty cycle
T_o = The modulation period with chopping frequency f_S, ($T_o = 1/f_S$)

The transistor current $i_{Q3}(t) = i_{b1}(t)$. During the interval ($D.T_o/2 < t \leq T_o/2$ where, Q_1 = on and Q_3 = off, the voltage balance equations according to this mode are:

$$V_{pv1} = R_L.i_o'(t) + L_b\frac{di_{b1}'(t)}{dt} + \frac{1}{C_b}\int i_{b1}'(t).dt + V_{cb}'(0)$$
$$Vc_o'(0) = R_L.i_o'(t) - \frac{1}{C_o}\int i_{co}'(t).dt \quad (4)$$
$$i_{b1}' = i_{co}' + i_o'$$

Equation 4 in matrix form:

$$\begin{vmatrix} \frac{(V_{pv1} - V_{cb}'(0))}{S} + L_b.I_{b1}'(0) \\ \frac{V_{co}'(0)}{S} \end{vmatrix} = \begin{vmatrix} L_{b1}.S + \frac{1}{C_b.S} + R_L & -R_L \\ R_L & -(R_L + \frac{1}{C_o.S}) \end{vmatrix} \begin{vmatrix} I_{b1}'(S) \\ I_{co}'(S) \end{vmatrix} \quad (5)$$

where, V_{pv1}, $V_{ccb}'(0)$ and $Vc_o'(0)$ are PV voltage and initial voltages of existing capacitors, respectively at $t = D.T_o/2$, R_L is the load resistance, L_{b1} and L_{b2} are the boost inductances and C_o is low-pass filter. For symmetrical circuit purposes usually $L_b = L_{b1} + L_o = L_{b2} + L_o$. With purpose further simplification of the derived mathematical model, the capacitor charging current is negligible, therefore, the boost current flowing through the transistor Q_1 will be the load current $i_o(t) = i_{co}(t) + i_{b1}'(t) \cong i_{b1}'(t)$ that can be expressed as:

$$i_{bl}'(t) = \frac{Cb}{\sqrt{\delta^2 - 4}} \left(\begin{array}{l} \frac{V_{pvl} - V_{cb}'(0)}{\omega r}\left(e^{Slt} + e^{S2t}\right) + \\ \frac{L_b.I_{b1}'(0)}{2} \\ \left[\left(-\delta + \sqrt{\delta^2 - 1}\right).e^{Slt} + \right. \\ \left.\left(-\delta + \sqrt{\delta^2 - 1}\right).e^{Slt}\right] \end{array} \right) \quad (6)$$

Where:

δ = The damping factor
ω_r = The angular velocity
S_1, S_2 = The Laplace roots
I_{co} = The capacitor current
$I_{b1'}$ = The boost current

$$\delta = RL\sqrt{\frac{C_b}{L_b}}; \quad \omega_r = \frac{1}{\sqrt{L_b.C_b}}$$
$$S_1 = \frac{-\delta + \sqrt{\delta^2 - 4}}{2}\omega_r; \quad S_2 = \frac{-\delta - \sqrt{\delta^2 - 4}}{2}\omega_r \quad (7)$$

Realizing over damping condition for the inverter current requires setting:

$$\delta^2 > 4, \Rightarrow R_L > 4.\sqrt{L_b/C_b} \quad (8)$$

The initial current at $I_{b1}'(0)$ can be determined by setting the current I_{b1} ($t_1 = DT_o/2$) as follows:

$$i_{b1}'(0) = i_{b1}(t_1) = I_{bm1}.\sin(\omega_r.t_1) + I_{b1}(0).\cos(\omega_r.t_1) \quad (9)$$

The initial current $I_{b1}(0)$ is determined from the inverter current flows in the circuit according to mode 2 at instant $t_2 = T_o$ where the current will be:

$$i_{b1}(0) = i_{b1}'(t^2) = \frac{C_b}{\sqrt{\delta^2-4}}\left(\frac{\left(V_{pv1}-V_{cb}'(0)\right)}{\omega r}\left(e^{S1t2}+e^{S2t2}\right) + \frac{L_b.I_{b1}'(0)}{2}\left[\left(-\delta+\sqrt{\delta^2-1}\right).e^{S1t2} + \left(-\delta+\sqrt{\delta^2-1}\right).e^{S1t2}\right]\right) \quad (10)$$

The boundary conditions for current continuous mode can be determined from Eq. 10 by setting $i_{b1}(0) = i_{b1}(T_o) = 0$.

Mode 2: Transistor switches Q_2 and Q_4 operates in complementary mode for negative half cycle of the output voltage. The equivalent circuit for this mode is illustrated in Fig. 4. The derived equations for mode 1 are still valid for mode 2 whereas $i_{Q2}(t) = i_{b1}'(t)$ and $i_o(t) = i_{Q4}(t) = i_{b1}(t)$ therefore, they will not be derived furthermore. The rms load voltage V_{rms} can be expressed as:

$$V_{rms} = \left[\frac{1}{T_s}\int_0^{T_s}(R_L * i_o(t))^2\,dt\right]^{1/2} = \left[\frac{1}{T_s}\int_0^{T}\left(\frac{C_b * R_L}{\sqrt{\delta^2-4}}\left(\frac{\left(Vpv1-V_{cb}'(0)\right)}{\omega r}\left(e^{S1t}+e^{S2t}\right) + \frac{Lb.b1'(0)}{2}\left[\left(-\delta+\sqrt{\delta^2-1}\right)e^{S1t} + \left(-\delta+\sqrt{\delta^2-1}\right)e^{S1t}\right]\right)\right)^2 dt\right]^{1/2} \quad (11)$$

where, T_s is the period of inverted voltage. The transistor losses P_{Q1}, P_{Q2}, P_{Q3} and P_{Q4} can be expressed as follows:

$$P_{Q\_mode1} = \left[f_s\left(\int_0^{D.To}\left(V_{Q1\_on}.i_{Q1(t)}\right)^2 dt + \int_{D.To}^{To}\left(V_{Q1\_off}.i_{Q1\_off(t)}\right)^2 dt\right)\right]^{1/2}$$

$$P_{Q1} = P_{Q2} = P_{Q\,mode1}$$

$$P_{Q\_mode2} = \left[f_s\left(\int_0^{D.To}\left(V_{Q3\_off}.i_{Q3\_off(t)}\right)^2 dt + \int_{D.To}^{To}\left(V_{Q3\_on}.i_{Q3(t)}\right)^2 dt\right)\right]^{1/2} \quad (12)$$

$$P_{Q3} = P_{Q4} = P_{Q\,mode2}$$

where, V_{Q1-on}, V_{Q1-off}, V_{Q3-on}, V_{Q3-off} transistor voltge during on-state and off-state conduction respectively for Q_1 and Q_3, i_{Q1-off}, i_{Q3-off} are the transistor current during off-state conduction, respectively for Q_1 and Q_3. The load power expressed in rms value P_{rms} can be expressed as:

$$P_{rms} = \left[\frac{1}{T_s}\int_0^{T_s}(V_o(t) * i_o(t))^2\,dt\right]^{1/2}. \quad (13)$$

RESULTS AND DISCUSSION

Figure 2 shows that inverter is simulated using PSIM software and Matlab/Simulink platforms with circuit's data shown in Table 1. The obtained simulation results are shown that Fig. 5 for both cases with and without boost capacitor C_b where, it is shown that existing of boost capacitor reshape the output voltage. While removing C_b by shorting it improves the shape of the output voltage and reduces the transistor losses as shown in Fig 5c and d. The observed improvement is achieved on the expense of the low magnitude of this voltage and low output power as shown in Fig 5e and f.

Improvement of the circuit performances: The main disadvantages are shown in Fig 2, circuit are low output voltage with heavy harmonic content and high huge transistor losses therefore, overcoming these drawbacks can be achieved by proposing modified circuit operation mode with predetermined sequence as follows:

Mode 1: Q_1, Q_3 operates in complementary sequence while Q_2 is maintain in switched-on state.

Mode 2: Q_2, Q_4 operates in complementary sequence while Q_1 is maintain in switched-on state. The equivalent circuits of the modified operation are shown in Fig. 6 for 2 operation modes with time interval of $D.T_o/2$.

Mathematical modeling: During the interval ($0 \le t \le D.T_o/2$) where Q_3 = on, Q_1 = off and Q_2 = on, the boost current $i_{b1}(t)$ is the same as that expression derived in Eq. 3 therefore, $i_{Q1}(t) = i_{b1}(t)$ and $i_{Q3}(t) = i_{b1}(t)$. While $i_{b2}(t)$ has complicated character with expression:

Table 1: Data specifications of simulated circuits

V_{PV1} (V)	R_L (Ω)	f_S (kHz)	V_{ref} (V)
5..30V	10	10	1.25
C_b, µF	L_{b1}, µH	L_{b2}, µH	V_{tm},V
50	200	200	3
C_o, µF	L_o, mH	C_{S1}, µF	C_{S2}, µF
200	20	10	100
C_b, µF	L_{G1}, µH	Tr	$V_{dc1}=V_{dc2}$
20	100	1:2	20
Qp,Q1,Q2,Q3,Q4,Q5,Q6		D1,D2, Ds1, Ds2	
IGBTs		Fast switching diodes	

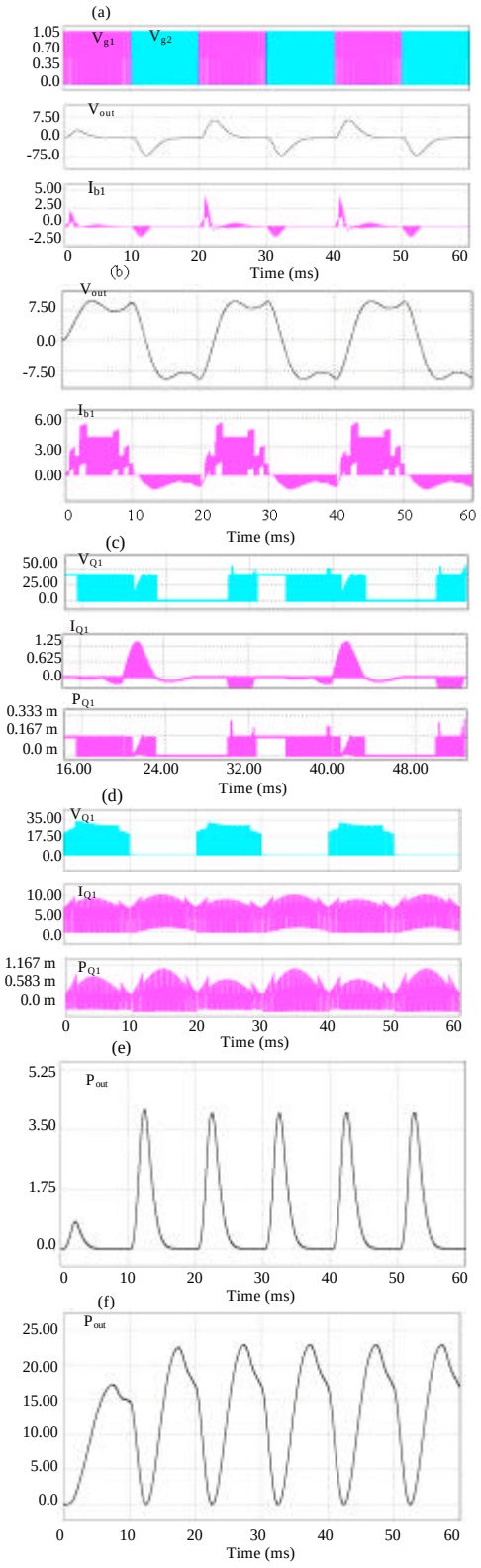

Fig. 5: Inverter circuit waveforms: a) Circuit waveforms and b) C_b, c) C_b, d) C_b, e) C_b, f) C_b

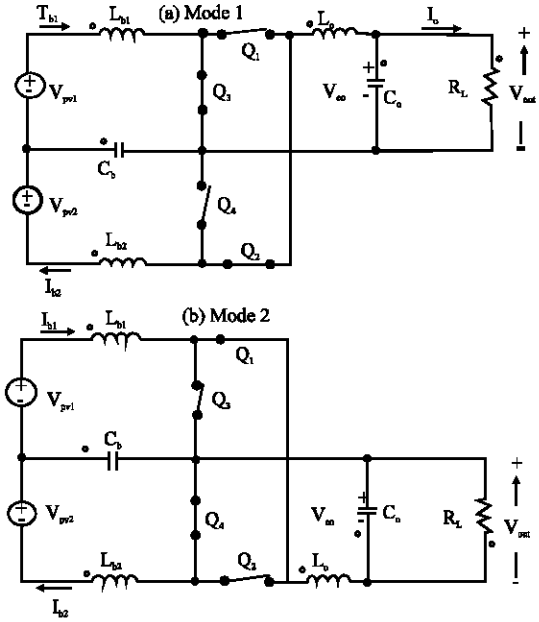

Fig. 6: Equivalent circuits of modification opertaion

$$i_{b2}(t) = \frac{V_T}{L_b}\cos\omega t + \frac{V_T}{\omega L_b}\left(\frac{1}{\omega^2 - \omega_T{}^2}\right)\left[\frac{1}{\omega r}\sin\omega t - \frac{1}{\omega}\sin\omega t\right] + I_{b2}(0)\sqrt{\frac{L_b}{C_b}}\sin\omega t.\cos\omega t \quad (14)$$

Where:

$$V_{pv} = V_{pv1} = V_{pv2}$$
$$V_T = V_{pv} - V_{cb}(0) + L_T.I_{b2}(0)$$
$$L_b = L_o + L_{b1} = L_o + L_{b2} \quad (15)$$
$$\omega = \frac{1}{\sqrt{L_{b1}.C_b}};$$

For this mode, the transistor current $i_{Q2}(t) = i_{b2}(t)$. During the interval $(D.T_o/2 \le t \le T_o/2)$ where Q_3 = off, Q_1 = on and Q_2 = on.

For simplification purposes when deriving the current equation, the effect of C_o and the initial values of the circuit currents are neglected therefore, the boost current can be expressed as follows:

$$i_{b1}(t) = i_{b2}(t) = \frac{V_{pv}}{L_b}t \quad (16)$$

where, $V_{pv} = V_{pv1} = V_{pv2}$ is the PV voltage corresponds to MPPT voltage. Figure 7 shows the simulation results of the operation sequence of inverter transistors, transistor

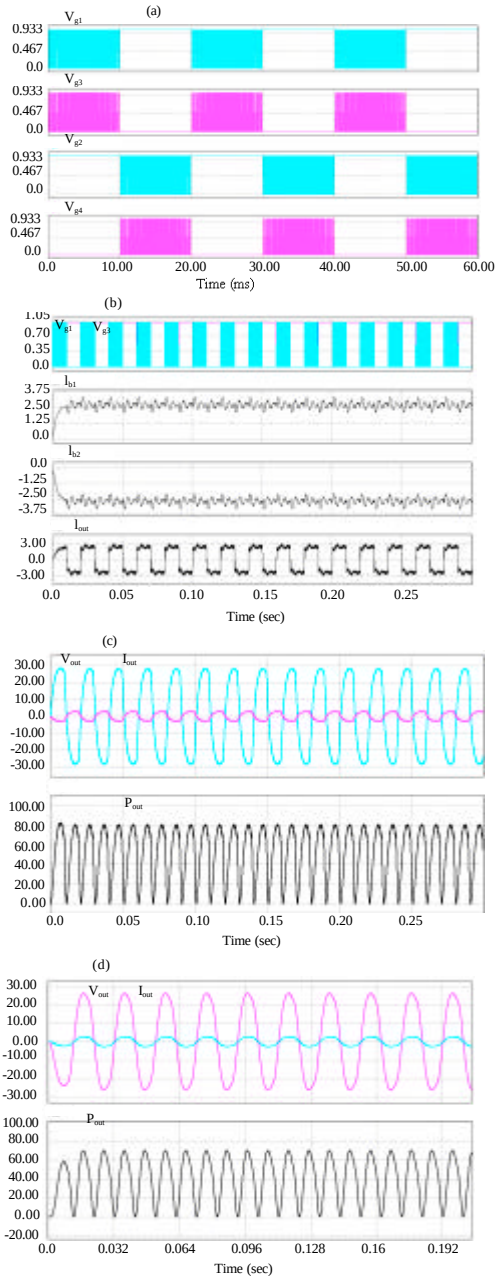

Fig. 7: Modification circuit waveform: a) Transistors switching sequence; b) i_{Q1} and i_{Q2} without Co.; c) Output performances without Co.; d) Output performances with Co.

current of Q_1 and Q_2, output voltage and current and load power. It is shown that the sinusoidal waveforms of the output voltage and current can be realized by connecting low-pass filter C_o across the load.

According to simulated results shows in Table 2 the effect of connecting both C_b and C_o cause significant

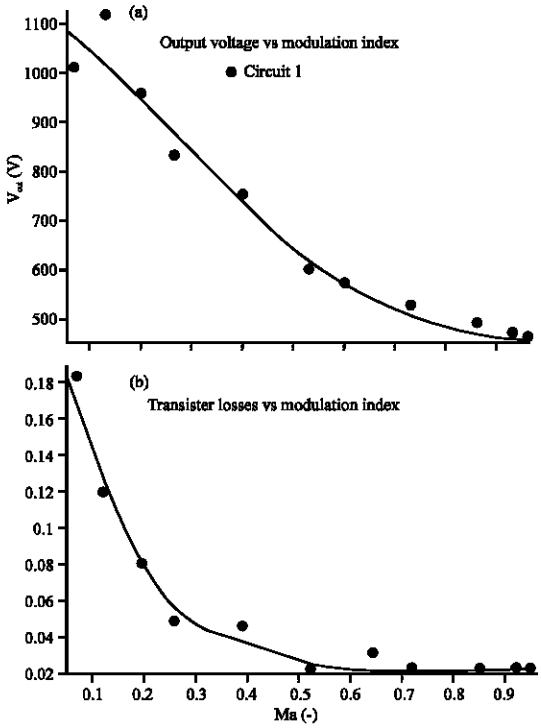

Fig. 8: RMS output voltage of interver circuit 1: a) Output voltage V_{rms} -circuit1 and b) Transistor losses PQ1 circuit 1

Table 2: Output performance of circuit 2

Status/Quantities	With C_b	Without C_b
With C_o		
V_{rms}, V	19.93	13.53
P_{rms}, W	46.48	21.26
V_{dc}, V	-0.35	-0.031
V_{Q1}, V	156.15	130.32
I_{Q1}, A	1.891	1.42
P_{Q1}, W	0.0066	0.0032
Without C_o		
V_{rms}, V	17.15	11.15
P_{rms}, W	32.85	13.86
V_{dc}, V	0.042	-0.032
V_{Q1}, V	158.1	131.51
I_{Q1}, A	1.53	1.14
P_{Q1}, W	0.0078	0.0035

increase in the load power up to 300% while the transistor looses increases to around 200% which justified the connection of such elements.

The output voltage of the inverter can be regulated by varying the duty cycle within safety operation limits ($D_{min} \leq D \leq D_{max}$).

Figure 8 shows the output voltage and transistor losses variation with respect to the modulation index M_a where it is shown that V_{rsm} and P_{Q1} changes rapidly at low values of modulation index which destabilize the circuit operating. Furthermore, the minimum inverter voltage

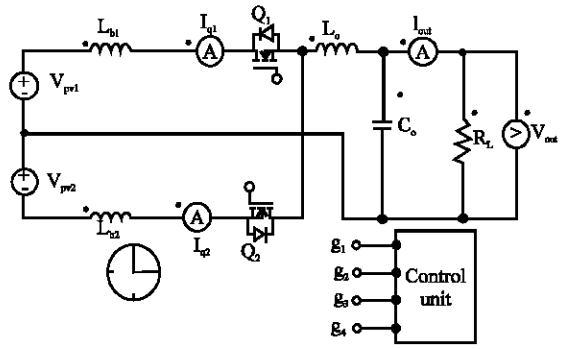

Fig. 9: Two-switch inverter-circuit 2

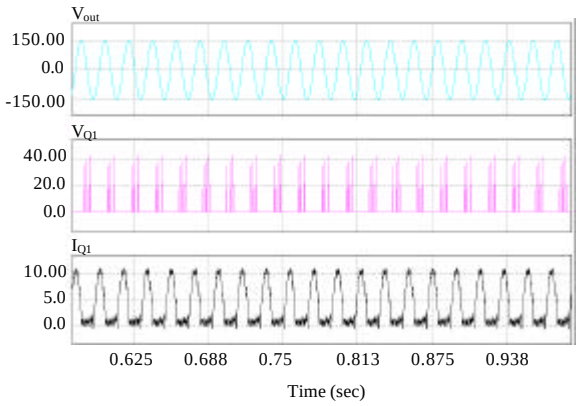

Fig. 10: Main waveform of circuit 2

is the input PV voltage while D varies in the whole control range from 0-1 which gives this circuit more advantages comparing with the conventional inverter circuits. The main disadvantage of this circuit is the existing of high harmonic content in the transistor current which causes an excess of heat in these transistors.

Two-switch inverter configuration (circuit 2): Figure 9 shows two-switche inverter circuit with minimized number of circuit elements and simplified control circuit where the transistor's current $i_{Q1}(t) = i_{Q2}(t) = i_{b1}(t)$ can be expressed as:

$$i_{b1(t)} = i_{b2\ (t)} = \frac{V_{pv}}{R_L}(1 - e^{-t/\tau}) + I_{b1}(0)e^{-t/\tau} \qquad (17)$$

The output voltage and current are shown in Fig. 10 where, it is shown that despite the significant enhancement in the character of the output performances the transistor current I_{Q1} still enough high to overheat the device and causes eventually damage.

Furthermore, the rapidly change of transistor voltage V_{Q1} affects the transistor stability and may cause great tension on the transistor junctions and fast aging. Avoiding this, status can be achieved by proposing the circuit.

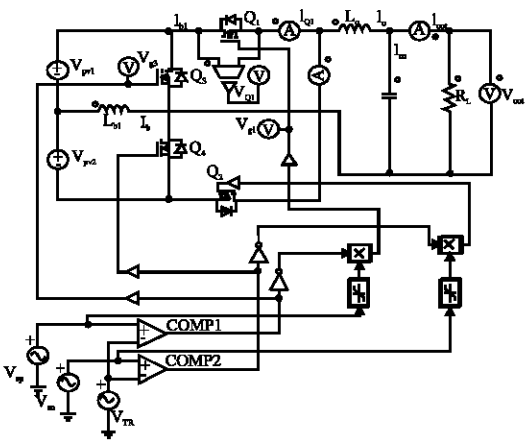

Fig. 11: Four-switch modified inverter-circuit 3

Four-switch modofied inverter configuration with improved stability (circuit 3): Figure 11 shows such a circuit where the drawbacks of discussed in previous topic/circuit 2 are completely eliminated. The boost currents according to proposed configuration are as follows.

During the interval $(0 \le t \le D.T_o/2)$ where, Q_1 = off, Q_2 = on and Q_3 = on, the transistor current $i_{Q3}(t)$, boost current $i_{b1}(t)$ and $i_{Q2}(t)$ flows in the circuit can be expressed as:

$$\begin{aligned} i_{Q3(t)} &= i_{b1(t)} - i_{Q2(t)} \\ i_{b1(t)} &= \frac{V_{pv}}{L_{b1}}t \\ i_{Q2(t)} &= -\frac{V_{pv}.e^{-t/2\tau}}{L_b\tau\sqrt{K}\omega^2}\left(\frac{1}{2\tau}\sin\sqrt{K}t + \sqrt{K}\cos\sqrt{K}t\right) \end{aligned} \qquad (18)$$

Where:

$$\begin{aligned} \omega &= \frac{1}{\sqrt{L_{b1}.C_o}};\ \tau = R_L.C_O \\ K &= \omega^2 - \frac{1}{4\tau^2};\ K > 1;\ \Rightarrow C_o > \frac{L_b}{4R_L^2}. \end{aligned} \qquad (19)$$

During the interval $(D.T_o/2 \le t \le T_o/2)$ where Q_1 = on, Q_2 = on and Q_3 = off, the circuit currents are $i_{Q1'}(t)$ and $i_{b1'}(t)$ have the following expressions:

$$\begin{aligned} i_{Lo'(t)} &= i_{b1'(t)} = i_{Q1'(t)} + i_{Q2'(t)} \\ i_{b1'(t)} &= \frac{V_{pv}}{\sqrt{K}L_b}e^{-t/2\tau}\left(\frac{2\tau^2\omega^2 - 1}{2\tau^2\omega^2}\right)\sin\sqrt{K}t + \\ &\frac{V_{pv}}{\tau\omega^2 L_b}e^{-t/2\tau}\cos\sqrt{K}t \end{aligned} \qquad (20)$$

The obtained simulation results are shown in Fig. 12 where, it is shown that the load voltage and current have sinusoidal character, the transistor has stabilized

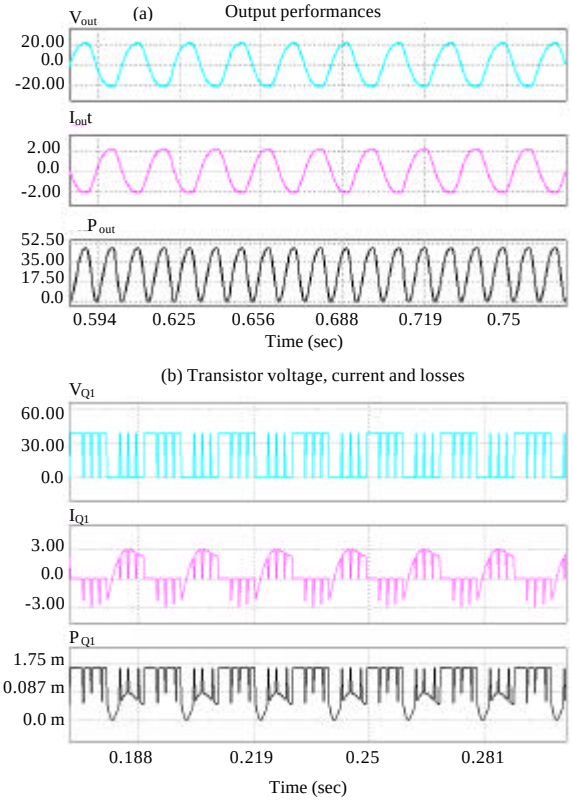

Fig. 12: Main waveform of circuit 3: a) Output performances and b) Transistor voltage, current and losses

Table 3: Output performance of circuit 3

Status/Quantities	With L_b	Without L_b
With C_o		
V_{rms},V	16.135	15.16
P_{rms},W	32.91	31.6
V_{dc}, V	0.031	0.047
V_{Q1}, V	28.26	27.44
I_{Q1}, A	1.59	1.56
P_{Q1}, W	0.00012	0.00011
Without C_o		
V_{rms},V	16.02	11.26
P_{rms},W	32.54	16.56
V_{dc}, V	0.014	0.013
V_{Q1}, V	26.67	26.42
I_{Q1}, A	0.81	0.798
P_{Q1}, W	0.000103	100 10^{-6}

parameters with respect to its voltage and current due to realized return current path leading to slightly change in switch status which in turn reduces the commutation voltage.

Table 3 shows the main inverter output parameter and transistor losses where its shown that the effect of low-pass filter is negligible therefore, it can be removed with purpose reducing the circuit elements and avoiding capacitor rush currents. The Matlab/Simulink model and PWM control model of circuit 3 are shown in

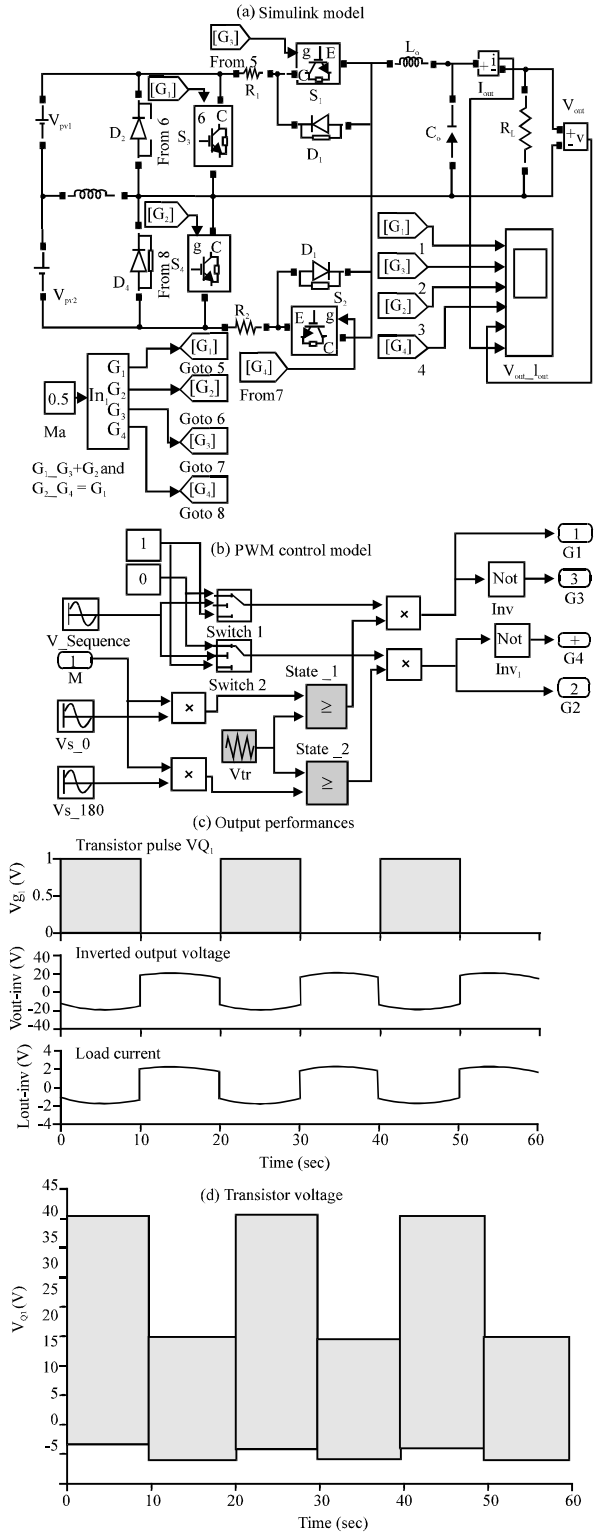

Fig. 13: Simulink results for circuit 3

Fig 13a, b while the main circuit waveforms and transistor voltage are shown in Fig. 13c, d. Comparison analysis

Table 4: Comparison analysis

Status/Quantities	With C_b (circuit 1)	With L_b (circuit 3)
With C_o		
V_{rms},V	19.93	16.135
P_{rms},W	46.48	32.91
V_{dc}, V	-0.35	0.031
V_{Q1}, V	156.15	28.26
I_{Q1}, A	1.891	1.59
P_{Q1}, W	0.0066	0.00012
Without C_o		
V_{rms},V	17.15	16.02
P_{rms},W	32.85	32.54
V_{dc}, V	0.042	0.014
V_{Q1}, V	158.1	26.67
I_{Q1}, A	1.53	0.81
P_{Q1}, W	0.0078	0.000103

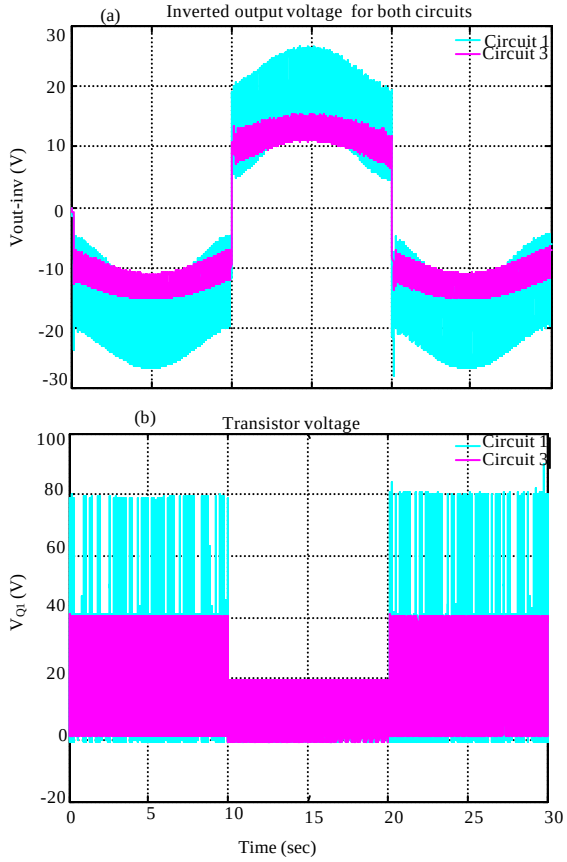

Fig. 14: Simulink resulsts for circuit 1 and 3

can be conducted between the 2 main circuits shown in Fig. 2 and 11 with respect to the output voltage, power and transistor switching parameters mainly transistor voltage, current and switching losses. Table 4 shows the obtained simulation results at modulation index of M_a = 0.8 while Fig. 14 shows the output voltage and transistor voltage for these circuits, respectively. The obtained simulation results according to Table 4 shows that maximum output power could be obtained when both boost and low-pass capacitors are added to the circuit. In this case the transistor must handle high blocking

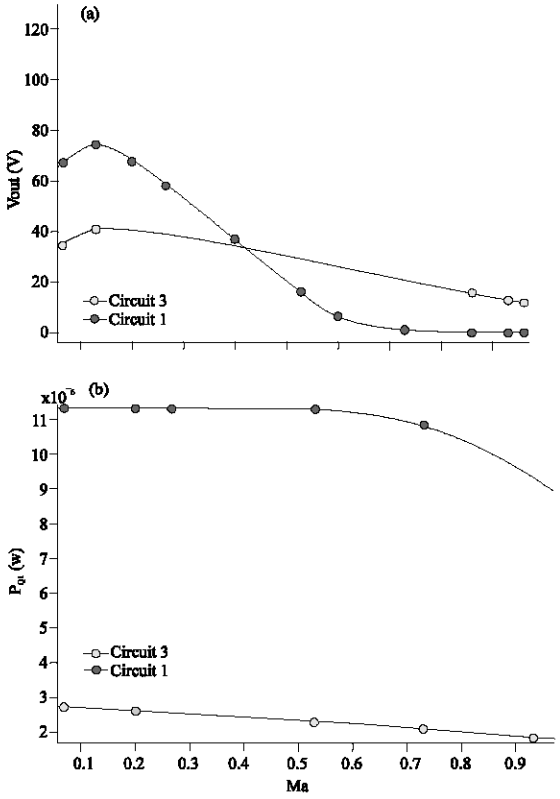

Fig. 15: Simulink results for circuit 1 and 3

voltage. On other hand, replacing C_b by boost inductor L_b reduces the rms output power in additional to significant decrease in the transistor blocking voltage. Figure 15 shows how the output voltage, transistor losses varies with respect to modulation index for both circuits where it is shown that the output voltage, transistor voltage and switching losses of circuit1 are greatly high comparing with that of circuit 3 therefore, circuit 3 presents optimized solution with respect to both transistor and output performances. Further, enhancement in the output performances can be achieved by using flyback-based inverter that combines bridge inverter with buck-boost converter. This approach is going to be described in future research.

CONCLUSION

Several circuit configurations have been studied with respect to the output voltage, load current, transistor current and losses where the following conclusion can be stated:

- Mathematical model for the main circuit configuration (circuit1) is derived with assigned conditions for realizing continuous current mode

- The combination of boost and low-pass filter in additional to propose switching sequence causes output voltage increase up to 70% but on the expense of high voltage across the switching devices in additional to observed high current ripples. Applying the configuration of circuit2 causes insignificant enhancement in the output performances
- Avoiding the existence of high voltage across the device with reduced current ripples can be achieved by proposing the configuration of circuit 3 where the boost capacitor is replaced by boost inductor. In the mean time existing of such inductance limits the increase in the output voltage to be within 40%
- The circuit stability and loss reduction are significantly enhanced according to the obtained results of circuit 3 built in Matlab/Simulink environment where the transistor voltage and yield losses are within the normal range
- Further enhancement in the output performances can be achieved by applying modified PV buck-boost circuit in combination with flyback inverter. This task will be the object of future study

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