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Reusable Network on Chip Design

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Abstract: Researchers present a Fault Tolerant Hardware Routing Model using reusability technique for the Network on Chips (NOC) during faulty conditions to enable the router to transmit the packets effectively without any loss. The network has been designed for 3×3 and 4×4. The faults are mainly injected due to transients in the real world which affects the routing path and they are modeled as digital faults. The reliability of the design has been found out to be 100% for bidirectional design of NOC routers at a frequency of 500 MHz.

Key words: Fault tolerant design, network on chips, routing table, model, path

INTRODUCTION

As the technology shrinks down, more complex chips have to be embedded into a single processor and the design parameters have to be designed so that the communication parameters meets the increasing bandwidth for many complex designs. With the current trends in communication, NOC finds its advantage in on chip bus based communication systems with the mechanism of packet forwarding (Zhang *et al*., 2013).

With the increasing high end communication to the third parties, the resources needed to implement the design for the bandwidth requirement has to be met with restrictions to satisfy Quality of Service (QOS). In order to obtain high speed communication for long range, hardware accelerators like FPGAs are being used in real time processing to obtain high through communication and low power trade off (Majumder *et al*., 2013). This method allows reconfiguration by the user as many processors are being connected from the central computer system to the host for the data to be transferred through a bus connection. This type of reconfiguration provides direct access to the peripheral devices which are connected to the neighboring host. In order to obtain congestion free routing for streaming applications which requires more bandwidth, an efficient switching scheme has to be developed which will reduce the delay in traffic energized applications. Circuit switching in NOC provides efficient routing by identifying the shortest path and is best used in intra routing in static manner block network resources. But this method provides a delay in establishing the connection and results in inefficient resource utilization (Talwar and Amrutur, 2013).

Network on chip: As the technology shrinks rapidly in nanometer, several issues have to be taken in the design relating to area and speed. As scalable bandwidth is the current trend in the network technology which is adopted to communicate with the on chip technology, necessary configurations have to be designed for the support of efficient on chip communication like switching logic, Routing algorithm and packet size which are the main components of NOC. The speed of NOC mainly depends on its wiring delay which the main aspect for intra communication systems. To overcome this problem, the hardwired NOC is proposed (Elrabaa and Bouhraoua, 2011). The components and design of NOC are shown in study.

Router: The main objective of the router is to forward the packets to the destination point as given by the control signal which directs the packets to East, West, North and South directions as shown in the Fig. 1. The data packets

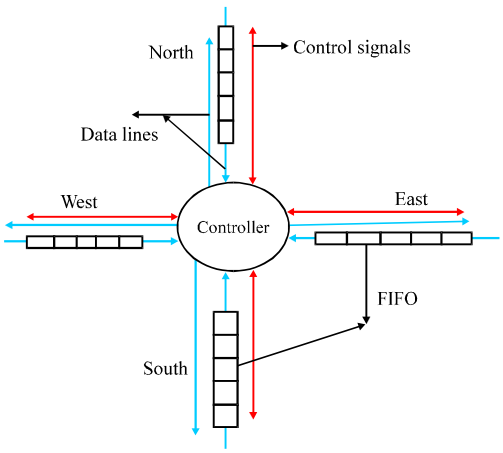

Fig. 1: Router design

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are stored in FIFO which acts as a temporary buffer and depending upon the control signal, it provides a handshake between the source and the destination. Each packet contains the destination address which determines the direction for transmitting the data, the control bits which decodes the address into 2D co-ordinates for the destination. The data packets sent in NOC are passed through queue which has storage registers for storing and reading the data in a serial manner. The messages which are sent into the FIFO are used by the router control to monitor the direction of the destination of the packets. Its main objective is to find the FIFO which is not full so that so that the packets will be sent to the input FIFO point.

Arbiter: The objective of the arbiter is to decide the packet which has to be sent to the output. It consists of a multiplexer and a finite state machine which follows Round Robin technique which decides the data to be sent out to the output end as shown in Fig. 2. As 4 data stream are coming in parallel to the input line in East, West, North and South. The data will be written into the FIFO in a particular direction when it is coming before the next direction. Once the particular register becomes full, it is sent to the multiplexer to shift the data so that the register becomes empty for the next data input.

Processing element: The main objective of the Processing Element (PE) is to carry an unique address along with the data to the router whose address is equal to the PE.

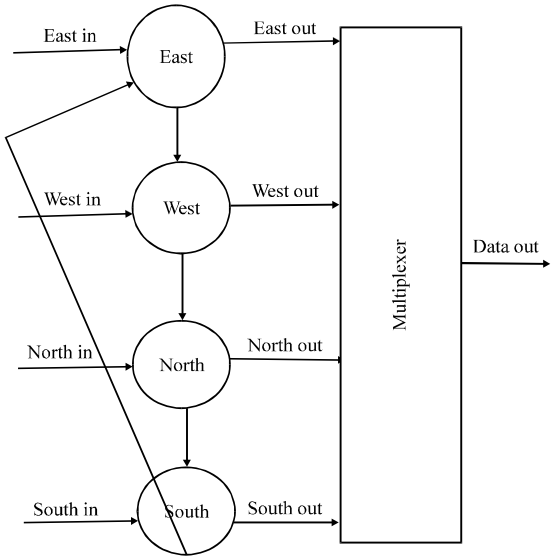


Fig. 2: Arbiter design

Wrapper: The transactions in the PE are controlled by the wrapper and also provides interface to it. Its functionality is to encode and decode the packets at both the sending and the receiving end.

Routing table design: The routing table decides the direction to send the packet with minimum number of hops to the destination so that the traffic load gets reduces. The direction of flow is given in Fig. 3 and the bidirectional routing table for 3×3 and 4×4 are shown in Fig. 4 and 5, respectively.

Figure 4 and 5 show the routing table and flow of direction where R8 and R10 are the sources, respectively. The total number of hops is shown in the table given in Fig. 4 and 5. The number 0 indicates that there is no

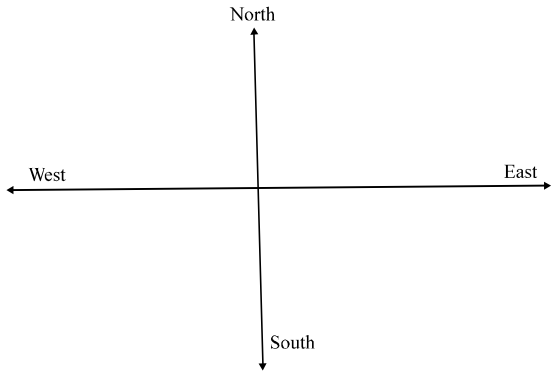
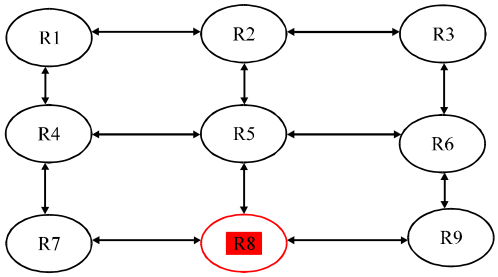
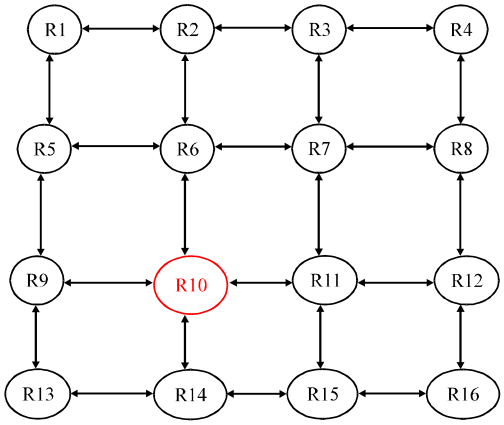


Fig. 3: Packet flow direction



Number of hops from source point RS to destination	East/West	North/South
R1	3	3
R2	4	2
R3	3	3
R4	2	2
R5	3	1
R6	2	2
R7	1	3
R8	0	0
R9	1	3

Fig. 4: Routing table for 3×3 router



Number of hops from source point R10 to destination	East/West	North/South
R1	3	3
R2	4	2
R3	3	3
R4	4	5
R5	2	2
R6	2	2
R7	2	2
R8	3	3
R9	1	3
R10	0	0
R11	1	3
R12	2	4
R13	2	2
R14	3	1
R15	2	2
R16	3	3

Fig. 5: Routing table for 4×4 router

connection to the router and the packets can't flow in that direction. Researchers present a bidirectional flow so that the router can find its shortest path to transfer the packets.

MATERIALS AND METHODS

Materials used in fault injection and materials used for rectification: In conventional data transfer, the faults mainly occur in the link which may be either temporary or a permanent. These are modeled as normal struck at faults and normally error correction codes namely hamming codes are employed to correct the faults (Jafri *et al*., 2012). The interconnection mainly ensures that the packets are transferred to the destination without

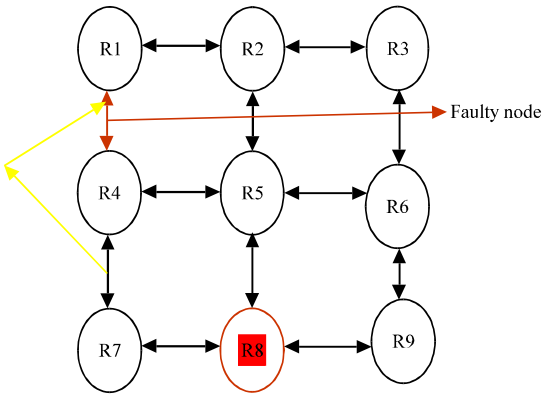


Fig. 6: Fault indication of 3×3 router

any disturbance in the network. The faults are injected into the system by using emulators which allows us to inject single or multiple faults (Griebnig *et al*., 2009).

In high performance routing system (Ebrahimi *et al*., 2013) which was proposed, mainly provides a fully adaptive Routing algorithm without affecting the performance of the system. But this technique provides only 98% reliability and the packets bypasses the faults before getting close to the destination.

In NOCs, the routing is mainly done dynamically by using shortest path algorithm (Aul *et al*., 2005) which will reduce the delay in routing so that the packets reach the destination within a short span of time. Consider the faulty node for 3×3 mesh when the packet transfers from R8 to R1 in the East/West direction which takes 3 clock cycles and for 4×4 mesh when the packet transfers from R10 to R4 in North/South mode where the faulty nodes are indicated by brown color in Fig. 6 and 7, respectively.

As the packet transfer is dynamic in nature, the faults injected in the system are due to transients in the real world. These faults are modeled as digital faults and the fault correction is done manually by the user by the principle of interconnect modeling by using the shortest path as indicated by yellow color.

The method to detect the fault is based on the comparators which compares both the ends for transmitting and receiving the data and when the fault occurs, it immediately sends the error signal to the alternate routing path so that the packet transfer will shoot up within a short span of time so that the delay gets reduced.

NOC mainly achieves its performance during the presence of faults when the packet reaches accurately without any errors to the destination. The packet delivery rate normally attains 95% (Kohler *et al*., 2010) during heavy traffic without any diagnosis and the corrupted packet never utilizes the network. The corrupted packets

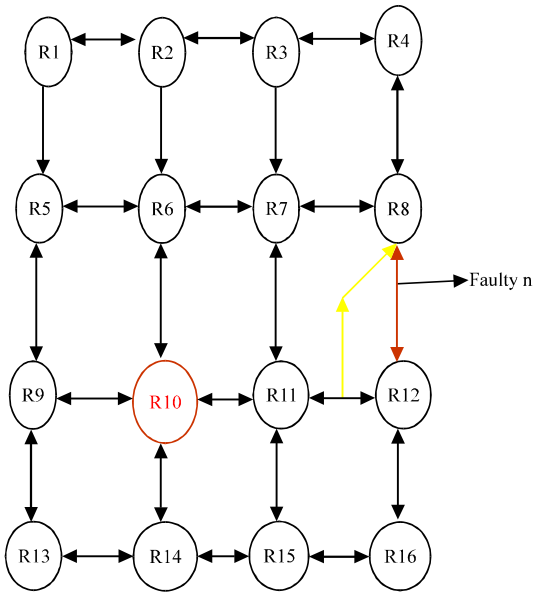


Fig. 7: Fault indication of 4×4 router

are mainly detected by the error detection capabilities which basically reduce the operating frequencies.

The bypass technique proposed also called as spare router technique which addresses both the link and the routers mainly employs error control code and replaces the faulty one by the backup path (Chang *et al*., 2011) by using Defect Awareness Path Allocation algorithm which provides diversities between the two routers and links but this technique yields only 99.9% fault coverage. The reliability of the NOC is to maintain the functional correctness even at the time of fault. The bidirectional fault tolerant scheme proposed provides only 90.80% of the fault coverage but do not address the detection mechanism (Tsai *et al*., 2011) as it mainly supports run time configuration utilizing bidirectional path which provides both transmission and receiving as the faults are located between two neighboring ends. These are mainly employed with the Cyclic Redundancy Check (CRC) logic where the faults are generally small and when one channel fails the other one normally takes its operation.

RESULTS AND DISCUSSION

The reusability technique proposed is able to rectify the fault and researchers are able to achieve 100% fault coverage for any permanent faults created in the circuit. In the experiment, researchers are able to inject 5 random faults struck at 1 and 0 which are generated by the emulator and correct it by the alternate routing method which usually takes place during the faulty conditions.

The routing technique proposed mainly reduces the latency for the system to regain its position after the injection of the fault so that the messages start routing and gives high efficiency for the NOC.

The proposed technique mainly overcomes the previous method (Feng *et al*., 2013) where the transients faults lasts for 2 clock cycles and the faulty link has to be shut down so that the router finds the alternate or uses spare components to start the routing so that the system comes back to the normal state. In the proposed method, researchers never go for any spare components so that the area gets reduced and the design itself automatically rectifies the fault by using component reusability technique which is mainly done by the user by the method of automatic interconnect technology where there are no alternate components. In this method, the data are stored in dummy cells which never take part in the normal design and once the fault is indicated, the dummy cell data are transferred to the alternate interconnects which will act as the spare to the faulty one. Thus, researchers are able to overcome the virtual channels which act as a spare cell during the faulty conditions for the packets to reach the destination node.

This technique never uses error correction codes and CRC which normally increases the area of the design and the testing mechanism becomes complex to detect and correct the fault. The reliability of this scheme is usually high during heavy traffic conditions which lead to failure thus degrading the system. The proposed configuration normally increases the redundancy of the system in all nodes and also increases the memory accessibility so that the performance increases even at higher frequencies for various design strategies and clustering techniques.

CONCLUSION

The future research will explore more on transient faults and increasing the size of the NOC and increasing the frequency and also more on temporary faults which contributes 100% packet reception and also exploring the reliability of the system and also increasing the fault detection mechanism which will reduce the latency of the system to bring back to the normal operation which gives 100% efficiency of the system when implemented in real time.

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