International Journal of Soft Computing 10 (2): 211-217, 2015
ISSN: 1816-9503

Power Reduction in SRAM-Based Processor Units Using 7T HETTs

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Abstract: In MOSFETs lower limit sub-threshold swing (60 mV/decade) restricts the low power operation. Low voltage operation is enabled by low threshold voltage while maintaining performance. Hence, steep sub-threshold slopes provide power-efficient operation without any loss of performance. To obtain sub-threshold swings of <30 mV/decade with large ON current, Si/SiGe heterojunction tunneling transistor uses gate controlled modulation. The sub-threshold swing of HETTs is <60 mV/decade. To overcome the impact of HETT characteristics on SRAM, seven transistors HETT based SRAM design is introduced. Without leakage-reduction techniques, it is now in the range of mA and in some cases can account for >50% of the total power consumption. Compared to CMOS this new HETT SRAM achieves reduction in leakage power. The obtained HETT, SRAM cells are used in register cells for power reduction in SRAM and CAM based processors. The average power consumption in 7T HETT SRAM is low as compared to 6T SRAM.

Key words: Heterojunctions, low power, processor, SRAM cells, tunneling transistor

INTRODUCTION

In low power design techniques, low voltage operation is the effective low-power design techniques because of its quadratic dynamic energy saving. Recent works (Seok *et al*., 2011; Lee *et al*., 2012, 2013) have shown that power consumption can be reduced by supply voltage reduction to near or below the threshold Voltage (Vth) of MOSFET devices. The ON current drops dramatically because of the lack of gate overdrive, resulting in large transition delays at low supply voltages. The threshold voltage can be reduced to regain this performance loss. But it exponentially increases the OFF current which leads to problems in applications that spend significant time in the standby mode (Zhai *et al*., 2004). Lowering the supply voltage from 500-250 V while enforcing performance by reducing the Vth increases the leakage power by 275 times in a commercial CMOS technology is unacceptable.

To address this there have been new devices with steeper sub threshold slopes then traditional MOSFETs (Hu *et al*., 2010). While maintaining low leakage, steep sub-threshold slope enables operation with a much lower threshold voltage. Low voltage operation is enabled by low Vth while maintaining performance. Hence, steep sub threshold slopes provide power-efficient operation without any loss of performance. The study focus on circuit designs using the recently proposed Si/SiGe Heterjunction Tunneling Transistor (HETT) (Nayfeh *et al*., 2008). To obtain sub-threshold swings of <30 mV/decade with large ON current, Si/SiGe heterojunction tunneling transistor uses gate controlled modulation. Furthermore, heterojunction transistors are fully compatible. Heterojunction transistors are developed by several industries and university teams and initial devices have been demonstrated (Krishnamohan *et al*., 2008). The differences between HETTs and traditional MOSFETs must be considered. HETTs display asymmetric conductance. The source and gate are interchangeable in MOSFETs and determined by the voltages during the operation. However in HETTs, source and drain are determined at the time of fabrication and the current flow is substantially less than for NHETT (n type HETT). Hence, HETTs operate unidirectional, i.e., passing logic values only in one direction. It has implications on Static Random Access Memory (SRAM). Another effect is a large increase in gate to drain capacitance (i.e., miller capacitance) in HETTs compared to MOSFETs. It can cause undesirable artifacts in the switching behavior of HETTs which is not present in MOSFETs. HETT based logic circuits are capable of improving energy efficiency by 19×compared to CMOS when operated at a supply voltage of 0.23 V. The SRAM design is impacted mostly by the novel characteristics of HETTs. Unidirectional characteristics of HETTs can be exploited in SRAM design to enable a novel 7T SRAM cell.

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MATERIALS AND METHODS

HETT device characteristics: The sub-threshold slope limitation 60 mV/decade of MOSFETs arises because of thermionic nature of turn-on mechanism. But tunneling transistors do not suffer this limitation. Since, in these devices turn on mechanism is not governed by thermionic emission. The tunneling transistors are very narrow bandgap semiconductors used to obtain sufficiently HIGH ON current. However, the problems with the narrow band gap semiconductors are it leads to higher OFF currents and incompatible with CMOS processing. For making this technology fully CMOS compatible, complementary n and p-HETTs can be fabricated by reusing the masks for NFETs and PFETs. To get optimized HETT drain, two masks are used and for optimized HETT source, two more masks are again required. Hence, depending on the degree of optimization 0-4 extra masks for HETT implementation. In BiCMOS more than eight masks are used.

HETT device modeling and circuit analysis: The HETT is modeled as a three-terminal device (source, gate and drain). Current is assumed to flow only between source and drain since gate leakage is negligible. Channel capacitance negligible due to its fully depleted channel and junction capacitance is negligible because it is silicon on insulator type. Lower threshold swing is exhibited by the HETT devices. Larger ON current and sub-threshold swing of HETTs permits voltage scaling, enabling dynamic power reductions.

Limitations of HETT-based circuits

Asymmetric current flow: During fabrication HETT source and drain are determined and current flows between two nodes are asymmetric. The use of traditional CMOS logic circuits with pull-up and down network does not restrict the asymmetric current flow because the current flow of each device in the pull-up and down is unidirectional. By this current direction, CMOS logic can be fully constructed with HETT. Pass transistor and transmission gate operation is restricted because it requires current flow in both directions. The forward ON current can strongly drive the output but the reverse ON current cannot. For HETT based circuits, pass gate logic is useless because of directional current driving capability. The asymmetric current flow limits the use of standard 6T SRAM cell and static latches/registers. By using clocked CMOS logic, latches and registers can be implemented without pass gates and transmission gates.

Increased miller capacitance: The capacitance between the gate and drain is referred as the miller capacitance due to miller effect (Sedra and Smith, 1998). Due to the linking of the inversion layer in HETTs to the drain rather than the source, miller capacitance in HETTs is larger than that in MOSFETs.

6T SRAM design with HETT: The limitation of asymmetric current flow restricts the use of the passgate and the transmission gate. Since, CMOS logic is the most widely used logic not affected by this limitation as the current is expected to flow only in one direction in the channel of each transistor. To prevent the malfunctions with HETT, any pass-gate logic is converted to CMOS logic. However, standard 6T SRAM uses pass gates for access transistors. Since, the impact of HETTs asymmetric current flow on SRAM is significant. In this study, we first analyze the implications of asymmetric current flow on SRAM operation and go on to propose an alternative 7T HETT-based SRAM cell topology. Then, we compare the 7T performance and robustness to that of a CMOS-based 6T SRAM design. Microwind tool can be used to obtain the simulation results.

CMOS standard 6T SRAM: Trace the current flow paths in read and write operations to understand the difference between FETT-based 6T SRAM and CMOS-based 6T SRAM. From Fig. 1, it shows a CMOS 6T SRAM.

6T SRAM cell storing "0". Bit lines (BIT, BIT_B) are precharged to V_{DD} to read the stored value. NPDL pulls down the voltage at BIT when a Word Line (WL) is driven high for READ operation is shown in Fig. 1a. To determine the stored value, pull-down current or voltage can be sensed by a sense amplifier. AXL pulls up the internal node N0 while AXR pulls down the internal node N1for writing a value as shown in Fig. 1b. AXR plays the major role in write "1" operation. Since, both access transistors are NMOS which are better pulling low. AXL aids in writing a "1" by pulling up N0 to a certain extent and making the bit flop more easily. Read stability can be improved by increasing the sizing ratio of NPDL to AXL which is commonly referred to as the cell β-ratio. NPDL in Fig. 1a holds the voltage at node N0 to ground more strongly during read, making it more stable as the cell β-ratio increases. This worsens the write ability of the cell by making it more difficult to change the voltage at node N0 at the same time. Pull down current path plays the major role in writing. Critical one for writeability is the size ratio of AXR to PPUR or AX to PPU. It can be improved by increasing this ratio as shown in Fig. 1b. It implies that readability and writeability in CMOS 6T SRAM can be improved individually at the cost of larger area.

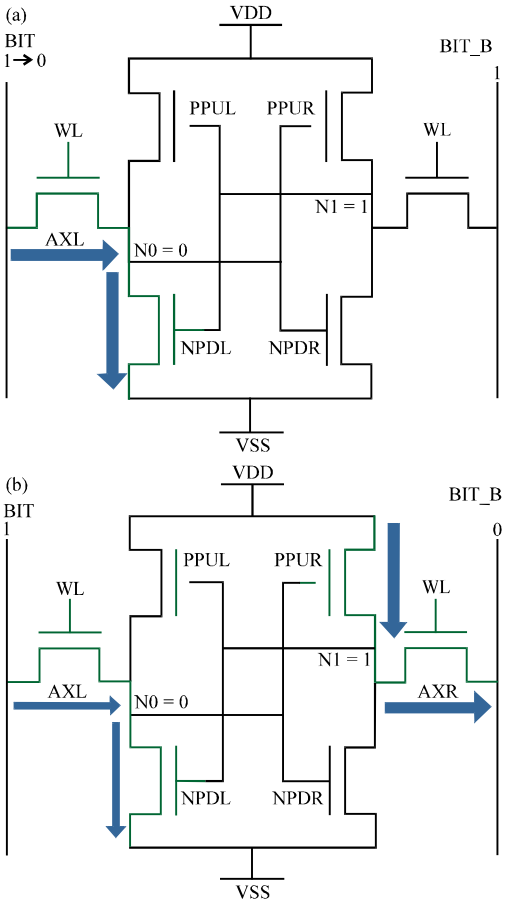

Fig. 1: Current flow paths in a) read and b) write operations in CMOS 6T SRAM

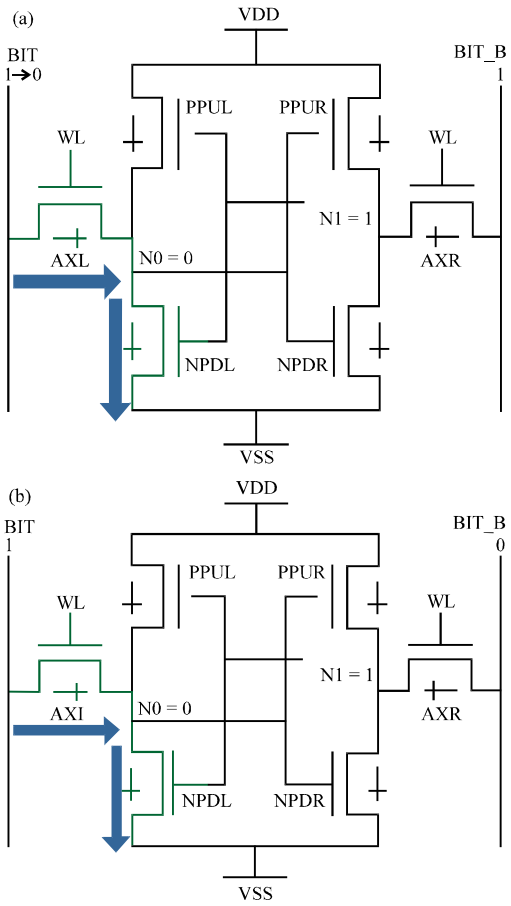

Fig. 2: Current flow paths in a) read and b) write operations in HETT 6T SRAM with inward direction access transistors

RESULTS AND DISCUSSION

HETT standard 6T SRAM with inward access transistors: Access transistors in HETT 6T SRAM can drive current either inward or outward due to its unidirectional nature. HETT 6T SRAM structure with inward current flow configuration and storing "0" shown in Fig. 2. Read operation for SRAM is similar to that of a CMOS 6T SRAM. The current flows through AXL and NPDL and bit lines are precharged. Thus, a higher cell β-ratio is preferred for preventing read upset similar to CMOS 6T SRAM. Here, 6T SRAM transistor cells are designed and simulated outputs are shown in Fig. 3a and b.

Figure 2b shows to write "1" to this cell, AXR cannot pull down the voltage at N1 since it can only conduct current inward, AXL must pull up the voltage at N0 without differential aid. Only by one side write operation is performed and the stronger current path removed in HETT 6T SRAM. Writeability of n-type transistor is worse than a CMOS 6T SRAM. To overcome this AXL should be strengthened compared to NPDL. Hence, the cell β-ratio should be decreased and it negatively affects the read margin.

Static Noise Margin (SNM) is the maximum DC voltage of the noise that can be tolerated by SRAM. It is widely used for modelling stability of SRAM cells (Seevinck *et al*., 1987). It can be defined for three different operations: read, write and standby (hold). But read and write only limit SRAM stability. For HETT 6T SRAM with cell β-ratio of 1, the read margin is 34 mV but write margin is impossible as it is 0 V. When β-ratio is 0.64, write margin becomes positive but the noise margin is degraded to <3 mV, i.e., at this design point, it is vulnerable to read. So, we conclude that HETT 6T SRAM with inward access transistors is not feasible.

HETT standard 6T SRAM with outward access transistors: A HETT 6T SRAM transistor has a similar limitation. Figure 2a shows a read operation where bit

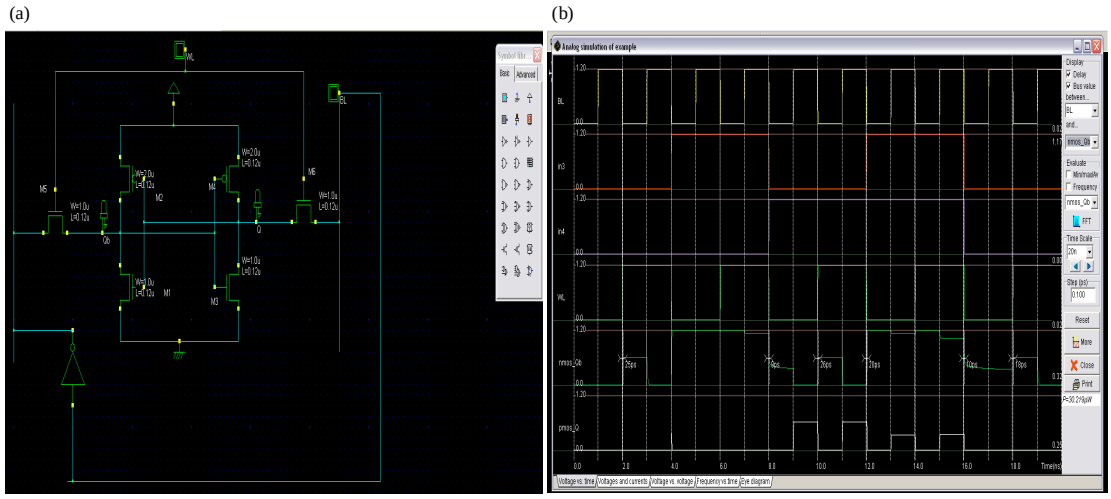

Fig. 3: a) Design of 6T SRAM and b) simulation of 6T SRAM

lines (BIT, BIT_B) are predischarged. BIT_B is charged through AXR and must be sensed. AXR must drive internal node N1 to ground for read operation and flip the stored value without assistance from AXL. Adjusting the ratio of PPUR to AXR strengths will improve one operation and worsen the other. AN alternative SRAM topology is required to achieve robust low leakage SRAM with HETTs. Because SNM for read/write operation is limits to <50 mV.

Alternative SRAM design with HETT: The implementation of 6T HETT SRAM limits the tradeoffs between writeability and readability. It can be avoided by separating read and write current flow paths at the cost of a new transistor. Here, various possible read and write structures for HETT-based SRAM are compared. Ten 7T HETT SRAM is proposed and analyzed.

Read structures for HETT SRAM: Back to back inverters are the components in 6T SRAM that store the value and at the same time two access transistors are used as read structure and write structure. Three possible structures are obtained to separate read and write operations. Additional HETT dedicated to read operation is attached to the back to back inverter pair. To minimize the chance of read upset, inward NHETT configuration is preferred to outward configuration in this structure. Separate cell β-ratios can be obtained for read and write operations. This is the benefit of this separate structure. While maintaining same write margin, better read margin can be obtained by utilizing a weaker inward NHETT. Widely used read structure in CMOS 8T SRAM is available.

Write structures for HETT SRAM: By allowing bidirectional current flow replacing access transistors with transmission gates, tradeoffs between readability and writeability can eliminate. This scheme requires eight HETTS which can be reduced by more advanced read and write structures. Single ended access can be used whereby transmission gate on one side can be eliminated to reduce HETT count.

7T SRAM for HETT: 7T SRAM is proposed for HETT. Readability/writeability tradeoffs in HETT based 6T SRAM are overcome by utilizing separate read and write structures. The 7T SRAM cell structure do not use decoupled read. The 7T SRAM is estimated to have <15% area overhead Over a standard 6T HETT. Making the overhead for two 7T cells are equal to one 8T SRAM cell (Kim *et al*., 2011). Minimum size of 7T cell shows improved robustness over 6T at low voltage. Upsized 6T is used to achieve iso-robustness. Cells are optimized after iso-robustness. To take the advantage of the low leakage current of the HETT devices, memory cell array should be HETT based for the proposed HETT 7T SRAM. Compare the Static Noise Margin (SNM) of HETT based SRAM cell with CMOS 6T SRAM. For maximum density, all HETT devices are set to equal width. Read operation uses an additional read transistor in the HETT 7T SRAM cell and all other transistors are in standby (hold) state during read operation; hold margin is equal to that in HETT 7T SRAM. HETT based SRAM standby power is reduced significantly as compared with CMOS 6T SRAM. The low leakage properties of HETT devices dominated for low leakage applications. Here, 7T SRAM transistor cells are designed and simulated outputs are shown in Fig. 4a and b.

7T HETT SRAM in register files of processor: To obtain the power reduction in processor, the predesigned 7T HETT SRAM is used in the register files of the processor.

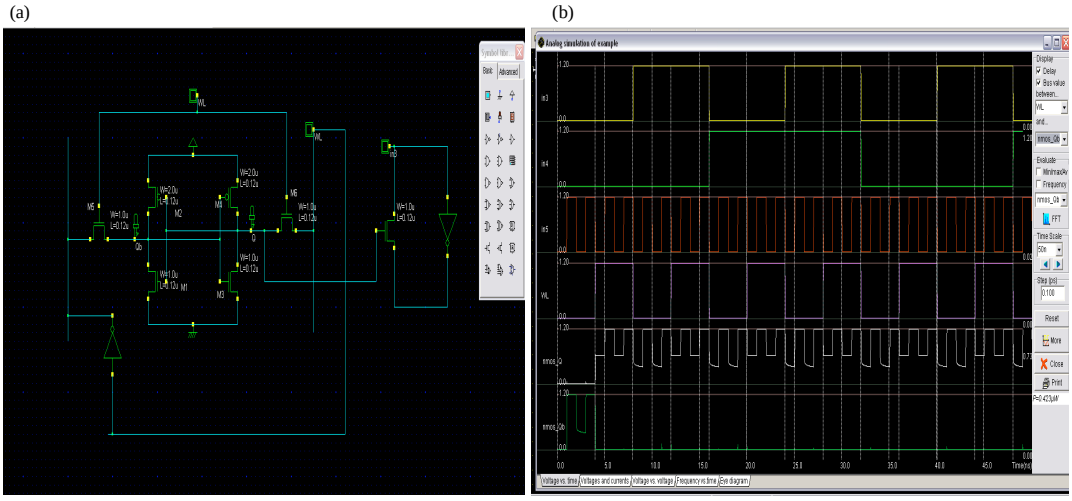

Fig. 4: a) Design of 7T SRAM and b) simulation of 7T SRAM

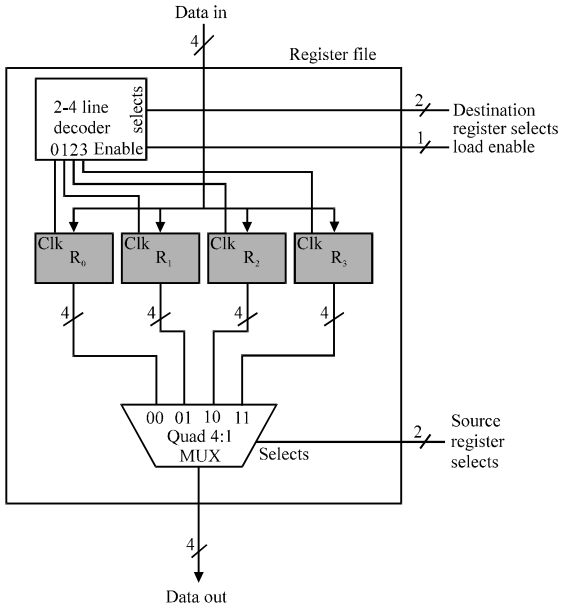

Fig. 5: Basic register file

Here, SRAM and CAM based processors are used. CAM based processors are used to get the address of the specified date or input. Register files and datapath are used to gain insight into the internal logic for data movement between registers in a computer. The basic diagram of register file is shown in Fig. 5a, register file is an array of processor registers in a Central Processing Unit (CPU). Modern integrated circuit-based register files are usually implemented by the way of fast static RAMs with multiple ports. Such RAMs are distinguished by having dedicated read and write ports whereas ordinary multiported SRAMs will usually read and write through the same ports.

Set of registers are used to stage data between memory and the functional units on the chip. It shows the minimal required hardware modifications to dynamically adjust the size of these units. Tanner tool can be used to design register cell. The designed diagram and its simulation output are shown in Fig. 6a and b. The predesigned 7T HETT SRAM is used in the register files of the processor. Here, 4×4 register file is constructed. The register file requires a 2-4 line decoder with HI-true outputs and one HI-true enable input as shown in Fig. 5. The register file also requires a Quad 4:1 multiplexer. A Quad 4:1 MUX has four 4 bit data. Register file also requires a Quad 4:1 multiplexer. A Quad 4:1 MUX has four 4 bit data inputs, a 4 bit data output and two select lines.

Comparison results: The power results of the normal 6T SRAM and the designed 7T HETT SRAM are compared. The design of 6T SRAM on register files are obtained in Fig. 7a. Six transistors are used here. But it is more power consuming. The simulation output is represented in Fig. 7b.

The power consumed in the processor by using 6T SRAM is obtained in Table 1. The average power is $4.59e^{-4}$ W. The minimum power is high with value of $4.24e^{-8}$ W. In the case of 7T HETT SRAM, seven transistors are used is shown in Fig. 8a. By using 7T HETT cells in register files, power consumption is reduced as compared to the 6T SRAM. The average power for 7T HETT is $4.10e^{-8}$ W. The minimum power is also reduced. The value of power reduced by the use of 7T SRAM by combining with HETT. In 6T SRAM the area overhead is high as compared with 7T HETT. The simulation output is obtained with four registers are shown in Fig. 8b.

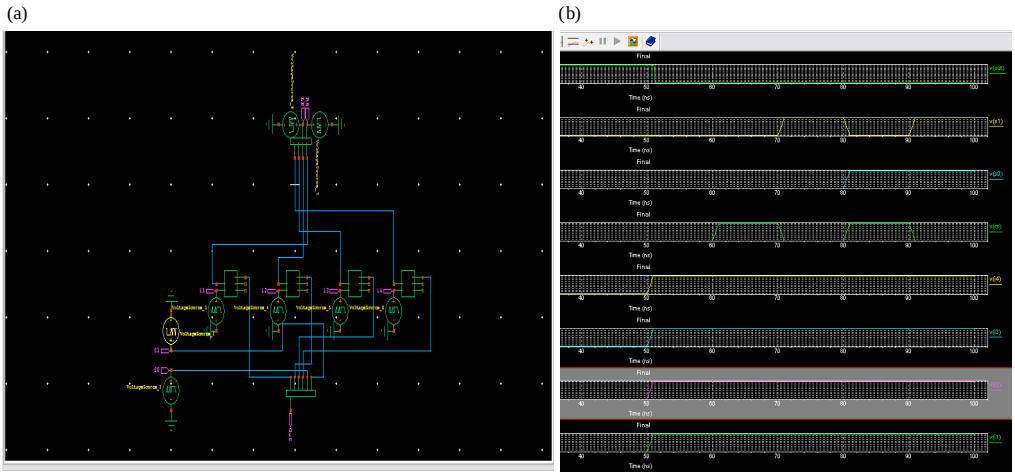

Fig. 6: a) Design of register file and b) simulation output

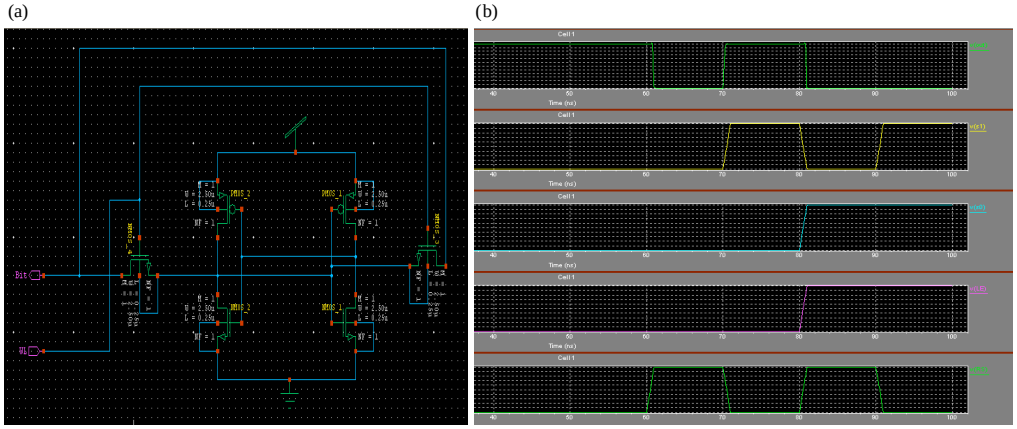

Fig. 7: a) Design of 6T SRAM on register file and b) simulation output for 6T SRAM on register file of processor

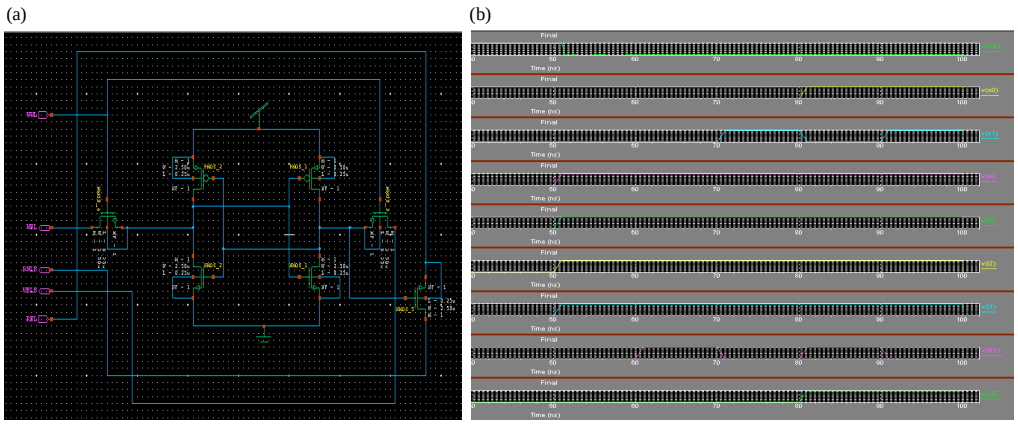

Fig. 8: a) Design of 7T HETT SRAM cell and b) simulation output for 7T HETT SRAM on register file of processor

Table 1: Power comparison

Parameters	6T SRAM (W)	7T HETT SRAM (W)
Average power	4.59	4.10
Minimum power	4.24	1.11

CONCLUSION

The asymmetric current flow and miller capacitance are investigated. With HETT based circuits, 9-19 times dynamic power reduction is expected due to tier improved voltage scalability. The drawbacks of HETT are obtained. It can be overcome by a new HETT-based SRAM cell topology with leakage power reduction. The use of 7T HETT SRAM in register file of processors reduces the power in processors with effective performance. The average power consumed processors using 6T SRAM is more as compared to the 7T HETT SRAM. The average power consumed in 6T SRAM is $4.59e^{-4}$ and $4.10e^{-4}$ in 7T HETT. And the minimum power is also reduced in 7T HETT as compared to 6T SRAM. The minimum power value is $1.11e^{-8}$. Hence, the power in processors reduced.

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