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Performance Analysis of EMTCMOS Technique Based D Flip Flop Design at Varied Supply Voltages and Distinct Submicron Technology

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Abstract: Power is a major concern in the design and implementation of sequential circuits. Various attempts were made in the past to optimize power consumption values in the sequential circuits such as flip flops. Enhanced multi threshold CMOS is adopted in this work, which yielded best results for D flip-flop in terms of power consumption. The results are also examined for 180, 90 and 45 nm technology and the performance of the circuit is analyzed. A comprehensive analysis is carried out in terms of performance parameters as power consumption, leakage current and delay. The EMTCMOS Flip Flop is also used to design the ripple counter circuit and the performance was analyzed. However, this design is analyzed for only 90 nm technology. This research is carried on Cadence Virtuoso tool at 180, 90 and 45 nm technology.

INTRODUCTION

Novel electronic systems demands novel procedures as the challenges are distinct. Power consumption is one such challenge faced by the industry with the growing demand for scaling of the devices and systems. The reduction of power consumption is a cumbersome task that covers variety of parameters to look into. But any reduction in power consumption is welcomed by the electronics world, particularly in the high performance gadgets like mobiles, personal computers where digital logic is predominant.

The concept of reducing power consumption can be dealt at different levels such as architectural, design and device levels. The primary components of power consumption in a circuit are leakage, dynamic and static power. Dynamic is mainly due to switching, static depends on logic and leakage is due to improper designing of the circuit and leakage current[1].

The other side of this power reduction challenge is very interesting in the backdrop of evolution of integrated circuit technology. IC's demands lesser energy levels for operation and scaling is the principle for achieving higher functional densities. This puts upon consistent demand for the miniaturization. Balancing the objective of higher functional density and arriving at feasible solutions pertinent to power consumption and smartness in the design is periodically challenging researchers.

On the other hand, higher the power consumption the degree of reliability is under scanner. This also poses

issues such as electron migration which in turn compelling the designers and researchers to look for optimal power consumption solutions for various designs[2, 3].

This challenge is subsidized to certain extent in the case of combinational circuit designing. By choosing a proper logic and the method of realizing the logic, one can counter the challenges in the combinational circuit designing. But it reaches to the next level in the sequential circuit designing as it involves time as a prime concern. When delay is associated in the set of parameters of performance, it directly or indirectly influences the designer choice of power consumption and area optimization[3, 4].

There is an effective way of reducing the supply voltage in the process of achieving lesser power consumption in digital logic design as the $P_{average} = CV^2f$. Here, care should be taken in such a way that scaling should not hamper the progress of achieving lesser power consumption as scaling increases static power consumption. Scaling no doubt enhances the chance of achieving objective of increasing density of components in an integrated circuit. As an example, a constant field scaling can almost double the expectancy in the frequency and switching power values of a design. Leakage current also may increase exponentially, even though sub threshold leakage values are not predominant factors of power consumption in MOS circuits. But the point to be remembered is the context of scaling, leakage currently also plays a significant role in the performance of the design. So, the idea of reducing supply voltage should be carefully weighed in the line of designing digital logic circuits[5, 6].

Most of the researchers worked on optimizing distinct parameters pertinent to circuit designing in accordance with the need or specifications. Various methodologies or techniques adopted in achieving the results. Power reduction or estimating power consumption is one such attempt which was vital for the progress of the digital circuit design exploration. Increasing the clock frequency is one best solution for tackling the challenge of power consumption[7]. But it also poses problems in the design of a sequential circuit like flip flop. So, other alternative methods have to be explored for the purpose of curtailing higher energy consumption values. Multi threshold logic is one such good attempt of achieving feasible solutions in terms of power consumption and mostly delay in the digital logic designing.

Multi threshold logic and its impact in digital circuit designing: Threshold voltage is the key factor in analyzing the performance of a transistor. In the circuit level design, the compulsion of having the same threshold voltage for all the components or transistors is made flexible with the recent developments in the technology. This revolution in this technology paved the way for using different threshold voltages in a design which was famous as multi threshold CMOS logic or MTCMOS logic. Numerous advantages that this logic has brought to the circuit designing as it enable to optimize the delay and power values in a design.

Components with lesser threshold voltage generally possess higher switching capacity. This is very significant when it comes to the sequential circuit designs such as Flip-Flops (FF), counters, etc. The trade off factor, here is the static leakage power consumption. To overcome this disadvantage, the solution can be using higher threshold voltage components. But care should be taken such that higher threshold voltage components are used in the non critical paths. It was proved by the researchers that static leakage reduced by almost 10 times in the case of higher threshold voltage component designs when compared with their counterparts[5].

MTCMOS logic or technology is popular because it caters both lesser threshold voltage as well a reduced stand by current. This ensures high speed lower energy consumption in the circuits which is the most desirable aspect of modern day aspirations of circuit designing. The versatility of this technology is it employs both high and lower threshold voltage components in a single platform. It also operates in active and sleep modes for achieving effective power management, especially in the digital circuits[8].

With all the aforementioned reasons, MTCMOS is the choice of modern day designer as it offers higher performance in addition to lesser leakage current by the method of employing sleep transistors. Proper sizing of these sleep transistors becomes more significant as it saves the power consumption in this technology.

Summarizing the facts of this technology, MTCMOS uses lower threshold voltage transistors in the logic cell designing and higher threshold voltage transistors as the sleep transistors. These sleep transistors isolates the logic cells from the supply voltage and ground in order to reduce the leakage in the sleep mode. This is also termed as power gating. This is based on virtual VDD and virtual ground concept. Here also, the key aspect here is sizing the sleep transistors. The time for which the transistor is in the sleep mode also influences the performance of the IC, so, care should be taken in the aspects related to the timing of the sleep and active modes in the design. The transition time between these two modes and the current in the sleep mode is also responsible for the rise in the unwanted energy or noise in the circuit[9].

With all the emphasis made on the evolution and ease of using this technology, it can be said that MTCMOS has been emerging as the promising technique for the circuit designers. This is because it is offering higher speed as well as the possibility of arriving at lower power consumption values. The typical circuit model of MTCMOS logic is shown in Fig. 1.

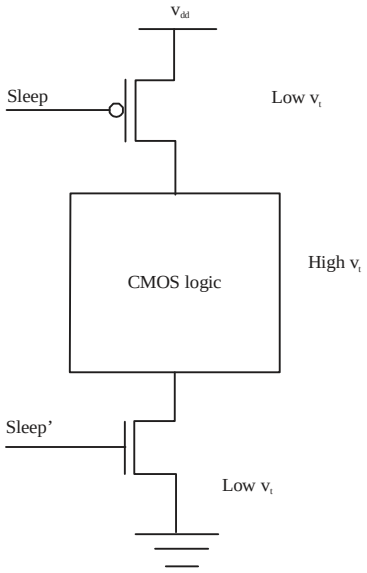

Fig. 1: MTCMOS circuit

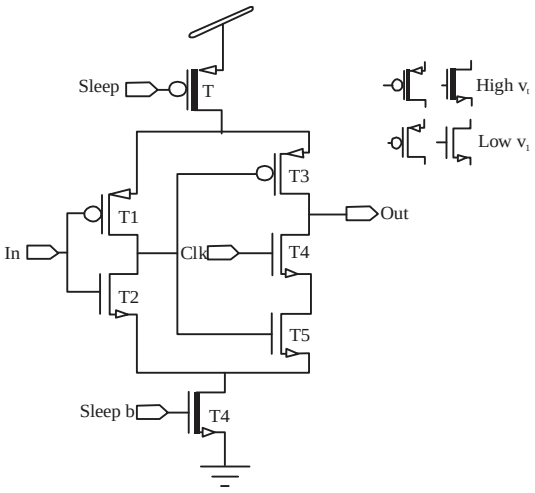

Fig. 2: D FF using MTCMOS technique

As MTCMOS technology uses lower as well as higher threshold voltage transistors in a monolithic platform. It offers lesser leakage current and lesser power consumption. As dynamic power consumption is in direct relation with the supply voltage. Reducing supply voltage cannot be considered as the unique solution for reducing power consumption as it also leads to performance degradation of the circuit. So, using multi threshold voltage in the circuit along with the reduced supply voltage has become the central principle of this technology.

Using this multi threshold logic is more flexible and easy in the case of combinational circuits when compared with the sequential circuits[10]. The challenge in the sequential circuit implementation appears in the form of data loss. In this resesarch, this challenge is effectively dealt by extending this method in arriving at enhanced performance of the D flip flop circuit in terms of power consumption and delay with appropriate values of threshold voltages and supply voltages which is termed as enhanced multi threshold voltage CMOS of (EMTCMOS) logic.

MATERIALS AND METHODS

Design of D flip flop using EMTCMOS technique: Flip-flop is the fundamental memory element of the digital logic. Flip-flop is used to store the information with two stable states. When these are used in the design of larger memory circuits, the speed of the system depends not only on the present input but also on the present state. It is an iterative procedure which gives results at every instant in two states whereas one is complement to other. Clock governs this process and clock management itself is a larger domain of research[11]. Any advancement in the performance of this component yields multiple results in the next level memory circuits designing. This made us to choose flip-flop circuit for the analysis in this work. Flip-flops are very critical in terms of time, speed and power consumption. Due to the above mentioned reasons, enormous research was done and is going on in this domain of designing high performance flip-flops[12].

MTCMOS FF operation is similar to traditional FF operation, but transistor sizing aspect should be taken care as the distinct threshold voltage components are in the same platform. The possibility of leakage current is high so the sizing becomes crucial in order to protect weak transistors. Choice of threshold voltage also plays a major role in this process. EMTCMOS takes care of all these aspects and can achieve better performance than the former methods. Figure 2 represents the design of a D FF using MTCMOS technique.

In this circuit, higher threshold voltage transistors are to be in the OFF state to separate from the lower threshold voltage transistors from the supply voltage. Higher threshold voltages are necessary for the reduction of leakage currents is the established fact. The design of D flip-flop using the MTCMOS technique in the cadence platform is as shown in Fig. 3. The design of EMTCMOS D FF using cadence platform is as shown in Fig. 4.

The power consumption in the design depends on frequency, capacitance, supply voltage and many other factors. The total power consumed is the sum of dynamic, short circuit and leakage power components in a circuit[13].

The dynamic power depends on the switching transients in the FF circuit[7]. Static power consumption

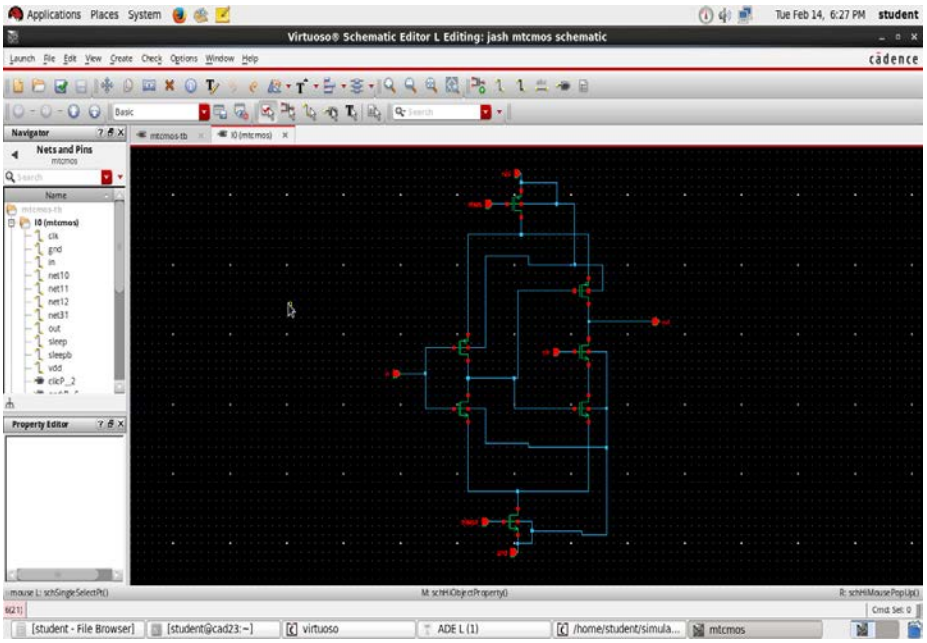

Fig. 3: Design of MTCMOS D FF

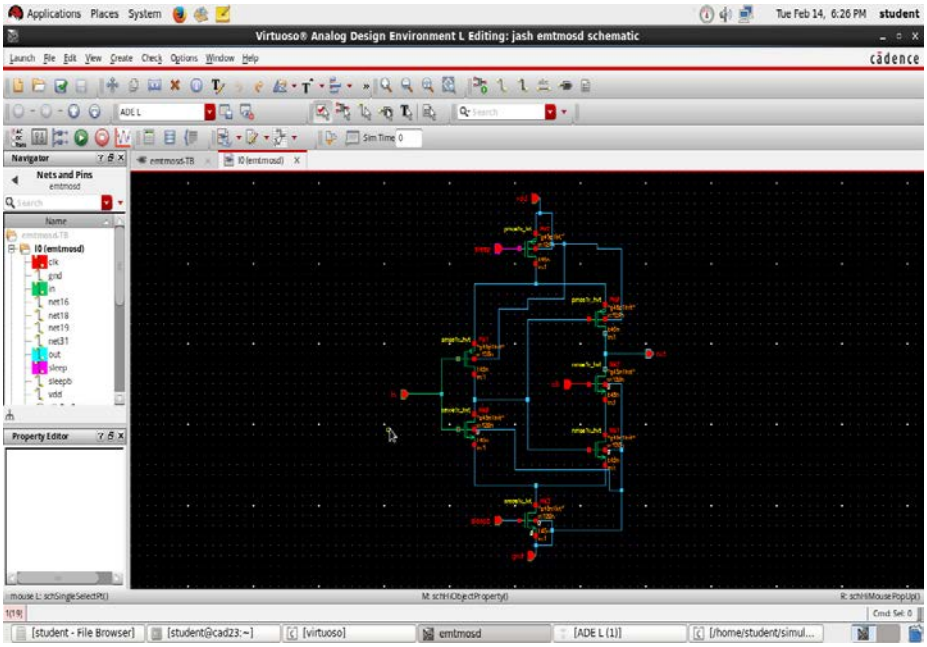

Fig. 4: Design of EMTCMOS D FF

depends on the logic or the number of components used in the circuit. The impact of flip flop design on the power consumption values is notable[14]. Average power, Power delay product, delay are the generic parameters used in the power analysis of the circuit[15, 16]. In this work also the same set of parameters were considered for the performance analysis.

RESULTS AND DISCUSSION

Simulation results: After the exhaustive literature survey, the standard supply voltage values for the design and threshold voltage values of the transistors are considered in two sets for the analysis. DC voltage Vdc of 0.3, 0.5, 1, 1.2, 1.5 and 1.8 v are considered for both 180,

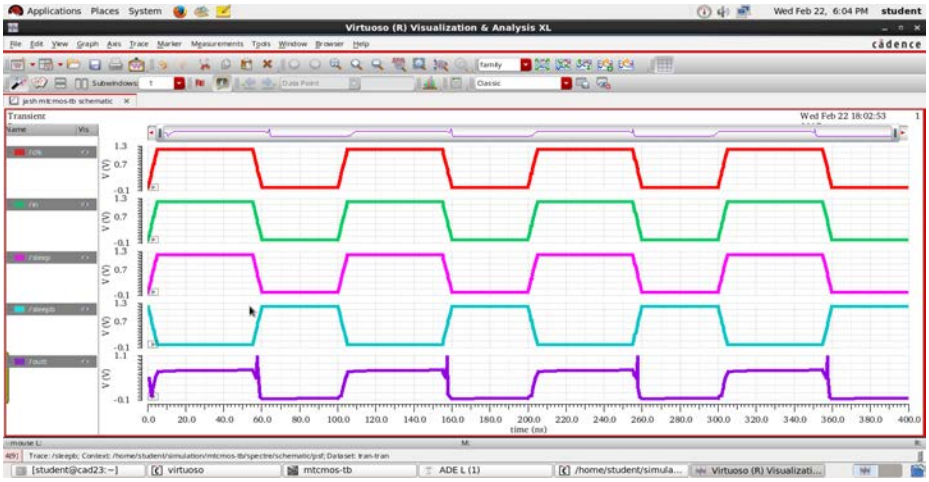

Fig. 5: The output waveform of MTCMOS D FF at180 nm technology

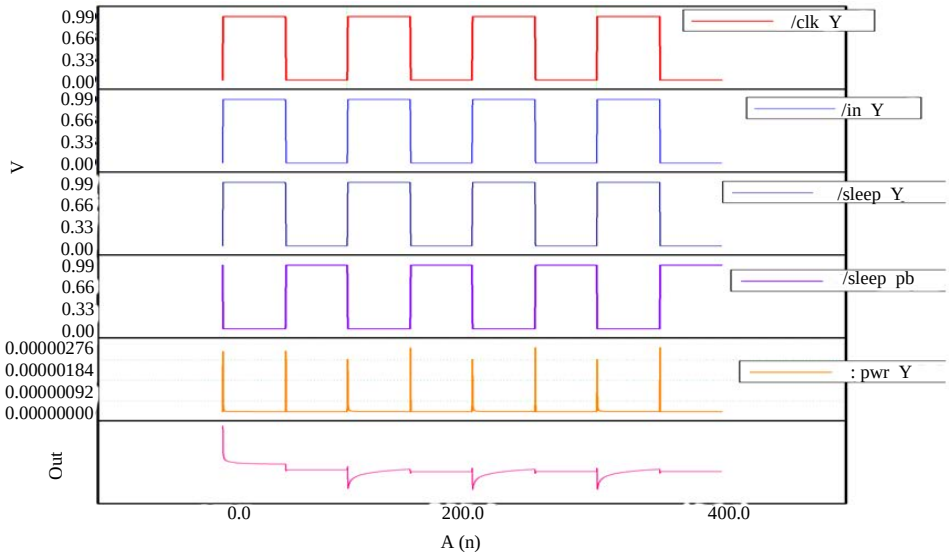

Fig. 6: The output waveform of EMTCMOS D FF 180 nm technology

90 and 45 nm technology. Threshold voltages are also considered in relevance to these values. Figure 5 and 6 represents the output waveforms of MTCMOS D FF and EMTCMOS DFF at 180 nm technology with the respective supply voltages of 1.8 v for MTCMOS and 1.2 v and subsequent threshold voltages. Table 1 and 2 represents the comparative analysis of MTCMOS and EMTCMOS D flip-flop designs at 180 and 45 nm technology, respectively for varied supply and threshold voltages.

The analysis of the results indicates that EMTCMOS D FF average power consumption and delay values are better than MTCMOS D FF with variable supply voltages. Figure 7 and 8 represents the output waveforms of MTCMOS D FF and EMTCMOS D FF at 45nm technology with the respective supply voltages of 0.7 v for MTCMOS and 0.5 v and subsequent threshold voltages.

The output waveforms obtained in Fig. 5-8 are in coherence with the truth table of traditional D Flip-flop. The analysis of the results indicates that EMTCMOS D FF average power consumption value is obtained in pico watts whereas in MTCMOS D FF it is in nano watts when the supply voltage is of 0.5 v. Similarly, power consumption, leakage current and delay values are better in EMTCMOS D FF than MTCMOS D FF with

Table 1: Comparative analysis of MTCMOS and EMTCMOS D FF with respect to differential supply and threshold voltages at 180 nm technology

Name of the circuit design	Supply voltages and threshold voltages	Leakage current (Amp, pA)	Average power (nW)	Delay (sec, nS)
MTCMOS D FF	Vdc =0.3v, Vth = 0.15 v	57	0.307	149
EMTCMOS DFF	Vdc = 0.3v, Vth = 0.15 v	2.12	0.22	131
MTCMOS D FF	Vdc = 0.5v, Vth = 0.25 v	265	10.1	119
EMTCMOS DFF	Vdc = 0.5v, Vth = 0.25 v	5.1	3.5	104
MTCMOS D FF	Vdc = 1v, Vth = 0.5 v	311	290	96
EMTCMOS DFF	Vdc = 1v, Vth = 0.5 v	9.2	85	83
MTCMOS D FF	Vdc = 1.2v, Vth = 0.6 v	351	330	74
EMTCMOS DFF	Vdc = 1.2v, Vth = 0.6 v	12	130	62
MTCMOS D FF	Vdc = 1.5v, Vth = 0.75 v	490	510	64
EMTCMOS DFF	Vdc = 1.5v, Vth = 0.75 v	35	171	53
MTCMOS D FF	Vdc = 1.8v, Vth = 0.9 v	560	615	46
EMTCMOS DFF	Vdc = 1.8v, Vth = 0.9 v	67	204	39

Table 2: Comparative analysis of MTCMOS and EMTCMOS D FF with respect to differential supply and threshold voltages at 45 nm technology

Name of the design	Supply voltages and threshold voltages	Leakage current (Amp, pA)	Average power (W)	Delay (sec, nS)
MTCMOS D FF	Vdc = 0.3v,Vth = 0.15 v	40	159 pW	110
EMTCMOS DFF	Vdc = 0.3v,Vth = 0.15 v	0.76	148 pW	102
MTCMOS D FF	Vdc = 0.5v,Vth = 0.25 v	57	688 pW	98
EMTCMOS DFF	Vdc = 0.5v,Vth = 0.25 v	1.2	389 pW	92
MTCMOS D FF	Vdc = 1v,Vth = 0.5 v	77	1.586 nW	79
EMTCMOS DFF	Vdc = 1v,Vth = 0.5 v	2.3	0.937 nW	72
MTCMOS D FF	Vdc = 1.2v,Vth = 0.6 v	85	1.928 nW	68
EMTCMOS DFF	Vdc = 1.2v,Vth = 0.6 v	2.75	1.151 nW	63
MTCMOS D FF	Vdc = 1.5v,Vth = 0.75 v	102	2.419 nW	59
EMTCMOS DFF	Vdc = 1.5v,Vth = 0.75 v	8.8	1.451 nW	52
MTCMOS D FF	Vdc = 1.8v,Vth = 0.9 v	174	2.955 nW	49
EMTCMOS DFF	Vdc = 1.8v,Vth = 0.9 v	101	1.797 nW	36

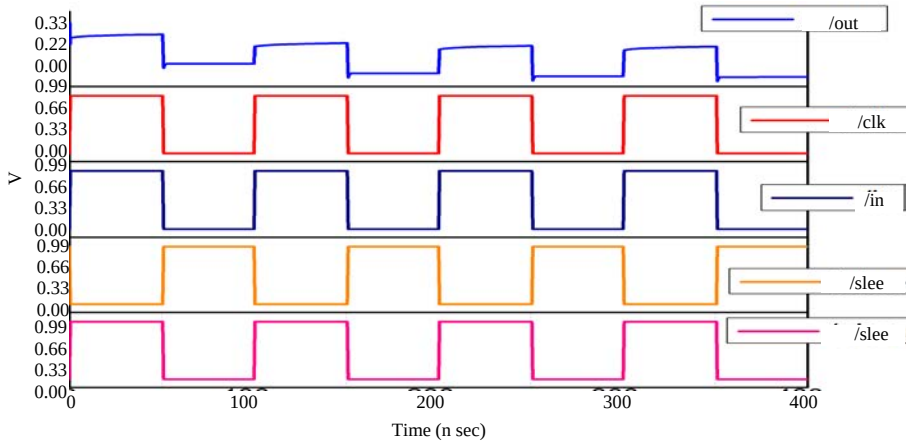

Fig. 7: The output waveform of MTCMOS DFF 45 nm technology

Fig. 8: The output waveform of EMTCMOS DFF 45 nm technology

Table 3: Comprehensive analysis of MTCMOS and EMTCMOS D FF with respect to differential supply and threshold voltages at 90 nm technology

Name of the design	Supply voltages and threshold voltages	Leakage current (Amp, pA)	Average power (W)	Delay (sec, nS)
MTCMOS D FF	Vdc = 0.3v,Vth = 0.15 v	2.2	149 pW	105
EMTCMOS DFF	Vdc = 0.3v,Vth = 0.15 v	0.9	136 pW	99
MTCMOS D FF	Vdc = 0.5v,Vth = 0.25 v	4.2	738 pW	92
EMTCMOS DFF	Vdc = 0.5v,Vth = 0.25 v	1.2	526 pW	86
MTCMOS D FF	Vdc = 1v,Vth = 0.5 v	6.4	1.62 nW	84
EMTCMOS DFF	Vdc = 1v,Vth = 0.5 v	2.33	1.44 nW	51.3
MTCMOS D FF	Vdc = 1.2v,Vth = 0.6 v	8.1	1.97 nW	78
EMTCMOS DFF	Vdc = 1.2v,Vth = 0.6 v	3.1	1.78 nW	67
MTCMOS D FF	Vdc = 1.5v,Vth = 0.75 v	92	2.48 nW	68
EMTCMOS DFF	Vdc = 1.5v,Vth = 0.75 v	8.82	2.32 nW	54
MTCMOS D FF	Vdc = 1.8v,Vth = 0.9 v	166	3.03 nW	61
EMTCMOS DFF	Vdc = 1.8v,Vth = 0.9 v	110	2.919 nW	48

Table 4: Comparative analysis of MTCMOS D FF Ripple counter and EMTCMOS D FF Ripple counter with respect to differential supply and threshold voltages at 90 nm technology

Name of the design	Supply voltages and threshold voltages	Leakage current (Amp, pA)	Average power (nW)	Delay (sec, nS)
MTCMOS D FF	Vdc = 0.3v,Vth = 0.15 v	120 nA	2.8	34
EMTCMOS DFF	Vdc = 0.3v,Vth = 0.15 v	80 nA	2	29
MTCMOS D FF	Vdc = 0.5v,Vth = 0.25 v	346 nA	4	28
EMTCMOS DFF	Vdc = 0.5v,Vth = 0.25 v	250 nA	3.1	25
MTCMOS D FF	Vdc = 1v,Vth = 0.5 v	1.2 uA	27.04	16.9
EMTCMOS DFF	Vdc = 1v,Vth = 0.5 v	1 uA	26.5	11
MTCMOS D FF	Vdc = 1.2v,Vth = 0.6 v	5 uA	132.6	15
EMTCMOS DFF	Vdc = 1.2v,Vth = 0.6 v	4.13 uA	60.21	9
MTCMOS D FF	Vdc = 1.5v,Vth = 0.75 v	8.9 uA	149.1	8.2
EMTCMOS DFF	Vdc = 1.5v,Vth = 0.75 v	7 uA	141.2	7.8
MTCMOS D FF	Vdc = 1.8v,Vth= 0.9 v	13 uA	302	5.5
EMTCMOS DFF	Vdc = 1.8v,Vth = 0.9 v	11 uA	279.8	4.3

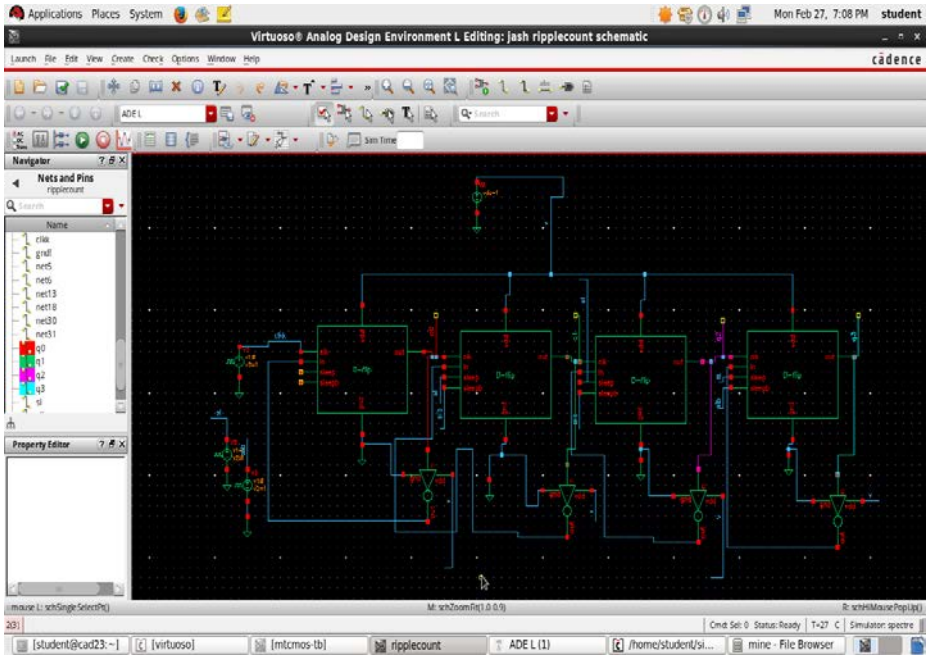

Fig. 9: Design of emtcmos ripple counter at 90 nm technology

variable supply voltages. Table 3 shows the comprehensive analysis of the results obtained at different submicron technology with the set of voltage variables (Fig. 9).

The overall analysis reveals that the power consumption, leakage current and delay values of EMTCMOS D FF are better when compared with MTCMOS DFF at 180, 90 and 45 nm technology. The

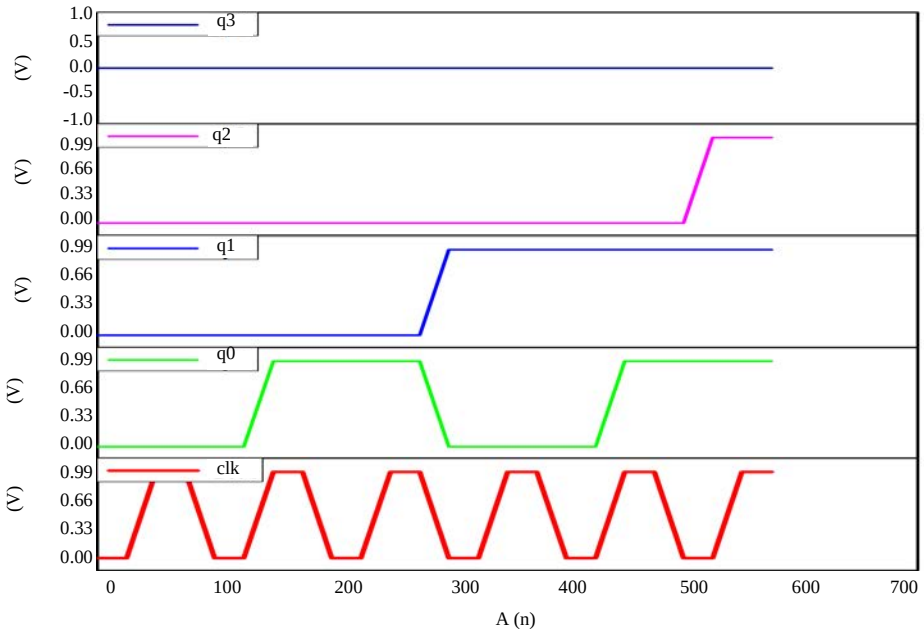

Fig. 10: Output waveform of ripple counter

results also establish the fact that higher threshold voltages in non critical paths yield reasonably better power consumption values. Delay values are observed exceptions in some cases as mentioned earlier. At threshold voltage value of 0.25 v, i.e., is in general considered as ultra low power analysis of the circuit also the EMTCMOS D FF design obtained better power consumption values and delay values is another significant observation. So, this EMTCMOS D FF performs is better not only with distinct technologies but also with variable voltages and ultra low power values, which is an encouraging aspect for the research in this domain.

Figure 9 represents the modulo 4 ripple counter designed using EMTCMOS D Flip-flop at 180nm technology, whereas Fig. 10 represents the output waveform of the counter.

CONCLUSION

This research is resulted in the effective analysis of the performance of the D flip-flop in terms of average power consumption and delay. The results proved that EMTCMOS is better in performance when compared with MTCMOS. The technique of using the combination of varied supply and threshold voltages yielded better values of power consumption and delay which is crucial for the flip-flop circuit. This is also extended to the ripple counter circuit and encouraging results are obtained. The comparative analysis of this work at 180, 90 and 45 nm projected the pitfalls in the performance of the circuit with respect to technology scaling in terms of power consumption, leakage current and delay. This research is going to be significant for the design of higher complexity memory circuits using this method and this comprehensive analysis of D flip-flop performance can change the pace in which the research is taking place in this domain.

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