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Study of Waveform Sampling Front-End ASIC Development for GSO/APD with DOI Information

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Abstract: Study of Waveform Sampling Front-End (WSFE) Application Specific Integrated Circuit (ASIC) development for GSO/APD with DOI Information has been presented in this research. This study confined to a detector module multi-array avalanche photodiodes (APD) with GSO crystal for high resolution animal PET, Depth-of-Interaction (DOI) information by pulse shape discrimination and multi-channel waveform sampling front-end ASIC. Study reveals that APD has shown better performance compared with PMTs for a given geometry and radiopharmaceuticals while individual readout of detector have better resolution and counting rate over light sharing or charge division schemes. Each channel of the WSFE ASIC which has been fabricated on a 4.9×4.9 mm wafer using Rohm 0.35 μ CMOS ASIC development technology comprises of a preamplifier, a Variable Gain Amplifier (VGA) and a fast Analog to Digital Converter (ADC) to digitize signals from the APD. Micrograph, design specifications, performance and test results of the WSFE chip for individual components have been presented as well.

INTRODUCTION

An Application-Specific Integrated Circuit (ASIC) is an Integrated Circuit (IC) chip customized for a particular use, rather than intended for general-purpose one. ASIC chips are typically fabricated using Metal-oxide-Semiconductor (MOS) technology as MOS integrated circuit chips. The maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 logic gates to over 100 million. Modern ASICs often include entire microprocessors, memory blocks including ROM, RAM, EEPROM, flash memory and other large building blocks. The detector module for animal PET based on APDs has been described followed by the designs and test results of a prototype and an improved front-end ASIC. Finally, the test results from several preamplifiers fabricated in a separate chip are reported[1].

By Yeom *et al.*[2], the test results of a new 9-channel Waveform Sampling Front-End (WSFE) ASIC and experiments performed with this chip for readout of GSO scintillating crystal coupled to an avalanche photo-diode (APD). Study of micrograph, design specifications, performance and results of the waveform sampling front-end (WSFE) application specific integrated circuit (ASIC) development with GSO/APD as well as DOI Information for individual components have been presented in the current research.

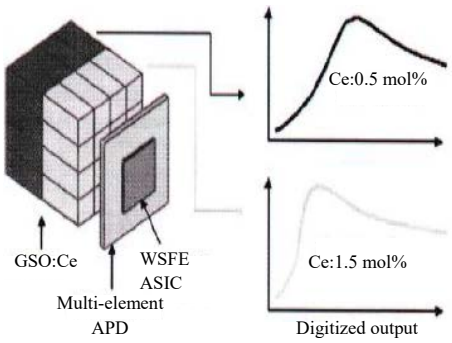

Fig. 1: The proposed detector module for DOI information. A third layer of GSO with Ce doping of 1.0 mol% can be added if pulse shape discrimination is possible

METHODOLOGY

Study of Waveform Sampling Front-End (WSFE) Application Specific Integrated Circuit (ASIC) development for GSO/APD with DOI Information has been presented in this research. As the choice of scintillators for the detector, GSO:Ce is a promising choice because the concentration of Ce dopant determines its decay time[3]. GSO with Ce-dopant concentrations of 0.5 and 1.5 mol.% has decay time constants of 60 and 35 nsec, respectively. The proposed detector module is shown in Fig. 1. Each detector module consists of two or more crystal types with different decay times that are stacked as in a phoswich detector where each crystal of the bottom layer is coupled to a pixel of a multi-element APD for individual readout[4].

DESIGN SPECIFICATIONS OFTHE WSFE CHIP

The 10-channel WSFE ASIC has been fabricated on a 4.9×4.9 mm die using Rohm 0. 35 µ CMOS ASIC technology through VLSI Education and Development Center of the University of Tokyo. The micrograph of the WSFE ASIC has been shown in Fig. 2.

Preamplifier: The preamplifier is based on the telescopic cascade topology[5]. The performance of the preamplifier is summarized in Table 1.

VGA: The input stage of the VGA is the same as that of the preamplifier to eliminate offset errors. The gain can be varied through two external pins and the results are shown in Table 2. The l0-90% rise time is 20 nsec.

ADC: Since, the ADC consumes the most power in the WSFE chip, a 6-bit folding ADC which greatly reduces the number of comparators (7) needed compared to a flash ADC (63) has been implemented[6]. The folding ADC

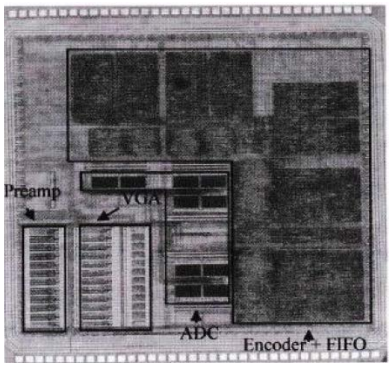

Fig. 2: Micrograph of the 10-ch WSFE ASIC

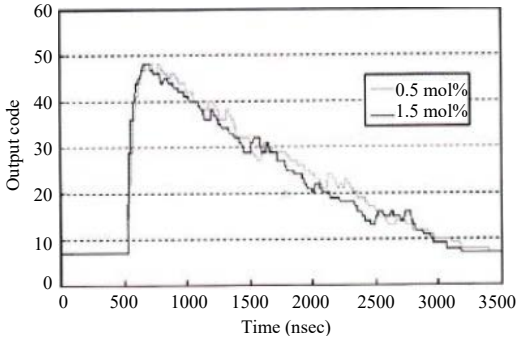

Fig. 3: Typical digitized output of GSO crystals with 0. 5 and l. 5 mol% Ce doping seen in a logic analyzer

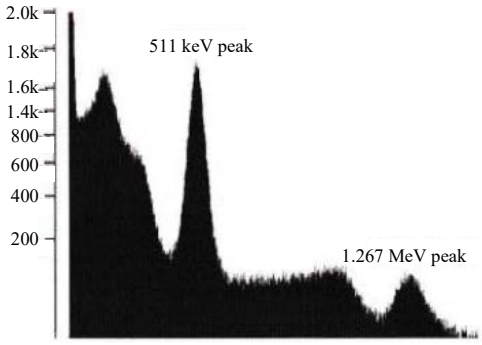

Fig. 4: Energy Spectrum of Na-22 source obtained at 360 V

Table 1: Summary of preamplifier parameters

Parameters	Specification
Gain	1.2/pF
Rise time	20 nsec (Cin = 0 pF)
Linearity	<0.5% (-0.6 to 1.5 pC)
ENC (0.25 µsec)	1130 e^-+35e^-/pF FWHM

was tested to be working up to 60 M samples/s. However, all experiments in this report were performed with a 50 MHz clock. The differential nonlinearity (DNL) and integral nonlinearity (INL) are l.l and 1.4 LSB, respectively (Fig. 3-5).

Fig. 5: The 40-ch WSFE board made with prototype WSFE ASICs. The board consists of four bare chips, a FPGA (Altera Flex) and USB controller, etc.

Table 2: First stage of the VGA

VGA gain control input	Gain
00	3.6
01	6.9
10	10.0
11	12.7

CONCLUSION

The article Yeom *et al*.[1] reported that each component of the prototype WSFE chip was working with the insufficient performance for their system. After careful considerations of the layouts and testability of the chip, a significantly improved second chip was fabricated, although, further modifications seem inevitable. Yeom *et al*.[2] described that multi-channel WSFE ASIC chip has been successfully developed to readout and digitized signals from individual pixel of a multi-array APD. The rising edge of signals from 0.5 and 1.5 mol% Ce-doped GSO crystals could be distinguished for DOI information. A board has been developed with prototype WSFE chips for this purpose.

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