Journal of Engineering and Applied Sciences 2 (5): 859-863, 2007

A Novel Technique for Canceling Maternal ECG from Fetal ECG Using Virtex FPGA

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Abstract: Abdominal elcetrocardiograms make it possible to determine the fetal heart rate and to detect multiple fetuses and are often used during labor and delivery.The background noise due to muscular activity and feotus motion, however, often had an amplitude equal to or grater than that of fetal heartbeat. A still more serious problem is the mother's heart beat, which has an amplitude 2-10 times grater thatn that of the fetal heartbeat and often interferes in recording. The Maternal ECG (MECG) is the main source of interference in Fetal ECG (FECG) monitoring. The MECG is detected at all electrodes placed on the mother's skin (thoracic and abdominal). The noise is found to be too strong for the algorithm (and the naked eye) to notice any fetal heart signal. This study briefs the implementation of Adaptive noise cancellation algorithms such as LMS algorithm using MATLAB suitable for real time implementation, which can be used during measurements and developed using VLSI.

Key words: Adaptive filters, ECG extraction, FECG, MECG, FPGA

INTRODUCTION

The monitoring of FECG has clinical importance. If the physician could obtain a reliable reading of the FECG, he could detect problems in the fetal heart activity even before he is born. The fetal heart is a small heart so that the electrical current it generates is very low. Presently, in order to record the FECG, electrodes are placed on the maternal abdomen as close as possible to the fetal heart. Hence, the FECG is acquired by placing a number of electrodes around the general area of the fetus and hoping that at least one of the electrodes has the FECG with high enough SNR (Emmanuel and Barrie, 2002).

Besides the problem of electrode placement, noise from electromyographic activity effects the signal due to the fetus low voltage signal. Another interfering signal is the Maternal ECG (MECG) which can be 5-10 times higher in its intensity and has the ability to induce surface potentials (Barnard and Samuel, 2002). The MECG effects all the electrodes, that are placed on the chest (thoracic electrodes) and those placed on the abdomen (abdominal electrodes) of the mother. Because the FECG is a very weak signal, an electrode placed on the thorax of the pregnant woman will hardly record any of it, if at all (Kam and Cohen, 1998).

The best solution for this situation is the filtering. The filters used are of two types namely, fixed and adaptive. The fixed fitlers impose an additional criterion that the characteristics of the signal shouild be known prior in hand. The adaptive filtering has an obvious advantage that its coefficients can adjust automatically as shown in Fig 1. There may be a million dollar question in the minds so as why not the conventional filtering but not the adpative filtering. The main disadvantage that prohibits the use of the conventional filtering is that the interfereng signals are all in the same bandwidth. Moreover the ECG signals are non stationary in nature. Hence the best and apt solution for this is the adaptive filtering.

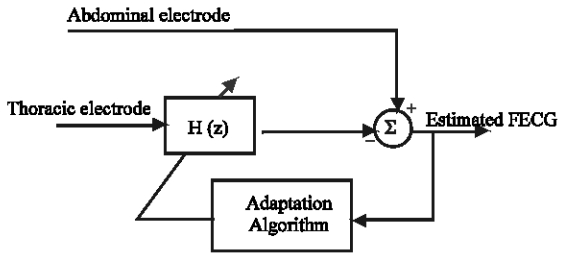

Fig. 1: Adaptive scheme for MECG cancellation

SINGLE FETUS EXTRACTION

This fact implies that an adaptive cancellation algorithm may be employed. An illustration of this conventional approach is given in Fig 1. The maternal ECG interfered fetal ECG can be obtained by placing electrodes anywhere in the general abdomen. The reference maternal ECG is obtained using thoracie electrode. These are then passed into adaptive noise

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canceller as shown. Alternatively, four ordinary chest leads can also be used to record the mother's heartbeat which provides multiple reference inputs to the canceller. A single abdominal lead is used to record the combined maternal and fetal ECG that served as the primary input. Multichannel adaptive noise canceller is used in this case.

ADAPTIVE FILTER ALGORITHM

An adaptive Filter is essentially a digital filter with self-adjusting characteristics When, there is a spectral overlap between the signal and noise and the band occupied by noise is unknown or varies with time, adaptive filters can be modeled as a NOISE CANCELLER (Emmanuel and Barrie, 2002). Let us assume that Sk and Nk are uncorrelated with each other. The desired signal estimate is found out by,

$$S_{1k} = Y_k - N_{1k} \rightarrow \quad (1)$$

$$S_{1k} = S_k + (N_k - N_{1k}) \rightarrow \quad (1.1)$$

The estimate of Nk is obtained by,

$$N_k = W_k(i)\, X_{k-i} \rightarrow \quad (2)$$

Wk(i) is adjustable filter coefficients (Bernard and Samuel, 2002). Adaptive algorithms are used to adjust the co-efficient of digital filter so that the noise is minimized.In LMS algorithm, a weighted sum of all the observations is used as an estimate of desired signal by using weight vectors and as current input samples (Haykins, 1996). The Computational procedure for the LMS algorithm (Emmanual and Berrie, 2002) is, Initially set each weight $W_k(i)$, i = 0,1,2,3....n-1 to an obituary fixed value such as zero. For each subsequent sampling instant, k =1,2,3... carry out steps (2) to (4) below and Compute filter output:$N_k = \Sigma\, W_k\,(i)\, X_{k-I}$ and then Compute the error estimate:$e_k = S_k = Y_k - N_{1k}$ and finally Update the next filter weights using

$$W_{k+1}\,(i) = W_k(i) + 2\mu\, e_k\, X_{k-i}.$$

RESULTS AND DISCUSSION

The MATLAB program responded for both original ECG as well as manually generated ECG. However, the response of the program for the original ECG is more apt. Although the Maternal ECG is uncorrelated with the Fetal ECG, the adaptive technique proved worthy. The Maternal ECG Singal (i.e.,) Inteterference is cancelled from the fetal heart ECG Signal. ECG Signals are given as an input and is simulated using MATLAB. The result of the program is shown in the Fig. 2.

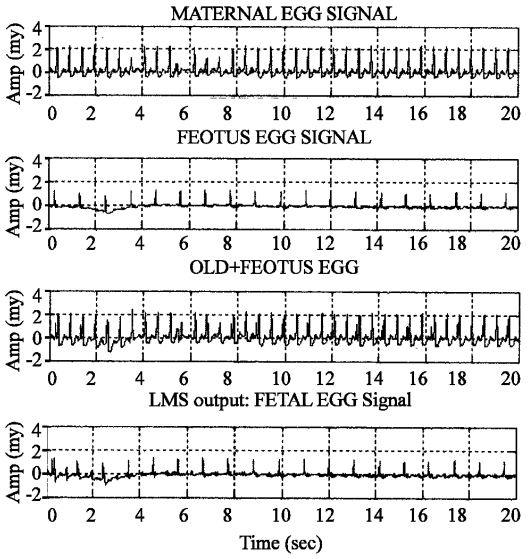

Fig. 2: LMS algorithm output

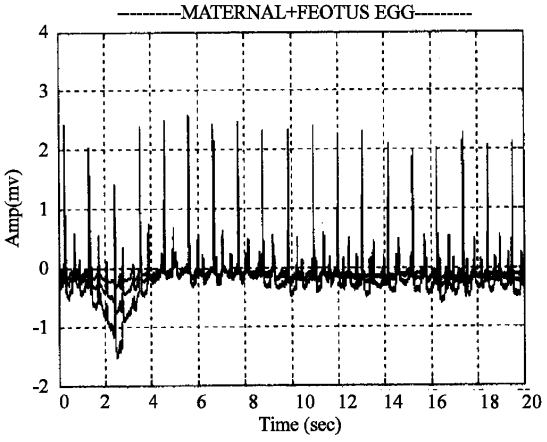

Fig. 3: Abdominal electrode signal

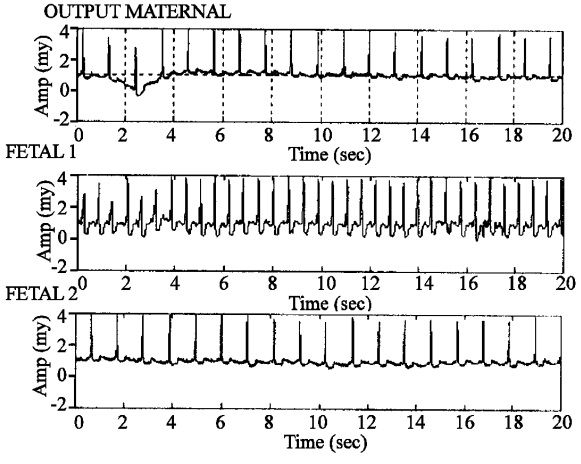

Fig. 4: Obtained output signal

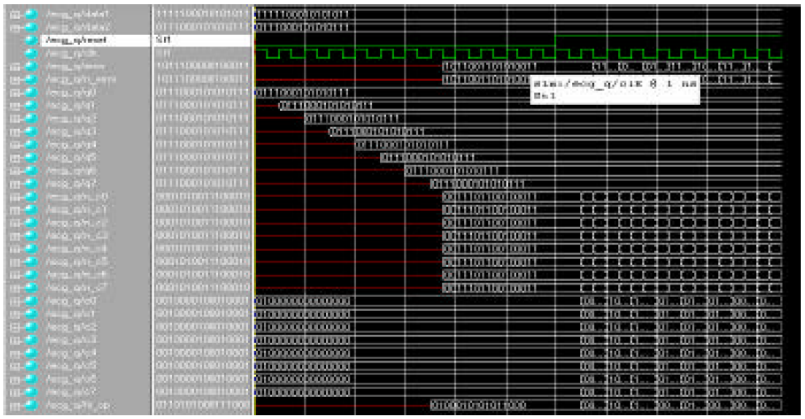

Fig. 5: Timing diagram of LMS algorithm

In order to study the problem, simulation studies were performed. Two ECG signals taken from three persons (men or non-pregnant women) were chosen to simulate each source (MECG, FECG1). The MECG was about ten times larger in amplitude from the FECG1. One of the observations was simulated as a thoracic electrode and the other two as abdominal ones. The matlab simulation results as shown in Fig. 2-4. were very encouraging and suggesting the method for real signals.

With the growing complexity of the logic circuits that could be packed on an FPGA chip, having automatic synthesis tools that implement logic functions has become indispensable on these architectures (Lok-Kee and Rogger 2005). Conventional synthesis approaches fail to produce satisfactory solutions for FPGAs, since the constraints imposed by the FPGA architectures are quite different.

The design is coded in Verilog HDL (hardware description language), a more generalized method of describing the behavior of logic systems than logic equations. The system was visualized as a set o f black boxes called modules. The top level module is broken into successively less complex functions until the bottom level is reached (RTL level description of the function). The LMS algorithm is simulated and examined to assess whether the simulation has achieved the desired result using Modelsim 5.8. Its equivalent timing diagram is shown in Fig. 5.

Logic synthesis takes the circuit description at the register-transfer level and generates an optimal implementation in terms of an interconnections of logic gates. Schematic capture is, probably, still most popular method of defining l ogic for FPGAs and many ASICs. It is a CAD systems dedicated to logic design. L ogic 8functions of complexity ranging from an inverter to multi-bit counters are stored in a

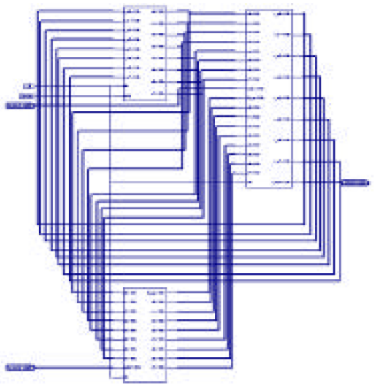

Fig. 6: Synthesis result

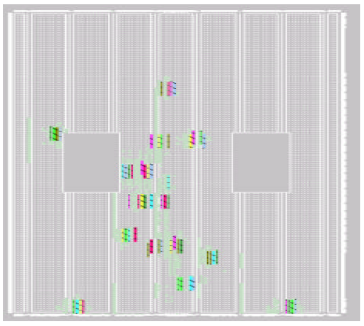

Fig. 7: Floorplanning report in FPGA

library which describes both their functionality and a graphic symbol. The designer calls up the symbols from the library, places them on the screen of a PC or workstation and connects them with wires and busse (Meyer, 2006).

The RTL description of LMS algorithm is first optimized for an objective function such as minimum chip area, meeting the performance constraints, low power, etc.

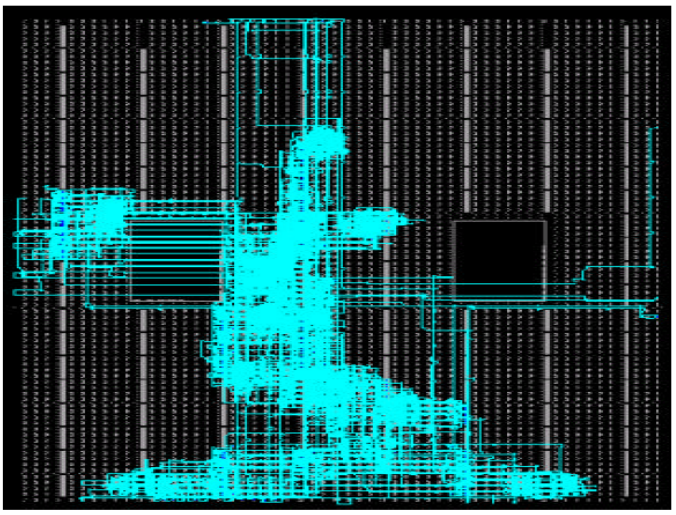

Fig. 8: Implementation report in FPGA

Table 1: Characteristics of LMS

Architecture	Registers	Adders/Subtractors	Multipliers	Comparators
LMS	137	46	24	15

Table 2: Characteristics of LMS

Architecture	Gatecount	Power	Frequency	IOB's	Memory Usage
LMS	113423	798 mW	18 MHz	2400	146 MB

Table 3: Device utilization summary of LMS

Device utilization summary of LMS		
Selected Device : 2vp40ff1148-6		
Number of External IOBs	50 out of 556	8 (%)
Number of LOCed External IOBs	0 out of 50	0(%)
Number of MULT18×18s	24 out of 136	17 (%)
Number of SLICEs	996 out of 13696	7 (%)
Number of BUFGMUXs	1 out of 16	6

This step is called logic optimization. The optimized representation is then mapped to some primitive cells present in a library. The final implementation is in terms of interconnections of gates, functional units, registers, is synthesized in Xilinx 6.3i and implemented on a Virtex XC2VP40-6 chip is shown in Fig 6.

The objectives of floorplanning are to minimize the chip area and minimize delay (Micharel, 2001). The LMS algorithm is floor planned and its result is shown in Fig. 7.

The locations of various modules on the chip are determined (placement)and the interconnections of the circuit are routed between or through the placed modules. Also, the pad locations for inputs and outputs are determined in this step (Michael, 2001). The final layout is sent for fabrication and the layout for the LMS algorithm is shown in Fig. 8.

The timing simulation data generated from Place and Route are generated to carry out the timing simulation for the final verification of the design. Best performance is achieved by mapping the basic components to use the minimum Array-of-Slices (AoSs) (Parhi, 1999). The arrangement of the component's position in the Virtex device is important in minimizing the interconnect delay. The components used to implement the Filtered X-LMS have been optimized for the Virtex FPGA circuit. Characteristics of LMS algorithm and the device utilization table is given below (Table 1-3).

CONCLUSION

Although the science is the mastermind of today's activities, there are still situations where certain obvious problems are unanswered. One such is the measurement of the fetal ECG. This is a vital part of the diagnosis when the mother has had some kind of accidents or even illness. In such cases, the main source to check the proper working of the fetal heart is its ECG. In such cases, the cancellation of Maternal ECG from the Fetal ECG is more important in case of further processing of the signal; because the interference causes the Fetal ECG to be dispersed and distorted due to the high amplitude of Maternal ECG. This makes unreliable data on which any diagnosis could be made. Further, this paper is enhanced using VLSI high-speed FPGA implementation. The LMS algorithm has been successfully implemented on the Virtex:2vp40ff148-6.chip. The powerful design of LMS algorithm using reconfigurable logic shortens the design cycle and provides good utilization of the device and also provides synthesizer options, i.e., chooses between optimization speed versus size of the design. As inferred from speed analysis, the LMS algorithm, exhibits considerably more speed consumption at the RTL coding stage and other data prove to be exceptional. The MATLAB results also prove that it is effective. This implementation gives a better way for extracting the Fetal ECG in order to check the working of the fetal heart.

ACKNOWLEDGEMENT

The authors thank Dr. S.Thangavelu, Chairman, Shri Shakthi Institute of Engineering and Technology, Coimbatore for the guidance, support and providing research facilities.

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