Journal of Engineering and Applied Sciences 5 (4): 252-256, 2010
ISSN: 1816-949X

Small-Signal Modeling of pHEMTs and Analysis of their Microwave Performance

[1]Z. Hamaizia, [1]N. Sengouga, [2]M. Missous and [3]M.C.E. Yagoub
[1]Laboratory of Metallic and Semiconductor Materials, University of Biskra, 07000 Biskra, Algeria
[2]Microelectronic and Nanostructure Group,
School of Electric and Electronic Engineering, University of Manchester, UK
[3]SITE, University of Ottawa, 800 King Edward, Ottawa, Ontario, K1N 6N5, Canada

Abstract: Accurate extraction of the small-signal equivalent circuit of GaAs microwave Field Effect Transistors (GaAs FET) is crucial for efficient design of microwave analog circuits such as Low Noise Amplifiers (LNAs). This study proposed an improved direct analytical extraction procedure. Its efficiency was demonstrated through the characterisation of two 1 μm gate-length pseudomorphic heterojonction transistors.

Key words: pHEMT, extraction, small signal modeling, LANs, GaAs FET, Canada

INTRODUCTION

Microwave amplifiers constitute an area of prime interest for the high-frequency industry. Most of them use III-V semiconductors such as Gallium Arsenide (GaAs) and Indium Phosphide (InP) because of their higher performance in terms of gain and noise. At the component level, pseudomorphic Heterojonction Transistors (pHEMTs) are widely used in Monolithic Microwave Integrated Circuits (MMICs). The aim of this study is the modeling of such transistors subsequently used to design a low-noise amplifier.

MATERIALS AND METHODS

Small signal equivalent circuit: One of the most widely used small-signal HEMT equivalent circuit is shown in Fig. 1 (Dambrine and Cappy, 1988; Berroth and Bosh, 1990; Anholt and Swirhun, 1991a). According to its structure and operation mode, this circuit can be divided into two parts namely the intrinsic and the extrinsic parts. The intrinsic part corresponds to the active part of the transistor i.e., the channel. The extrinsic part corresponds to the connecting zone (access lines and electrode components).

Extraction of small signal parameters: Determination of the elements of a linear model is based on an experimental characterization of the transistor. The small-signal extraction method proposed in this study is based on S-parameters measurements. It involves the use of 2 sets

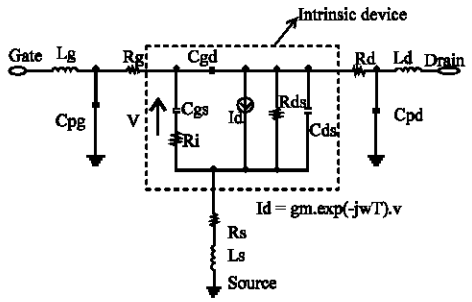

Fig. 1: Small signal equivalent circuit of a HEMT

of measurements at different bias conditions; pinched or cold and hot device measurements. The measured S matri is converted to a impedance matrix (Z) whose elements Z_{ij} have real and imaginary part: real (Z_{ij}) and imag (Z_{ij}) (Freckey, 1994).

The extrinsic elements can be obtained from S-parameters measurements under cold and pinched off biasing conditions: a zero drain source voltage V_{ds} and a gate source voltage much lower than the pinch-off voltage V_p (i.e., V_{ds} = 0 V and $V_{gs} << V_p$). In fact, cold pinched off bias conditions can simplify the topology of the small signal equivalent circuit as shown in Fig. 2. For more efficiency, the π circuit model in Fig. 2 can be transformed to a T circuit (Caddemi *et al*., 2006; Anholt and Swirhun, 1991b). Thus, the Z-parameters Z_{pij} can be expressed as:

$$Z_{p11} = R_g + R_s + j*\left[\omega(L_g + L_s) - \frac{1}{\omega}\left(\frac{1}{C_g} + \frac{1}{C_s}\right)\right] \quad (1)$$

Corresponding Author: Z. Hamaizia, Laboratory of Metallic and Semiconductor Materials, University of Biskra, 07000 Biskra, Algeria

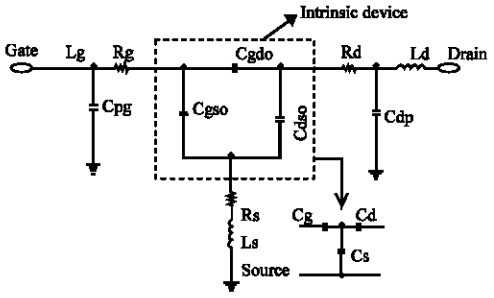

Fig. 2: Small signal equivalent circuit of HEMT at zero drain bias and gate voltage pinch-off

$$Z_{p12} = Z_{p21} = R_s + j*\left[\omega L_s - \frac{1}{\omega C_s}\right] \quad (2)$$

$$Z_{p22} = R_d + R_s + j*\left[\omega(L_d + L_s) - \frac{1}{\omega}\left(\frac{1}{C_s} + \frac{1}{C_d}\right)\right] \quad (3)$$

Where, subscript p is pinched off condition. In order to simplify the circuit analysis, the capacitive π network is transformed into a T network consisting of 3 capacitances C_g, C_s and C_d (Caddemi *et al.*, 2006; Anholt and Swirhun, 1991b; Khalaf, 2000):

$$C_g = C_{gso} + C_{gdo} + \frac{C_{gso}C_{gdo}}{C_{dso}} \quad (4)$$

$$C_s = C_{gso} + C_{dso} + \frac{C_{gso}C_{dso}}{C_{gdo}} \quad (5)$$

$$C_g = C_{gso} + C_{gdo} + \frac{C_{gso}C_{gdo}}{C_{dso}} \quad (6)$$

The parasitic resistances R_g, R_s and R_d can be deduced from the real part of 1, 2 and 3 (Khalaf, 2000). The parasitic inductances L_g, L_s and L_d can be extracted from the slope of the curve of ω* imag (Z_{pij}) vs. ω^2 (Caddemi *et al.*, 2006; Khalaf, 2000; Chen *et al.*, 2006; White and Healty, 1993). When the conduction in the channel is removed (i.e., deeply in pinch off $V_{ds} = 0$, $V_{gs} << V_p$), it is possible to extract the parasitic (extrinsic) capacitances C_{pg} and C_{pd}.

Frequencies of some GHz, the effects due to parasitic inductances and resistances can be neglected and thus have little influence on the imaginary parts of the admittance matrix, assuming $C_{gso} = C_{gdo}$ and neglecting C_{ds} (Dambrine and Cappy, 1988; Freckey, 1994; Anholt and Swirhun, 1991b; White and Healty, 1993; Chigaeva *et al.*, 2000). We can write these equations:

$$C_{pg} = \frac{\text{Imag}(Y_{11}) + 2*(\text{Imag}(Y_{12}))}{\omega} \quad (7)$$

$$C_{pd} = \frac{\text{Imag}(Y_{22}) + \text{Imag}(Y_{12})}{\omega} \quad (8)$$

Once all the extrinsic elements are determined, we can directly extract the intrinsic elements (R_i, C_{gs}, C_{gd}, R_{ds}, C_{ds}, G_m and τ) from the intrinsic Y-parameters according to the expressions proposed by Dambrine and Cappy (1988), Berroth and Bosh (1990), Khalaf (2000), Chigaeva *et al.* (2000), Shirakawa *et al.* (1995) and Wurtz (1994):

$$C_{gs} = \frac{(1 + d_1^2)}{\omega} * (\text{Imag}(Y_{\text{int}11}) + \text{Imag}(Y_{\text{int}12}) \quad (9)$$

$$R_i = \frac{d_1}{(1 + d_1^2) * (\text{Imag}(Y_{\text{int}11}) + \text{Imag}(Y_{\text{int}12})} \quad (10)$$

$$C_{gd} = -\frac{(1 + d_2^2)}{\omega}\text{Imag}(Y_{\text{int}12}) \quad (11)$$

$$R_{gd} = -\frac{d_2}{(1 + d_2^2) * \text{Imag}(Y_{\text{int}12})} \quad (12)$$

$$C_{ds} = \frac{\text{Imag}(Y_{\text{int}22}) + \text{Imag}(Y_{\text{int}12})}{\omega} \quad (13)$$

$$g_{ds} = \text{Real}(Y_{\text{int}22}) + \text{Real}(Y_{\text{int}12}) \quad (14)$$

$$g_m = |G_m| \quad (15)$$

$$\tau = -\frac{1}{\omega}\angle(G) \quad (16)$$

Where:

$$d_1 = \frac{\text{Real}(Y_{\text{int}11}) + \text{Real}(Y_{\text{int}12})}{\text{Imag}(Y_{\text{int}11}) + \text{Imag}(Y_{\text{int}12})}$$

$$d_2 = \frac{\text{Real}(Y_{\text{int}12})}{\text{Imag}(Y_{\text{int}12})}$$

$$G = g_m * \exp(-j\omega\tau) = (Y_{\text{int}21} + Y_{\text{int}12})(1 + j * d_1)$$

Description of device technology: The fabricated high breakdown InGaAs-InAlAs-InP pHEMT (sample-1841) and InGaAs-AlGaAs-GaAs pHEMT (sample-1891) were chosen for this research.

These devices with 1 μm gate length and 200 μm (2×100 μm) gate width are used. The epitaxial layer structure of the used device is shown in Fig. 3. Looking at

the structure from bottom to top, a lattice-matched undoped InAlAs buffer layer of thickness 4500 Å is grown on top of an InP semi insulating substrate. A highly strained, undoped InGaAs, channel is grown well below the critical thickness of this composition (140 Å). The spacer is a lattice matched, undoped InAlAs layer of thickness 100 Å used to spatially separate the heavily doped delta-region from the active channel. A supply layer is formed with thickness 150 Å to supply electrons into the 2DEG with Delta-doping sheet density of 3.6×10^{12} cm^{-2}.

Noise figure characterization: The main target of the fabricated devices (GaAs and InP HEMTs and pHEMTs) is the design and implementation of broadband low noise amplifiers for SKA applications. Thus, it is important to get an accurate analytic expression for calculating the minimum noise figure of these devices. Since, the noise figure of a FET is affected by both bias point and generator impedance, the minimum noise figure, NF_{min} defined here is an absolute minimum noise figure obtained by adjusting both bias and generator impedance.

Using the four equivalent element values Gm, Cgs/Fc Rs and Rg, determined by S-parameter measurement and small-signal parameter extraction Fukui empirically derived a simple expression for NF_{min}:

$$F_{min}(dB) = 10Log(1 + 2\pi k_f f C_{gs}\sqrt{\frac{(R_s + R_g)}{G_m}}) \quad (17)$$

K_f is a fitting factor which depends on the material system used. Applying this empirical form to the fabricated devices used in this study and comparing with experimentally measured NF_{min} for the same devices, the best extracted fit values for the fitting factor k is 2.8 for the GaAs based samples and 3.4-3.6 for the InP based samples, f is the frequency.

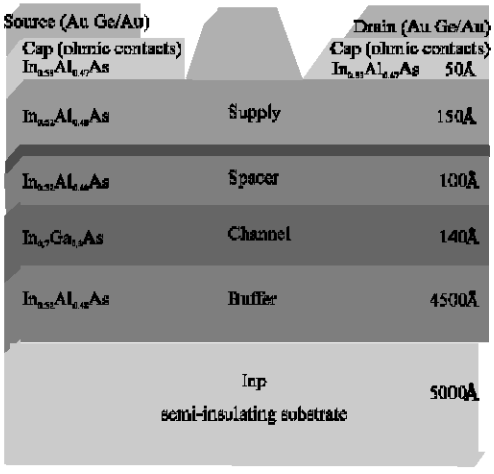

Fig. 3: Epitaxial layer structure of used transistor (Inp device)

RESULTS AND DISCUSSION

The direct method presented in this research was demonstrated through the extraction of the small-signal equivalent circuit of two pHEMTs. Practically, the values of the extrinsic components were optimized to best fit with measurements (Fig. 4). Table 1 shows the extrinsic and intrinsic element values of the small-signal equivalent circuit of the 2 following pHEMTs: the VMBE-1841-A132-InP (biased at V_{ds} = 1.5V and V_{gs} = -0.2V) and the VMBE-1891-A322-GAs (biased at V_{ds} = 0.5V and V_{gs} = - 0.4V). The curves displayed in Fig. 4 showed a good agreement between obtained and measured S-parameters (Table 2). It should be noted that the stability factor k as well as the maximum available gain G_{max} (with k≥1) or the most stable gain MSG (if k<1) are critical parameters for microwave circuits designers. By comparing the GaAs-pHEMT and the InP-pHEMT it is noted that the InP-pHEMT exhibits a lower minimum noise factor (NF_{min}) (Fig. 5 and 6), a higher gain G_{max} and a higher cut-off frequency F_c (Table 3):

Table 1: Extracted parameter values for the two transistors

	Devices	
Elements	VMBE-1841-A132-InP	VMBE-1891-A322-GaAs
R_g (Ω)	20.65	23.00
R_s (Ω)	2.60	5.77
R_d (Ω)	3.00	8.16
L_g (pH)	15.30	21.80
L_s (pH)	12.10	8.34
L_d (pH)	24.00	21.00
C_{pg} (fF)	2.20	1.47
C_{dpd} (fF)	30.00	34.00
R_i (Ω)	6.36	15.90
C_{gs} (fF)	506.00	291.00
C_{gd} (fF	25.20	60.00
R_{ds} (Ω)	285.00	585.00
C_{DS} (fF)	24.80	11.50
G_m (ms)	89.00	18.00
τ (ps)	1.86	2.84

Table 2: Errors between measured and modelled values of S-parameters

Error device	S_{11} (%)	S_{12} (%)	S_{21} (%)	S_{22} (%)
VMBE-1841-InP	5.27	7.37	5.41	2.06
VMBE-1891-GaAs	1.78	5.55	2.88	5.61

Table 3: Transistor performance parameters

	VMBE-1841 InGaAs-InAlAs-InP		VMBE-1891 InGaAs-AlGaAs-GaAs	
Device parameters	1 GHz	2 GHz	1 GHz	2 Ghz
$NF_{min\ measured}$ (dB)	0.661	1.255	0.805	1.526
$NF_{min\ simulated}$ (dB)	0.680	1.265	0.786	1.449
$k_{measured}$	0.432	0.804	0.292	0.546
$k_{simulated}$	0.252	0.504	0.259	0.516
$G_{max\ measured}$ (dB)	25.785	22.926	15.859	12.938
$G_{max\ simulated}$ (dB)	25.963	22.952	16.413	13.147
$S_{21\ measured}$ (dB)	15.371	14.224	2.900	2.410
$S_{21\ simulated}$ (dB)	15.602	14.829	3.248	2.458

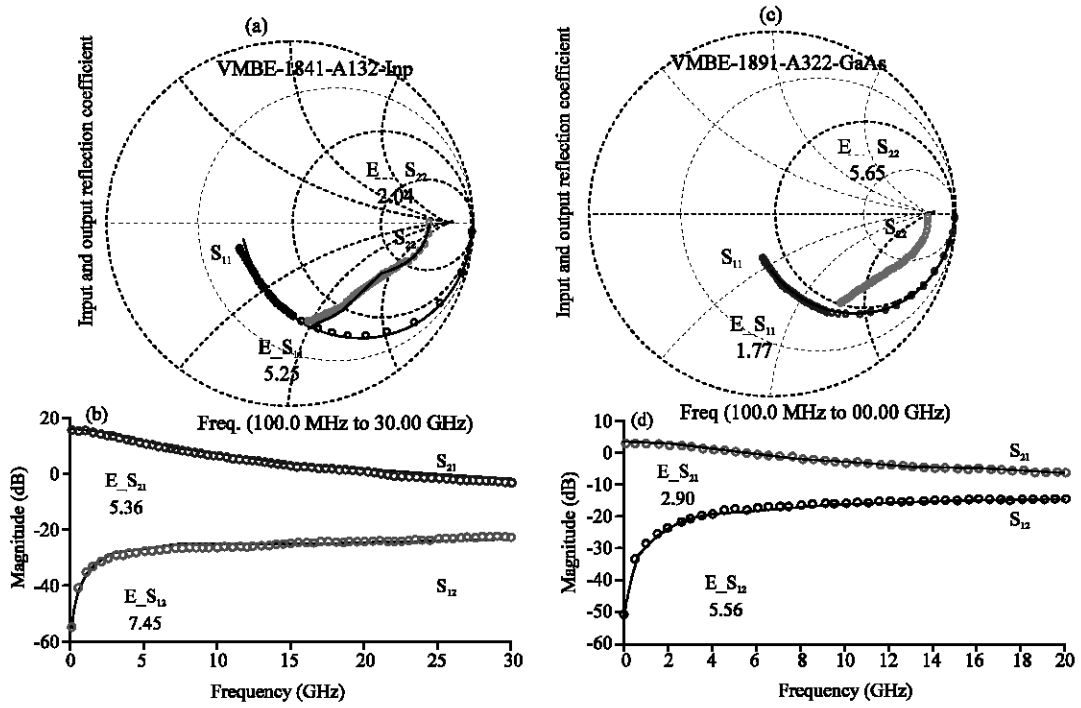

Fig. 4: Comparison between measured (circles) and calculated (lines) S parameters of pHEMT devices (a, b) VMBE-1841-A132-InP under the bias conditions: V_{ds} = 1.5V, V_{gs} = -0.2V (c, d) VMBE-1891-A322-GaAs under the bias conditions: V_{ds} = 0.5V, V_{gs} = -0.4V

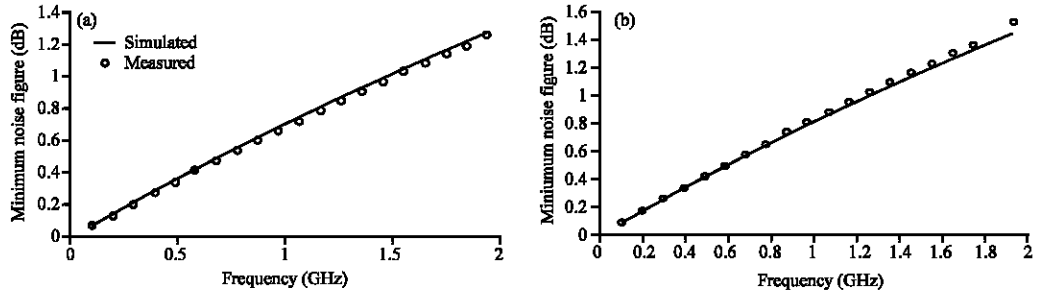

Fig. 5: Comparison of the measured minimum noise figure (room-temperature minimum noise figure of a 1×200 μm device from each sample up to 2 GHz) (circles) with minimum noise figure calculations based on Fukui's analysis (lines)

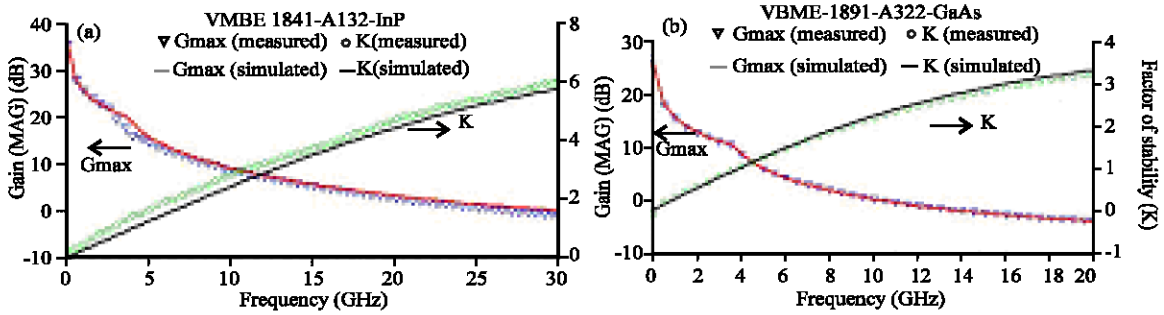

Fig 6: Maximum Gain G_{max}, stability factor K for the: (a) VMBE-1841-A132-InP under the bias conditions: V_{ds} = 1.5V, V_{gs} = -0.2V (b) VMBE-1891-A322-GaAs under the bias conditions: V_{ds} = 0.5V, V_{gs} = -0.4V

- InP-pHEMT: S_{21} = 14 dB, G_{max} = 22 dB, NF_{min} = 0.14 dB and F_C = 28 GHz
- GaAs-pHEMT: S_{21} = 2 dB, G_{max} = 13 dB, NF_{min} = 0.198 dB and F_c = 8.6 GHz

CONCLUSION

This research presents a direct extraction method of the elements of small signal equivalent circuit of 2 transistors PHEMT one on the GaAs substrate and the other on the InP substrate of which the length and the width of the gate, respectively 1 and 200 μm. This modelling is essential for any active or passive component and which precedes any design of a radio frequency circuit.

The technique suggested is of experimental type, rests to measures of the parameters of dispersion S, followed by a method of optimization with an aim of studying the linear behavior and the performances ultra high frequencies of the transistor. The results obtained show a good agreement between simulated and measured S parameters. The analysis of the performances ultra high frequencies such as the gain, the factor of noise NFmin and the frequency band justifies the choice of transistor pHEMT on the InP substrate for the application low noise.

REFERENCES

Anholt, R. and S. Swirhun, 1991a. Equivalent circuit parameter for cold GaAs MESFETs. IEEE Trans. Microwave Theory Tech., 39: 1243-1247.

Anholt, R. and S. Swirhun, 1991b. Measurement and analysis of GaAs MESFET parasitic capacitances. IEEE Trans. Microwave Theory Tech., 39: 1247-1251.

Berroth, M. and R. Bosh, 1990. Broad-band determination of the FET small-signal equivalent circuit. IEEE Trans. Microwave Theory Tech., 38: 891-895.

Caddemi, A., G. Crupi and N. Donato, 2006. Microwave characterization and modeling of packaged HEMTs by a direct extraction procedure down to 30K. IEEE Trans. Instrument. Measure., 55: 465-470.

Chen, G., V. Kumar, R.S. Schwindt and I. Adesida, 2006. A low gate bias model extraction technique for AlGan/GaN HEMTs. IEEE Trans. Microwave Theory Tech., 54: 2949-2953.

Chigaeva, E., W. Walth, D. Wiegner, M. Grozing and F. Schaich *et al*., 2000. Determination of small signal parameters of GaN based HEMTs. Proceedings of the IEEE/Cornell Conference on High Performance Devices, Aug. 7-9, Cornell University, Ithaca, USA., pp: 115-122.

Dambrine, G. and A. Cappy, 1988. A new method for determination the FET small-signal equivalent circuit. IEEE Trans. Microwave Theory Tech., 36: 1151-1159.

Freckey, D.A., 1994. Conversion between S, Z, Y, h ABCD and T Parameters which are valid for complex source and load impedances. IEEE Trans. Microwave Theory Tech., 42: 205-211.

Khalaf, Y.A., 2000. Systmatic optimization technique for MESFET modelling. Ph.D. Thesis, University of Virginia, USA.

Shirakawa, K., H. Oikawa, T. Shimura, Y. Kawasaka, Y. Ohasi and T. Saito, 1995. An approach to determining an equivalent circuit for HEMT's. IEEE Trans. Microwave Theory Tech., 43: 499-503.

White, P.M. and R.M. Healty, 1993. Improved equivalent circuit for determination of MESFET and HEMT parasitic capacitances from cold FET measurements. IEEE Microwave Guided Wave Lett., 3: 453-454.

Wurtz, L.T., 1994. GaAs FET and HEMT small-signal parameter extraction from measured S-parameters. IEEE Trans. Instrument. Measure., 43: 655-658.