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Design and Applications of Microprocessor Based Digital Filter

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Abstract: The purpose in this study is constructing digital filter with application of modern microprocessor systems, learning methods of automatic projecting and perfecting skills of programming in language of assembler. In this study, the microprocessor of firm MICROCHIP PIC16C711 is used which has possibilities of analog signal's processing. DAC is not a part of the microcontroller and it is carried out separately, its entrances are connected to port B. The program written in language of assembler is universal for all microcontrollers of MICROCHIP having a possibility for analog signal's processing. It is necessary to configure ports and to consider specification GPR (General Purpose Register) and special registers according to the documentation on demanded model.

Key words: Digital filter, microprocessor, signal processing, frequency-selective devices, register, assembler

INTRODUCTION

Digital signal processing is an arithmetical processing in real-time sequences values of signal amplitude (Concha *et al*., 2003) defined through equal temporary gaps. Examples of digital processing are signal filtering, convolution of two signals, calculation values of correlation function two signals and amplification, restriction or transformation of signal or forward/inverse fourier transformation.

The analog signal processing, traditionally used in all radio engineering devices is cheaper mode of achievement to demanded results in many cases. When high accuracy of processing, diminutiveness of the device and stability of its characteristics in various temperature conditions are required digital processing appears the unique good enough solution. The example of an analog filtering is showed in Fig. 1. The operational amplifier used in the filter allows to expand a dynamic range of handled signals. The form of amplitude-frequency characteristics of the filter is defined by sizes R2, C. For the analog filter, it is difficult to provide high value of good quality, characteristics of the filter strongly depend on a temperature condition. Components of the filter bring additional noise to resultant signal (Grossman and Morrisett, 2000). Analog filters are difficult for retuning in a wide frequency range. The major feature of the digital filter lies in the fact that with selection of the certain means of factors of difference equation describing output signal is possible to transformation input signal which will be impossible by using the analogue filter. The device realizing digital filtering will have compact sizes and will not demand special technical adjustment.

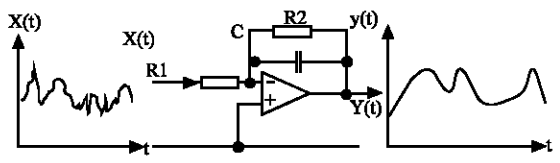

Fig. 1: Analog filtering of a signal

THE REVIEW OF SIMILAR DEVICES

Filters can be classified on their frequency characteristics. Figure 2 a-c shows the characteristics of the low-pass filter, the high-pass filter and zonal filter. The basic function of any filter consists in weakening the signals that lie in certain band of frequencies in bringing in them various phase shifts or in introducing a time delay between input and output signals.

By of active RC-filters, it is impossible to gain ideal forms of frequency characteristics in the form of rectangular with strictly constant transfer factor in bandwidth, the endless decay in a strip of suppression and endless steepness of recession at transition from bandwidth to a strip of suppression. Designing active filter always represents searching compromise between the ideal form of the characteristics and complexity of its realization. It is called as a problem of approximation (Hyde, 2003). In many cases, the requirements to quality of a filtration allow to manage the elementary filters of the 1st or 2nd order. Designing a filter in that cases is reduced

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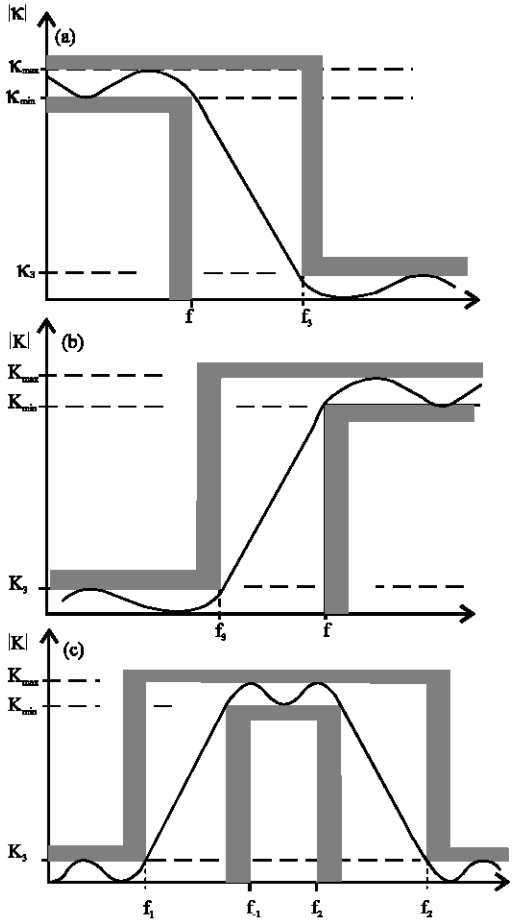

Fig. 2: Typical characteristics fo filters

to a choice of the scheme with the most suitable configuration and to the follow-on computing means of element, ratings for concrete frequencies. The analysis of a condition and tendencies of development of the theory and practice of a digital filtering show that the basic used methods are frequency selection of signals and an optimum (adaptive) filtering:

- Creating packages of application software for structure synthesis, the analysis of quality of a filtering, maintenance implementation by technical scheme and testing devices
- Perfecting existing methods of optimum projection of multistage structures with the purpose of their full formalization and including in structure of software
- Design new approaches to designing DF frequency selection with the improved quality figures

The newest engineering realizations both traditional and no conventional problems of digital processing of signals often used different technical-scheme decisions. The greatest attention of participants of section of digital filtration were on algorithms of multihigh-speed processing of complicated signals which contain as quick as slow varying components. Such algorithm should provide preliminary division of fast and slow components with downturn of sampling rate of slow components and their follow-on processing.

Modern computational capabilities allow to solve in a mode of real-time and problems of a multivariate filtration, it is essentially more complex than the digital filtration of one-dimensional signals which are carried out by means of alarm processors or multiprocessing systems. The block diagram PIC16C711 is shown in Fig. 3.

One shall list basic elements of the scheme; ALU where the elementary arithmetical operations are carried out and also logic operations; the accumulator (W) where, data of results of calculations are stored of outcomes of operations and also bits of choice of bank of memory; the register of indirect addressing (FSR) through which in directing one can turn to the RAM; memory (RAM), organized by 8-bit special registers and register of general-purpose, the working area of the user makes 68×8; the 13-bit counter of commands (Program counter), inferior 8 bats come from register PCL, seniors 5 of register PCLATH; EPROM, it makes 1K 14 bit cells of memory; the stack is 8 layered, length of a word is 13-bits during interruption contents of the counter of commands kept automatically in a stack; two bidirectional 8-bit ports A and D; 4 channel 8-bit A/D and timer 0 counter.

The chosen variant of design completely satisfies to the technical project. The microcontroller+photoelectric effect allow creating the flexible and high-powered system which meets the requirements of microdiminlature, high-speed performance, quality and simplicity of execution. Comparing the given microcontroller with the majority of modern microcontrollers, we can tell that it has rather low cost and access in the market of Ukraine.

In modern processing systems of signals high trank capacity of data and ADC for increasing precision of calculations is required also for these purposes, it is necessary that ALU could calculate operations with a floating point. The chosen microcontroller does not have given properties but owing to the speed and flexibility can reach the aims that are in the technical project (Smith, 2003). The architecture of the processor is constructed in such a manner that it is capable to execute a command for one cycle, except operations of conditional and unconditional transitions. It means that time of running, the program will be short and sampling rate of ADC will satisfy to a condition of signal's processing of a qualitative telephony. The assembler is very simple; it is

necessary to learn 35 commands. Last advantage allows to lower the time of preparation for completing the project.

SYNTHESIS OF THE PROJECTED DEVICE

The block diagram of type of realization DF is shown in Fig. 4. Parameters of parts of DF are the following:

$$Hn(Z): a_{10} = 0.25\ ,\ a_{11} = 0.125,\ b_{11} = 0.062,\ b_{12} = 0.75$$

$$Hk(Z): a_{20} = 0.25,\ \ b_{21} = 0.125$$

$$Hl(Z): a_{30} = 0.75,\ \ a_{31} = 0.5,\ \ a_{32} = 0.062,\ \ b_{32} = 0.75$$

Proceeding from this structure and also factors for each part we shall make difference in equations; the 1st part:

$$y_n = a_{10}U_m + a_{11}U_{m-1} - b_{11}y_{n-1} - b_{12}y_{n-2}$$

the 2nd part:

$$y_k = a_{20}U_m - b_{21}y_{k-1}$$

the 3rd part:

$$y_l = a_{30}(y_n + y_k) + a_{31}(y_{n-1} + y_{k-1}) + a_{32}(y_{n-2} + y_{k-2}) - b_{31}y_{l-1}$$

DESIGNING PROGRAMS IN THE ASSEMBLER`S LANGUAGE

Before writing the program, it is necessary to consider the specification of ROM microcontroller. The organization of ROM is shown in Fig. 5. It is visible that the beginning of the program (Wagner and Barr, 2002) of the user can be located below 0004h address (a 0000h address a vector of dump), 0004h (a vector of interruption). Before programming as a rule, one registers unconditional transition to the program of the user and unconditional transition to the program of processing interruption to given addresses. As in case of the, system the device carrying out inquiry of interruption is one so to the address of 0004h, it is possible to register the beginning of the program of processing interruption. By programming, it is necessary to consider the specification of banks of the RAM.

The structure of the RAM is shown in Fig. 5 and 6. By considering registers of the RAM every time, it is necessary to switch using the program between banks of the RAM, depending on that in what bank there is a register. The assembler delivered by the manufacturer, allows to all registers to appropriate the certain name instead of the address. It is convenient for making program (Walker and Morrisett, 2000). First, we shall write the program of processing of interruption.

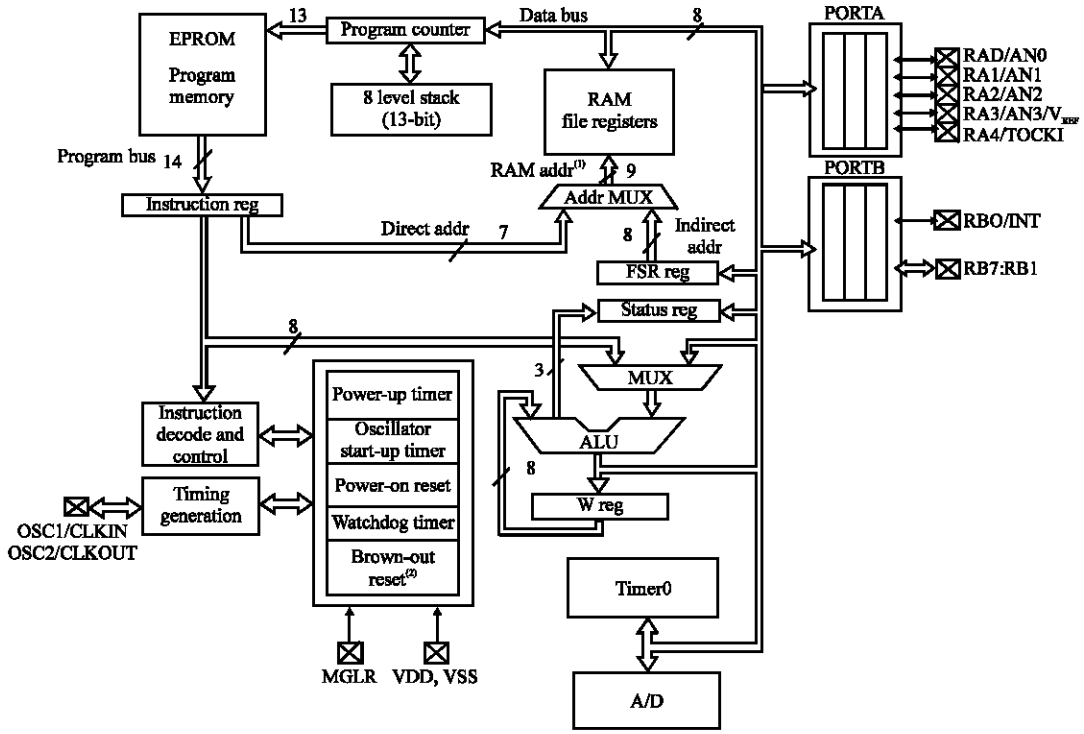

Fig. 3: Block diagram PIC16C711

We shall bring the program shown in the Table 1 with addresses of ROM and comments. The program realizing mathematical model of the filter, we shall begin with 000E h address and we shall place in Table 2.

Operations NOP are intended for synchronization of work of ADC with the program. Also for this purpose, four commands have been added before operations, above current mean of readout. In the made algorithm, the given corrections were not stipulated. Time for the program, realizing the digital filter is 49 micro sec. The interval of discrete sampling of a signal is 24.6 micro sec accordingly sampling frequency is 41000 Hz. In the

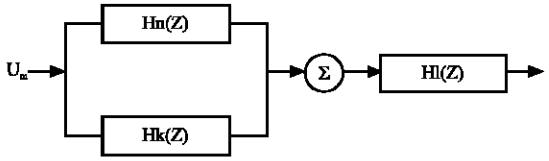

Fig. 4: The block diagram of the digital filter

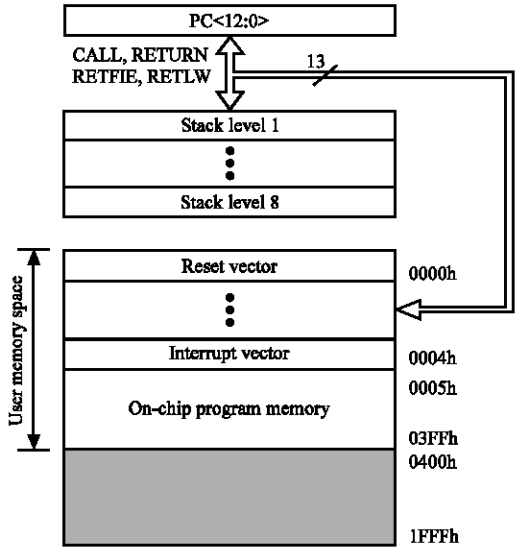

Fig. 5: Organization of ROM PIC16C71

Table 1: The program of processing of interruption with addresses and comments

Address	Name
	ORG 0×004
0004h	MOVWF W_TEMP
0005h	MOVF STATUS, 0
0006h	MOVWF STATUS_TEMP
0007h	BCF STATUS, RP0
0008h	MOVF ADRES, 0
0009h	MOVWF UM
000Ah	MOVF STATUS_TEMP, 0
000Bh	MOVWF STATUS
000Ch	MOVF W_TEMP, 0
000Dh	RETFIE

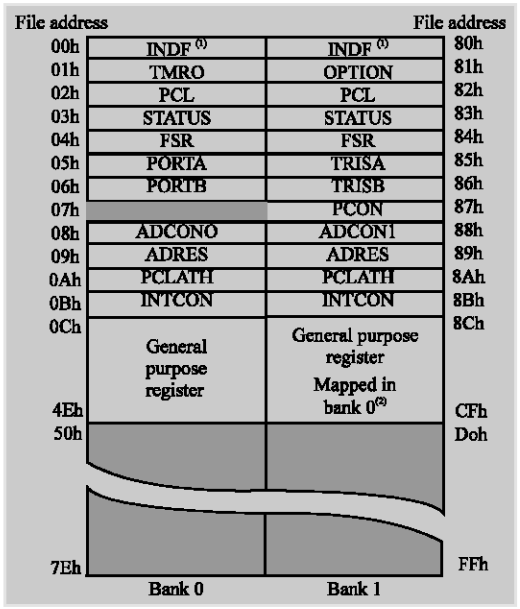

Fig. 6: Organization of ROM PIC16C71

Table 2: The program realizing mathematical model

Address		Name
		ORG 0×00E
000Eh		MOVLW 0×FF
000Fh		BSF STATUS, RP0
0010h		MOVWF TRISA
0011h		CLRF TRISB
0012h		MOVLW 0×18
0013h		BCF STATUS, RP0
0014h		MOVWF COUNT
0015h		MOVLW 0×0C
0016h		MOVWF FSR
0017h	M1:	CLRF INDF
0018h		INCF FSR, 1
0019h		DECF COUNT
001Ah		BTFSS STATUS, Z
001Bh		GOTO M1
001Ch	M2:	BSF STATUS,RP0
001Dh		CLRF ADCON1
001Eh		MOVLW 0×C1
001Fh		BCF STATUS,RP0
0020h		MOVWF ADCON0
0021h		BSF INTCON ADIE
0022h		BSF INTCON GIE
0023h		BSF ADCON0, GO
0024h		BCF STATUS, C
0025h		RRF UM1, 0
0026h		BCF STATUS, C
0027h		RRF W, 0
0028h		MOVWF A11UM1
0029h		BCF STATUS, C
002Ah		RRF YN1, 0
002Bh		BCF STATUS, C
002Ch		RRF W, 0
002Dh		BCF STATUS, C
002Eh		RRF W, 0
002Fh		BCF STATUS, C
0030h		RRF W, 0
0031h		MOVWF B11YN1
0032h		BCF STATUS, C

Table 2: Continued

Address	Name
0033h	RRF YN1, 0
0034h	ADDWF W, 0
0035h	ADDWF W, 0
0036h	ADDWF B11YN1
0037h	SUBWF A11UM1, 0
0038h	MOVWF YNN
0039h	BCF STATUS, C
003Ah	RRF UM1, 0
003Bh	MOVWF A21UM1
003Ch	BCF STATUS, C
003Dh	RRF YK1, 0
003Eh	BCF STATUS, C
003Fh	RRF W, 0
0040h	BCF STATUS, C
0041h	RRF W, 0
0042h	SUBWF A21UM1, 0
0043h	MOVWF YK
0044h	MOVF YN1, 0
0045h	ADDWF YK1
0046h	BCF STATUS, C
0047h	RRF W, 0
0048h	BCF STATUS, C
0049h	RRF W, 0
004Ah	BCF STATUS, C
004Bh	RRF W, 0
004Ch	BCF STATUS, C
004Dh	RRF W, 0
004Eh	MOVWF A31YN1YK1
004Fh	MOVF YN2, 0
0050h	ADDWF YK2
0051h	BCF STATUS, C
0052h	RRF W, 0
0053h	BCF STATUS, C
0054h	RRF W, 0
0055h	BCF STATUS, C
0056h	RRF W, 0
0057h	MOVWF A32YN2YK2
0058h	BCF STATUS, C
0059h	RRF YL1, 0
005Ah	ADDWF W, 0
005Bh	ADDWF W, 0
005Ch	SUBWF A32YN2YK2, 0
005Dh	ADDWF A31YN1YK1
005Eh	MOVWF YLL
005Fh	BCF STATUS, C
0060h	NOP
0061h	NOP
0062h	NOP
0063h	NOP
0064h	NOP
0065h	NOP
0066h	NOP
0067h	NOP
0068h	NOP
0069h	NOP
006Ah	NOP
006Bh	NOP
006Ch	NOP
006Dh	NOP
006Eh	NOP
006Fh	NOP
0070h	NOP
0071h	NOP
0072h	NOP
0073h	NOP
0074h	MOVF YK1, 0

Table 2: Continued

Address	Name
0075h	MOVWF YK2
0076h	MOVF YK, 0
0077h	MOVWF YK1
0078h	RRF UM, 0
0079h	ADDWF YNN
007Ah	MOVWF YN
007Bh	ADDWF YK
007Ch	BCF STATUS, C
007Dh	RRF W, 0
007Eh	ADDWF W, 0
007Fh	ADDWF YLL
0080h	MOVWF YL
0081h	MOVWF PORTB
0082h	MOVF YN1, 0
0083h	MOVWF YN2
0084h	MOVF YN, 0
0085h	MOVWF YN1
0086h	MOVF YL, 0
0087h	MOVWF YL1
0088h	MOVF UM, 0
0089h	MOVWF UM1
008Ah	GOTO M2
END	

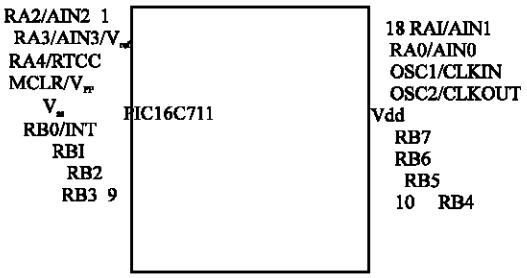

Fig. 7: Conclusion of processor PIC16C711

program, two transitions are used: one is for zeroing the RAM another for returning the program to a place of start ADC. It is possible to exclude the operation NOP by using modern PIC processors (Fig. 7).

DEVELOPMENT AND THE DESCRIPTION OF THE BASIC SCHEME

For technical realization of DF following elements are necessary:

- The processor
- DAC
- Power unit from a network 220 V, 50 Hz

Description DAC: In the capacity of DAC, the microcircuit of firm Analog Devices AD 7302 is used. Data DAC has following basic characteristics: AD 7302 Double, 8-bit DAC which works from the unipolar power supply with a pressure +2.7 to +5.5 V.

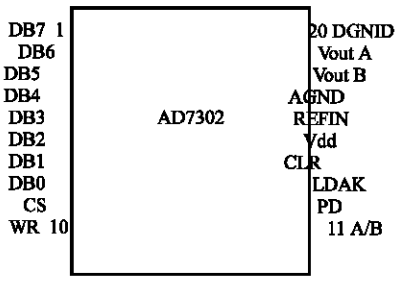

Fig. 8: Conclusion of DAC AD 7302

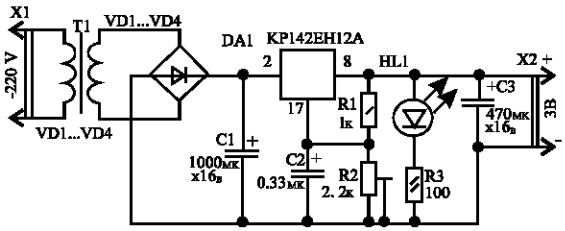

Fig. 9: Scheme of the generator

AD 7302 has the interface, compatible with a parallel output of microprocessors and Digital alarm processors (DSP). The interface possesses high-speed registers and double buffered logic. Data are loaded at the raised level on CS or WR. By means of pin ~A/B, one chooses one of 2 built DAC.

Power supply unit 220 V, 50 Hz: The brief characteristic of DAC interesting for a given problem (Fig. 8). In Fig. 9, there is a simple scheme of a power unit 3 V (a current in loading is 200 mA) with automatic electronic protection against overloading (Iз = 250 mA). The level of a pulsation of a compliance voltage does not exceed 1 mB. In the scheme as a source of a basic pressure light color diode HL1 is used. Transformer T1, it is possible to get from unified series TH but it is better to use the most small-sized TH1-127/220-50 or TH2-127/220-50. Types of transformers with a secondary winding for 5-6 V, reactors C3 type K 50-35 will be suitable as well. The scheme uses integrated stabilizer DA1 for normal work of a microcircuit, it is necessary that the entrance pressure exceeds output voltage not <3.5 V. It reduces efficiency of the balancer due to a thermal emission on a microchip by low output voltage the capacity lost in a power supply unit will exceed given one in loading. The necessary output voltage is established by tuning resistor R2. The microchip is established on a radiator.

CONCLUSION

According to results, we can estimate errors connected with numbering a signal. The basic error will be brought by limited with 8-bit wire ADC, the more levels of quantization the better. Also because of absence of operations with a floating point, division into two odd numbers will give inexact result. For numbering analog signals, the condition $Fd \geq 2F_B$ is necessary. In practice $Fd \geq 2, 5\ F_B$ is higher for better quality of a transferred signal. The spectrum of a speech signal of a qualitative telephony makes 0.3-3.4 kH ц according to the established international standard. The digital filter designed during research, meets the requirements of processing not only signals of qualitative speech but also signals with the top frequency of a spectrum 15.

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