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Analytical Model for the High Performance Si Channel N-MOS Process

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Abstract: A simple analytical expression for the 2D potential distribution in the Si channel n-MOS has been derived in the weak inversion regime. The analytical model includes the effect of short channel length, the influence of source to drain field on the substrate depletion depth through Voltage Doping Transformation (VDT), high-k dielectrics, interface trap charge density (Dit), gate work function and other device parameters. The analytical solution of the surface potential has been verified by the numerical solution of 2D Poisson's equation for two different values, the drain to source voltage V_{DS} with close agreement. Based on this model, the expression for threshold voltage V_{TH}, drain induced barrier lowering DIBL and the subthreshold slope S have been deduced. This model predictions show satisfactory agreement with the 2D numerical simulation results obtained by using MEDICI and also with reported experimental data. Further applying the model, threshold voltage and subthreshold slope have been comprehensively investigated.

Key words: Si channel n-MOS, high-k dielectrics, threshold voltage, subthreshold slope, DIBL, India

INTRODUCTON

Recently, Silicon (Si) has emerged as a promising high mobility channel material, alternative to germanium for future high performance n-MOS devices (Yamamoto *et al*., 2007; Nicholas *et al*., 2007; Zimmerman *et al*., 2006). The bulk hole mobility of Silicon is the highest of all group 4 and 3-5 semiconductor materials. There have been several reports of Si channel n-MOS with a variety of surface passivation schemes (Shasng *et al*., 2002; Chui *et al*., 2002). Some research groups performed TCAD simulations in order to forecast, the enhanced performance of Si channel n-MOS with different kinds of metal gate stacks (Mandal *et al*., 2005; Skotnicki *et al*., 1988). However, the analytical model for computing key performance parameters of the device such as threshold voltage, drain induced barrier lowering and the subthreshold slope based on the 2D surface potential approach is hardly available in the literature (Pershenkov *et al*., 1999).

In this study, we have shown an analytical model for the calculation of threshold voltage, drain induced barrier lowering and subthreshold slope of Si channel n-MOS devices with gate stacks (Bai *et al*., 2003; Taurus Medici, 2009). This model formulation entails the effect of short channel, the impact of source to drain electric field on the substrate depletion width, the interface trap density, high metal gate stacks and other material and device parameters. Based on the model, we have comprehensively investigated threshold voltage and subthreshold slope for a wide range of channel length L, Equivalent Oxide Thickness (EOT) and interface trap density.

MODELING AND SIMULATION

Formulation: A sandwich of thin oxide, silicon nitride and another thin oxide is prepared on the surface of a clean wafer. The first oxide acts as a buffer to relieve mechanical stress due to unequal thermal expansion of the substrate and nitride. The nitride also acts as a shield to prevent oxidation of the active region during field oxide growth. A layer of photo resist is deposited on the entire surface. Using a diffusion layer, the thin oxide and nitride are etched out. The open area is called as the field oxide region. A p^+ region is created by ion implantation which acts as a channel stop. A thick oxide about 1 μm is grown on top of the implanted region which together with channel stops serves neighboring active region. After this, the remaining oxide and nitride are removed. The active area will now be used for source, drain and channel regions for all transistors plus any diffusion wire needed for interconnect (Fig. 1). Electric flux at the gate-oxide and silicon channel interface is continuous, i.e.:

$$\frac{\varepsilon_{ox}}{t_{ox}}(V_{GS}-\phi_{fb}-\phi_S)=\varepsilon_{Ge}\frac{\partial\phi(x,y)}{\partial y}\Big/_{y=0} \quad (1)$$

Where, ϕ_{fb} is the flat band voltage and defined as:

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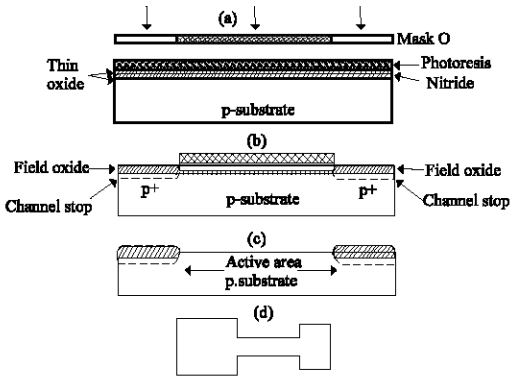

Fig. 1: a) A layer of photo resist deposited on the entire surface; b) thick oxide layer; c) oxide and nitrate removal and d) top view of the inverter circuit

$$\phi_{fb} = \phi_{ms} - \frac{Q_{it}}{C_{ox}}$$

ϕ_{ms} is the work function of the gate material with respect to silicon and Q_{it} is the interface trapped charge density per unit area given by:

$$Q_{it} = q^2 D_{it}(\phi_s - \phi_F)$$

D_{it} being the interface trap density:

$$\phi_F = -V_t \ln\left(\frac{N_D}{n_i}\right)$$

is the Fermi potential in the bulk silicon:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

is the capacitance across the gate oxide, V_t is the thermal voltage and n_i is the intrinsic carrier concentration of Si. The electric field vanishes at the depletion depth, i.e:

$$\frac{\partial \phi(x,y)}{\partial y}\Big/_{y \geq W_d} = 0 \quad (2)$$

Using Eq. 1 and 2, the coefficients $C_1(x)$ and $C_2(x)$ can be deduced as:

$$C_1(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Ge} t_{ox}}\left(\phi_S(x) - V_{GS} + \phi_{fb}\right) \quad (3)$$

and;

$$C_2(x) = -\frac{C_1(x)}{W_d} \quad (4)$$

Substituting these values in Eq. 1, we obtain:

$$\frac{\partial^2 \phi_S(x)}{\partial x^2} - \alpha \phi_S(x) + \beta = 0 \quad (5)$$

Where:

$$\alpha = \frac{C_{ox}}{W_d \varepsilon_{Ge}} \text{ and } \beta = (V_{GS} - \phi_{fb})\alpha + \frac{qN_d}{\varepsilon_{Ge}} \quad (6)$$

The solution can be written as:

$$\phi_s(x) = Ae^{\lambda x} + Be^{-\lambda x} + C \quad (7)$$

Where:

$$\lambda = \sqrt{\alpha},\ C = \frac{\beta}{\alpha}$$

By using boundary conditions, we obtain:

$$A = \frac{\left(V_{bi} + \frac{\beta}{\alpha}\right)\left(e^{\lambda L} - 1\right) + V_{DS}}{e^{-\lambda L} - e^{\lambda L}}$$

and:

$$B = \frac{\left(V_{bi} + \frac{\beta}{\alpha}\right)\left(e^{\lambda L} - 1\right) - V_{DS}}{e^{-\lambda L} - e^{\lambda L}} \quad (8)$$

In order to calculate the threshold voltage, one must know the maximum value of surface potential which is found from by setting:

$$\frac{\partial \phi_S(x)}{\partial x}\Big/_{x = x_{max}} = 0 \quad (9)$$

The maximum surface potential is evaluated as:

$$\phi_{smax} = 2\sqrt{AB} + C \quad (10)$$

The threshold voltage is an important electrical parameter which determines the electrical behavior of the MOS device. The threshold voltage V_{TH} is the value of the gate voltage at which:

$$\phi_{s\,max} = 2\phi_F \quad (11)$$

Substituting the value of V_{TH} can be obtained as:

$$V_{TH} = \left(\phi_{fb} - K - \frac{qN_D W_d}{C_{ox}}\right) \quad (12)$$

Where:

$$K = \left(\frac{K_{11} + K_{12}}{4\left(K_6 + K_6^2\right)}\right)$$

$$K_{11} = -4K_6V_{bi} - 2K_6 - 4K_6K_7 - 4K_6^2V_{bi} - 1$$

$$K_{12} = \sqrt{K_{13} + K_{14}}$$

$$K_{13} = 1 + 4K_6 + 8K_6V_{bi} + 4K_7^2$$

$$K_{14} = 8K_6^2V_{bi} + 8K_6K_7 - 8K_6\phi_{smax} - 8K_6^2\phi_{smax}$$

$$K_6 = \frac{K_3}{K_5};\ K_7 = \frac{K_4}{K_5};\ K_3 = \left(1 - e^{\lambda L}\right)$$

$$K_4 = V_{DS}e^{\lambda L} \text{ and } K_5 = e^{2\lambda L} - 1$$

Voltage-Doping Transformation (VDT): The influence of source-drain electric field on the potential barrier height has been identified as one of the important components of Short Channel Effects (SCEs). This effect can be taken into account by simply modifying the channel doping concentration, employing the voltage-doping transformation following: The modified channel doping concentration $N^*(x)$ can be deduced from the 2-D Poisson equation and is expressed as:

$$N^*(x) = N(x) + \frac{2\varepsilon_{Ge}V_{Ds}^*}{qL^2(x)} \quad (13)$$

Where:

$$V_{DS}^*(x) = V_{DS} - 2(V_{bi} + f_{smax}) - 2\sqrt{(V_{bi} + f_{smax})(-V_{DS} + V_{bi} + f_{smax})}$$

The drain induced barrier lowering DIBL can be computed as:

$$DIBL = \frac{V_{TH2} - V_{TH1}}{V_{DS2} - V_{DS1}} \quad (14)$$

Where, V_{TH1} and V_{TH2} are the value of threshold voltages at V_{DS1} and V_{DS2}, respectively. The high drain to source voltage, V_{DS1} is set at -1 V and the low drain to source voltage V_{DS2} is connected to -50 mV.

The subthreshold slope S is of great concern in controlling the turn-off characteristic of MOS. The smaller the slope, the lower the off state power of the device. The subthreshold slope S can be expressed as:

$$S = 2.3\frac{kT}{q}\left(\frac{\partial\phi_{smax}}{\partial V_{GS}}\right)^{-1} \quad (15)$$

Where:

k = The Boltzmann constant
T = The absolute temperature
V_{GS} = The gate to source voltage

RESULTS AND DISCUSSION

In order to verify the proposed analytical model, we have compared the theoretical results for the threshold voltage, Drain Induced Barrier Lowering (DIBL) and the subthreshold slope with the experimental data, reported for various channel lengths of silicon channel n-MOS. Furthermore, the 2-D device simulator MEDICI was employed to simulate the transfer characteristic of the Si channel n-MOS devices for a wide range of geometrical and material parameters. The characteristics have been utilized to extract the simulation value of threshold Voltage V_{TH}, drain induced barrier lowering DIBL and the subthreshold slope S. The simulation value of threshold voltage corresponds to the gate voltage at which volume density of inversion charge becomes equal to the channel doping concentration consistent with the model formulation. For low and high values of drain-source Voltage (V_{DS}). The maximum value of the surface potential occurs at the middle of the channel length for a low value of:

$$||V_{DS}||$$

while the maximum value of surface potential shifts towards the source end for higher value of:

$$|V_{DS}||$$

A large value of the maximum surface potential corresponds to a higher value of the threshold voltage of the device (Fig. 2). Figure 3 shows the analytical, simulation simulation and experimental results of

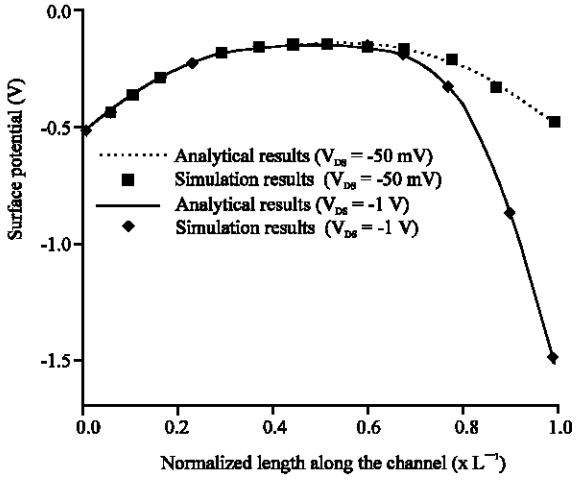

Fig. 2: Variation of surface potential with the normalized distance along the channel with V_{DS} = -50 mV and V_{DS} = -1 V

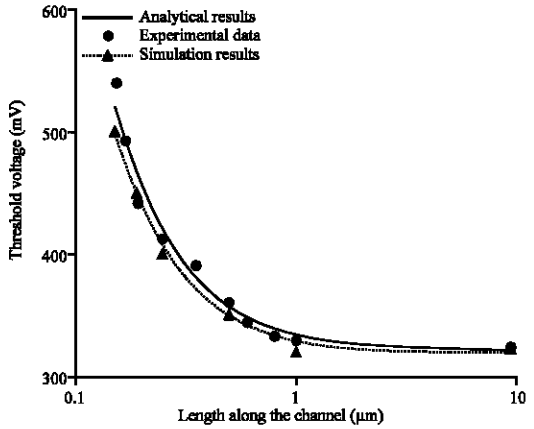

Fig. 3: Comparison of analytical, simulation and experimental results for different values of channel length with V_{DS} = -50 mV (Zimmerman *et al.*, 2006)

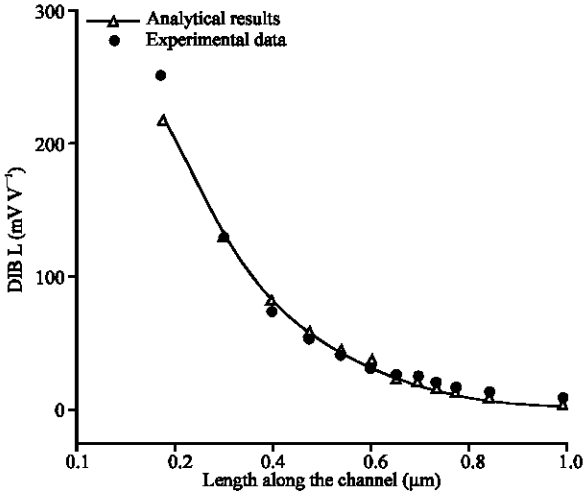

Fig. 4: Plot of DIBL against channel length with V_{DS} = -50 mV (Zimmerman *et al.*, 2006)

simulation and experimental results of voltage for different values of channel length in the range 125 nm-10 μm for Si channel n-MOS devices. Some important features are as follows: channel doping concentration is 5×10^{16} cm^{-3} and a gate stack capped by a 4 nm ALD HfO_2 gate dielectric followed by 10 nm TaN and 80 nm TiN PVD depositions. It is evident that the theoretical predictions for the threshold voltage of Si channel n-MOS devices track satisfactorily with the corresponding simulation value and also with the reported experimental data. We have also plotted the variation of DIBL for Si based n-MOS devices against the channel length (Fig. 4). One can easily observe from the Fig. 4 that the analytical results for DIBL match well with the

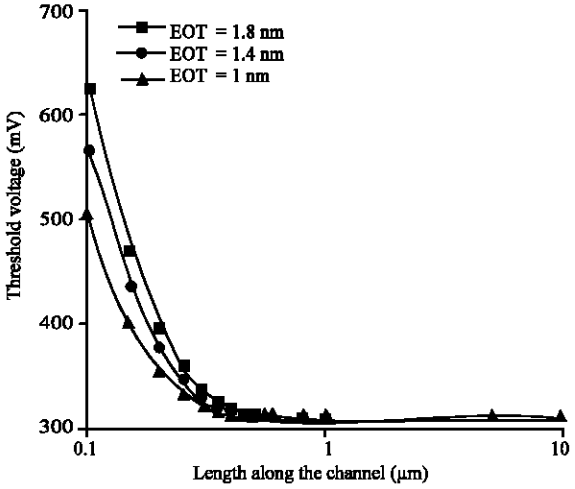

Fig. 5: Dependence of threshold voltage with channel length for different equivalent oxide thickness

Table 1: Comparison of experimental data and analytical results for subthreshold Slope (S) of Si channel n-MOS devices

Channel length (nm)	Experimental data for S (mV dec^{-1}) Yomamoto *et al.* (2007)	Analytical results for S (mV dec^{-1})
250	100	100
190	102	103
175	105	106

reported experimental results. Additionally, the results for the subthreshold slope for three different channel lengths have been shown in Table 1.

Once again, an excellent match between the predictions and reported experimental data is found. Clearly since, the predictions based on the analytical model for threshold voltage V_{TH}, drain induced barrier, lowering DIBL and subthreshold slope S, match satisfactorily with the simulation results obtained, using MEDICI and also with reported experimental data for various different devices, the validity of the model is clearly ensured. The variation of V_{TH} with the channel length of the device is shown in Fig. 5 for different values of Equivalent Oxide Thickness (EOT). As EOT increases, V_{TH} rises and the rate of rise is considerable particularly for channel lengths below 300 nm.

Figure 6 shows the dependence of V_{TH} against EOT with channel length as a parameter. The sensitivity of V_{TH} with EOT in particular for EOT <6 nm is considerable and as EOT >6 nm, V_{TH} increases slowly with EOT. Another notable feature of the plot is that the variation of V_{TH} with EOT for a shorter channel device is more pronounced than one with a larger channel length. Figure 7 shows the variation of S with both channel length and interface trap density. The dependence of S on L is

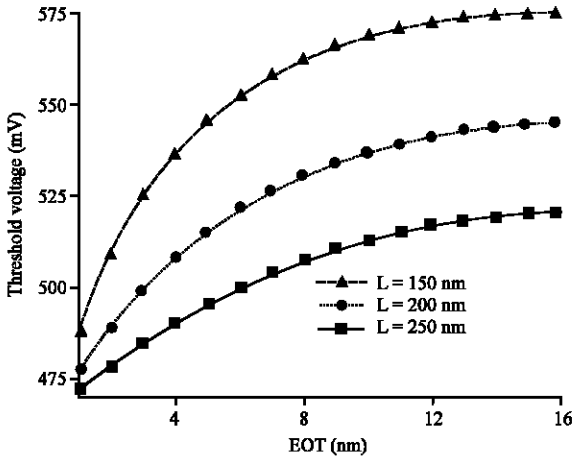

Fig. 6: Threshold voltage vs. effective oxide thickness for three different channel length

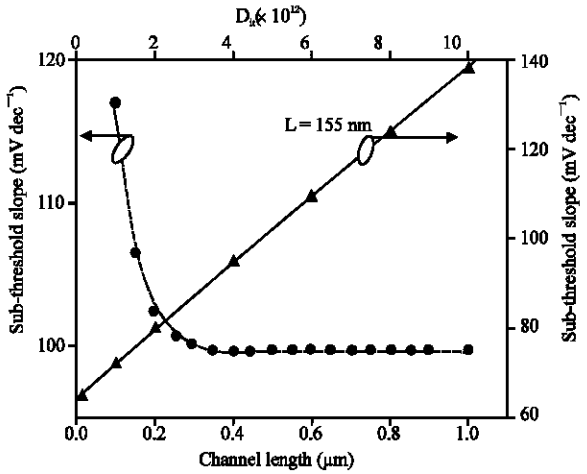

Fig. 7: Plot of sub-threshold slope with channel length and D_{it} for V_{DS} = -50 mV

nonlinear while on D_{it} is linear. The sub-threshold slope increases significantly with decreasing channel length particularly for L<250 nm. This feature indicates the early initiation of the short channel effects in comparison with the germanium devices.

CONCLUSION

The influence of various material and device parameters like channel length, equivalent oxide thickness, interface trap density, etc. on the device performance metrics such as threshold voltage, drain induced barrier, lowering and sub-threshold slope of Si channel n-MOS has been intensively investigated by developing an analytical model for the same. Based on the model, the prediction results show satisfactory concordance with the numerical simulation results and also with reported experimental data. Most importantly, the results point out that as the channel length reduces <0.25 μm, the threshold voltage rises considerably indicating the beginning of the short channel effect unlike Si n-MOS. Also both the DIBL and S deteriorate for channel lengths <250 nm.

Further threshold voltage reduces linearly <6 nm of EOT and its rate of rise with EOT is less than linear for EOT >6 nm for channel length in the range 150-250 nm. The model accurately predicts different performance metrics over a large range of material and device parameters and can be effectively employed to design and characterize high performance Si channel n-MOS with the desired performance.

REFERENCES

Bai, W.P., N. Lu, J. Liu, A. Ramirez and D.L. Kwong *et al.*, 2003. Ge MOS characteristics with CVD HfO_2 gate dielectrics and TaN gate electrode. Proceedings of the Symposium on VLSI Technology, Digest of Technical Papers, June 10-12, Francisco, CA., USA., pp: 121-122.

Chui, C.O., H. Kim, D. Chi, B.B. Triplett, P.C. Mcintyre and K.C. Saraswat, 2002. A sub-400°C germanium MOSFET technology with high-k dielectric and metal gate. Proceedings of the International Electron Devices Meeting, (IEDM'02), Francisco, CA., USA., pp: 437-440.

Mandal, S.K., S. Chakraborty, C.K. Maiti, 2005. Ge-channel p-MOSFETs with ZrO_2 gate dielectrics. Microelectron. Eng., 81: 206-211.

Nicholas, G., B.D. Jaeger, D.P. Brunco, P. Zimmerman and G. Eneman *et al.*, 2007. High-performance deep submicron Ge pMOSFETs with halo implants. IEEE Trans. Electron Devices, 54: 2053-2511.

Pershenkov, V.S., S.V. Cherepko, R.E. Ivanov, A.V. Shalnov, V.V. Abramov, 1999. Single transistor technique for interface trap density measurement in irradiated MOS devices. Microelectron. Reliab., 39: 497-505.

Shasng, H., H. Okorn-Schimdt, K.K. Chan, M. Copel and J.A. Ott *et al.*, 2002. High mobility p-channel germanium MOSFETs with a thin Ge oxynitride gate dielectric. Proceedings of the International Electron Devices Meeting, (IEDM'02), Francisco, CA., USA., pp: 441-444.

Skotnicki, T., G. Merckel and T. Pedron, 1988. The voltage-doping transformation: A new approach to the modeling of MOSFET short-channel effects. IEEE Electron Device Lett., 9: 109-112.

Taurus Medici, 2009. Medici User Guide, Version C-2009.06. Synopsys Inc., Schaumburg, IL., USA.

Yamamoto, T., Y. Yamashita, M. Harada, N. Taoka and K. Ikeda *et al*., 2007. High performance 60nm gate length germanium p-MOSFETs with Ni germanide metal source/drain. Proceedings of the IEEE International Electron Devices Meeting, Dec. 10-12, Washington, DC., pp: 1041-1043.

Zimmerman, P., G. Nicholas, B. DeJaeger, B. Kaczer and A. Stesmans *et al*., 2006. High performance Ge pMOS devices using a Si-compatible process flow. Proceedings of the International Electron Devices Meeting, Dec. 11-13, San Francisco, CA., USA., pp: 1-4.